9. Reviewing Printed Circuit Board Schematics with the Quartus II Software

This chapter provides guidelines for reviewing printed circuit board (PCB) schematics with the Quartus® II software. Altera FPGAs and CPLDs offer a multitude of configurable options to allow you to implement a custom application-specific circuit on your PCB.

Your Quartus II project provides important information specific to your programmable logic design, which you can use in conjunction with the device literature available on Altera’s website to ensure that you implement the correct board-level connections in your schematic.

This chapter highlights the important options in the Quartus II software, including Settings dialog box options, the Fitter report, and Messages window to which you should refer when creating and reviewing your PCB schematic. The Quartus II software also provides useful tools, such as the Pin Planner and the SSN Analyzer, to assist you during your PCB schematic review process.

The “Reviewing Quartus II Software Settings” section provides information about the settings you can make in the Quartus II software to help you review your PCB schematic. After verifying options in the Quartus II software, you can compile your design and use the data generated in the Fitter report, which is described in “Reviewing Device Pin-Out Information in the Fitter Report” on page 9–4 to verify settings in your PCB schematic. You should also ensure that you carefully review error and warning messages, as described in “Reviewing Compilation Error and Warning Messages” on page 9–6.

In addition to verifying your settings in the Settings dialog box and Fitter report, and checking messages, you can turn on additional settings, as described in “Using Additional Quartus II Software Features” on page 9–6 and “Using Additional Quartus II Software Features” on page 9–6.

Finally, Quartus II software tools, such as the Pin Planner and the SSN Analyzer, described in “Using Additional Quartus II Software Tools” on page 9–7, help you to verify proper I/O placement.

You should use this chapter in conjunction with Altera's device family-specific literature.

For more information, refer to the Schematic Review Worksheets and the Pin Connection Guidelines pages of the Altera.com website.
Reviewing Quartus II Software Settings

The **Device** dialog box in the Quartus II software allows you to specify device-specific assignments and settings. You can use the **Device** dialog box to specify general project-wide options, including specific device and pin options, which help you to implement correct board-level connections in your PCB schematic.

The **Device** dialog box provides project-specific device information, including the target device and any migration devices you specify. Using migration devices can impact the number of available user I/O pins and internal resources, as well as require connection of some user I/O pins to power/ground pins to support migration.

If you want to use vertical migration, which allows you to use different devices with the same package, you can specify your list of migration devices in the **Migration Devices** dialog box. The Fitter places the pins in your design based on your targeted migration devices, and allows you to use only I/O pins that are common to all of the migration devices.

For more information about the **Migration Devices** dialog box in the Quartus II software, refer to *Migration Devices Dialog Box* in Quartus II Help.

If a migration device has pins that are power or ground, but the pins are also user I/O pins on a different device in the migration path, the Fitter ensures that these pins are not used as user I/O pins. You must ensure that these pins are connected to the appropriate plane on the PCB.

If you are migrating from a smaller device with NC (no-connect) pins to a larger device with power or ground pins in the same package, you can safely connect the NC pins to power or ground pins to facilitate successful migration.

### Device and Pins Options Dialog Box Settings

You can verify important design-specific data in the **Device and Pin Options** dialog box when reviewing your PCB schematic, including options found on the **Configuration**, **Unused Pin**, **Dual-Purpose Pins**, and **Voltage** pages.

#### Configuration Page Settings

The **Configuration** page of the **Device and Pin Options** dialog box specifies the configuration scheme and configuration device for the target device. Use the **Configuration** page settings to verify the configuration scheme with the MSEL pin settings used on your PCB schematic and the I/O voltage of the configuration scheme.

Your specific configuration settings may impact the availability of some dual-purpose I/O pins in user mode. Refer to “Dual-Purpose Pins Page Settings” on page 9–3 for more information.
### Unused Pin Page Settings

The Unused Pin page specifies the behavior of all unused pins in your design. Use the Unused Pin page to ensure that unused pin settings are compatible with your PCB. For example, if you reserve all unused pins as outputs driving ground, you must ensure that you do not connect unused I/O pins to VCC pins on your PCB. Connecting unused I/O pins to VCC pins may result in contention that could lead to higher than expected current draw and possible device overstress.

The Reserve all unused pins list shows available unused pin state options for the target device. The default state for each pin is the recommended setting for each device family.

When you reserve a pin as output driving ground, the Fitter connects a ground signal to the output pin internally. You should connect the output pin to the ground plane on your PCB, although you are not required to do so. Connecting the output driving ground to the ground plane is known as creating a virtual ground pin, which helps to minimize simultaneous switching noise (SSN) and ground bounce effects.

### Dual-Purpose Pins Page Settings

The Dual-Purpose Pins page specifies how configuration pins should be used after device configuration completes. You can set the function of the dual-purpose pins by selecting a value for a specific pin in the Dual-purpose pins list. Pin functions should match your PCB schematic. The available options on the Dual-Purpose Pins page may differ depending on the selected configuration mode.

### Voltage Page Settings

The Voltage page specifies the default VCCIO I/O bank voltage and the default I/O bank voltage for the pins on the target device. VCCIO I/O bank voltage settings made in the Voltage page are overridden by I/O standard assignments made on I/O pins in their respective banks. Refer to the “Reviewing Device Pin-Out Information in the Fitter Report” on page 9–4 for more details about the I/O bank voltages for your design.

### Error Detection CRC Page Settings

The Error Detection CRC page specifies error detection cyclic redundancy check (CRC) use for the target device. When Enable error detection CRC is turned on, the device checks the validity of the programming data in the devices. Any changes made in the data while the device is in operation generates an error.

Turning on the Enable open drain on CRC error pin option allows the CRC ERROR pin to be set as an open-drain pin in some devices, which decouples the voltage level of the CRC ERROR pin from VCCIO voltage. You must connect a pull-up resistor to the CRC ERROR pin on your PCB if you turn on this option.

In addition to settings in the Device dialog box, you should verify settings in the Voltage page of the Settings dialog box.

For more information about the Device and Pins Options dialog box in the Quartus II software, refer to Device and Pin Options Dialog Box in Quartus II Help.
**Voltage Page Settings**

The Voltage page, under Operating Settings and Conditions in the Settings dialog box, allows you to specify voltage operating conditions for timing and power analyses. Ensure that the settings in the Voltage page match the settings in your PCB schematic, especially if the target device includes transceivers.

The Voltage page settings requirements differ depending on the settings of the transceiver instances in the design. Refer to the Fitter report for the required settings, and verify that the voltage settings are correctly set up for your PCB schematic.

For more information about voltage settings, refer to the Pin Connection Guidelines page of the Altera.com website.

Once you verify your settings in the Device and Settings dialog boxes, you can verify your device pin-out with the Fitter report.

**Reviewing Device Pin-Out Information in the Fitter Report**

After you compile your design, you can use the reports in the Resource section of the Fitter report to check your device pin-out in detail.

The Input Pins, Output Pins, and Bidirectional Pins reports identify all the user I/O pins in your design and the features enabled for each I/O pin. For example, you can find use of weak internal pull-ups, PCI clamp diodes, and on-chip termination (OCT) pin assignments in these sections of the Fitter report. You can check the pin assignments reported in the Input Pins, Output Pins, and Bidirectional Pins reports against your PCB schematic to determine whether your PCB requires external components.

These reports also identify whether you made pin assignments or if the Fitter automatically placed the pins. If the Fitter changed your pin assignments, you should make these changes user assignments because the location of pin assignments made by the Fitter may change with subsequent compilations.
Figure 9–1 shows the pins the Fitter chose for the OCT external calibration resistor connections (RUP/RDN) and the name of the associated termination block in the Input Pins report. You should make these types of assignments user assignments.

**Figure 9–1. Resource Section Report**

The I/O Bank Usage report provides a high-level overview of the VCCIO and VREF requirements for your design, based on your I/O assignments. Verify that the requirements in this report match the settings in your PCB schematic. All unused I/O banks, and all banks with I/O pins with undefined I/O standards, default the VCCIO voltage to the voltage defined in the Voltage page of the Device and Pin Options dialog box.

The All Package Pins report lists all the pins on your device, including unused pins, dedicated pins and power/ground pins. You can use this report to verify pin characteristics, such as the location, name, usage, direction, I/O standard and voltage for each pin with the pin information in your PCB schematic. In particular, you should verify the recommended voltage levels at which you connect unused dedicated inputs and I/O and power pins, especially if you selected a migration device. Use the All Package Pins report to verify that you connected all the device voltage rails to the voltages reported.

Errors commonly reported include connecting the incorrect voltage to the predriver supply (VCCPD) pin in a specific bank, or leaving dedicated clock input pins floating. Unused input pins that should be connected to ground are designated as GND+ in the Pin Name/Usage column in the All Package Pins report.

You can also use the All Package Pins report to check transceiver-specific pin connections and verify that they match the PCB schematic. Unused transceiver pins have the following requirements, based on the pin designation in the Fitter report:

- **GXB_GND**—Unused GXB receiver or dedicated reference clock pin. This pin must be connected to GXB_GND through a 10k Ohm resistor.
- **GXB_NC**—Unused GXB transmitter or dedicated clock output pin. This pin must be disconnected.
Some transceiver power supply rails have dual voltage capabilities, such as VCCA_L/R and VCCH_L/R, that depend on the settings you created for the ALTGX MegaWizard Plug-In Manager. Because these user-defined settings overwrite the default settings, you should use the All Package Pins report to verify that these power pins on the device symbol in the PCB schematics are connected to the voltage required by the transceiver. An incorrect connection may cause the transceiver to function not as expected.

If your design includes a memory interface, the DQS Summary report provides an overview of each DQ pin group. You can use this report to quickly confirm that the correct DQ/DQS pins are grouped together. This section also provides information on DLL usage.

Finally, the Fitter Device Options report summarizes some of the settings made in the Device and Pin Options dialog box. Verify that these settings match your PCB schematics.

**Reviewing Compilation Error and Warning Messages**

If your project does not compile without error or warning messages, you should resolve the issues identified by the Compiler before signing off on your pin-out or PCB schematic. Error messages often indicate illegal or unsupported use of the device resources and IP.

Additionally, you should cross-reference fitting and timing analysis warnings with the design implementation. Timing may be constrained due to nonideal pin placement. You should investigate if you can reassign pins to different locations to prevent fitting and timing analysis warnings. Ensure that you review each warning and consider its potential impact on the design.

**Using Additional Quartus II Software Features**

You can generate IBIS files, which contain models specific to your design and selected I/O standards and options, with the Quartus II software.

Because board-level simulation is important to verify, you should check for potential signal integrity issues. You can turn on the Board-Level Signal Integrity feature in the EDA Tool Settings page of the Settings dialog box.

For more information about signal integrity analysis in the Quartus II software, refer to the Signal Integrity Analysis with Third-Party Tools chapter in volume 3 of the Quartus II Handbook.

Additionally, using advanced I/O timing allows you to enter physical PCB information to accurately model the load seen by an output pin. This feature facilitates accurate I/O timing analysis.

For more information about advanced I/O timing, refer to the I/O Management chapter in volume 2 of the Quartus II Handbook.
Using Additional Quartus II Software Tools

This section describes additional tools found in the Quartus II software, specifically the Pin Planner and the SSN Analyzer, and how you can use these tools to assist you with reviewing your PCB schematics.

**Pin Planner**

The Quartus II Pin Planner helps you visualize, plan, and assign device I/O pins in a graphical view of the target device package. You can quickly locate various I/O pins and assign them design elements or other properties to ensure compatibility with your PCB layout.

You can use the Pin Planner to verify the location of clock inputs, and whether they have been placed on dedicated clock input pins, which is recommended when your design uses PLLs.

You can also use the Pin Planner to verify the placement of dedicated SERDES pins. SERDES receiver inputs can be placed only on DIFFIO_RX pins, while SERDES transmitter outputs can be placed only on DIFFIO_TX pins.

The Pin Planner gives a visual indication of signal-to-signal proximity in the Pad View window, and also provides information about differential pin pair placement, such as the placement of pseudo-differential signals.

For more information about the Pin Planner, refer to the I/O Management chapter in volume 2 of the Quartus II Handbook.

**SSN Analyzer**

The SSN Analyzer supports pin planning by estimating the voltage noise caused by the simultaneous switching of output pins on the device. Because of the importance of the potential SSN performance for a specific I/O placement, you can use the SSN Analyzer to analyze the effects of aggressor I/O signals on a victim I/O pin.

For more information about the SSN Analyzer, refer to the Simultaneous Switching Noise (SSN) Analysis and Optimizations chapter in volume 2 of the Quartus II Handbook.

**Conclusion**

This chapter describes guidelines and descriptions of settings to verify when reviewing your PCB schematic with the Quartus II software. You can use settings in the Settings dialog box; information in the Fitter report and Messages window; and the Pin Planner and SSN Analyzer during the PCB schematic review process.
Document Revision History

Table 9–1 shows the revision history for this chapter.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
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<tbody>
<tr>
<td>November 2012</td>
<td>12.1.0</td>
<td>Minor update of Pin Planner description for task and report windows.</td>
</tr>
<tr>
<td>June 2012</td>
<td>12.0.0</td>
<td>Removed survey link.</td>
</tr>
<tr>
<td>November 2011</td>
<td>10.0.2</td>
<td>Template update.</td>
</tr>
<tr>
<td>December 2010</td>
<td>10.0.1</td>
<td>Changed to new document template. No change to content.</td>
</tr>
<tr>
<td>July 2010</td>
<td>10.0.0</td>
<td>Initial release.</td>
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For previous versions of the Quartus II Handbook, refer to the Quartus II Handbook Archive.