

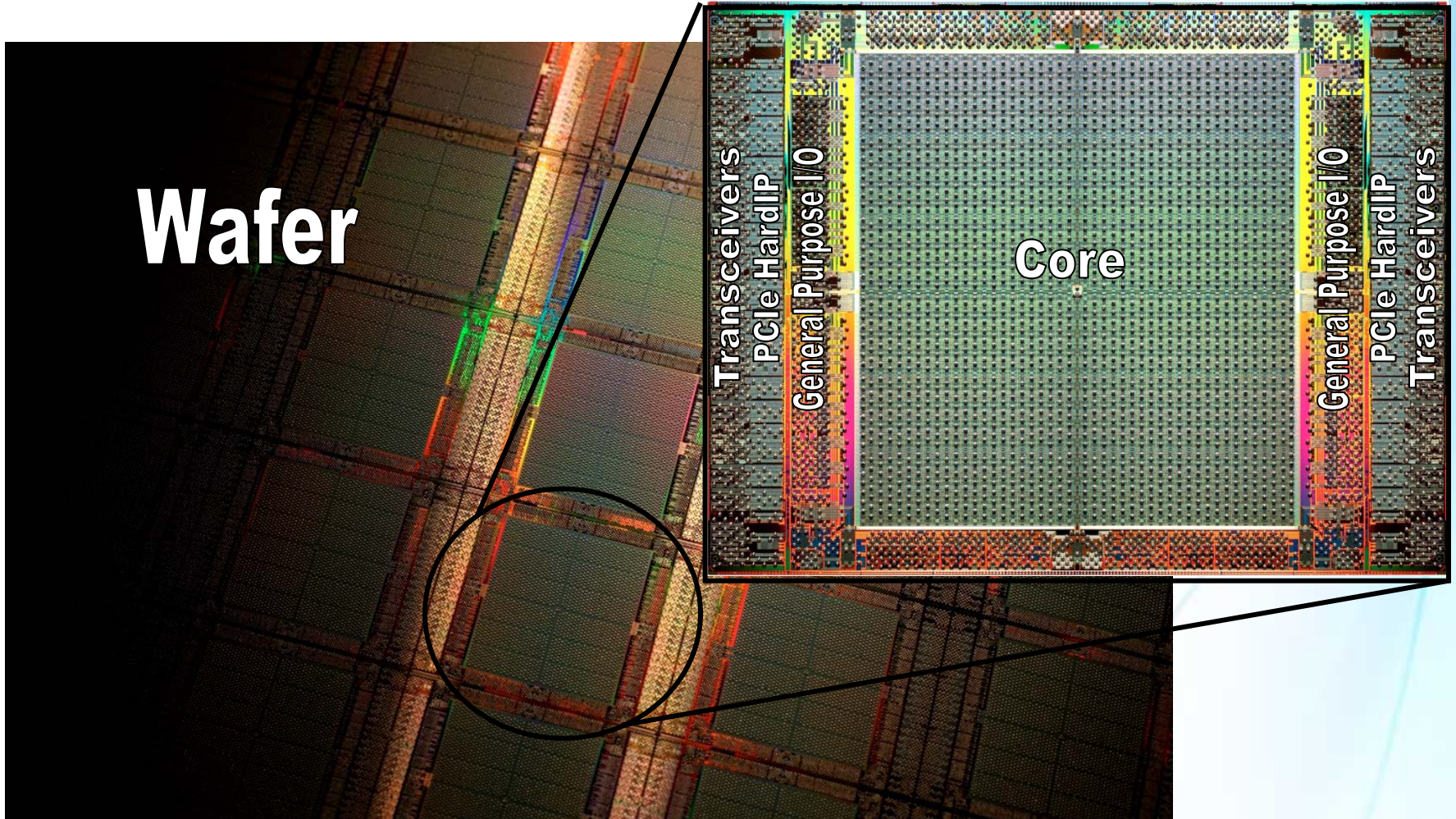
# FPGA Challenges and Opportunities

*Prof. Stephen Brown  
University Program Director  
Altera*



# Altera Stratix IV GX

40 nm: 2.5 billion transistors



# Why FPGAs use the Latest Technology

- Each new transistor technology:  
130 nm, 90 nm, 65 nm, 40 nm, 28 nm →  
  
~2X transistors
  - More logic elements, more RAM, more DSP blocks, ...
  - More processing on one chip
    - Lower system cost & power
    - Enable higher performance systems
  - New features:
    - High-speed serial I/O, memory interfaces, hard IP

# Why ASICs Don't!

## ■ Standard cell ASIC @ 40 nm

- ~\$4 M / mask set \* 2 spins = \$8 M
- Test & product engineering ~\$7 M
- Design, verification, software ~\$25 M

## ■ Economics

- \$40 M development cost
- 20% of revenue on R & D → need \$200 M revenue
- 10% market share → Need a \$2 B market

## ■ Result

- Falling ASIC starts: most still in 130 nm and above
- Structured ASICs
- ASICs increasing programmability → try to increase market size

# FPGAs are Process Leaders

## ■ Altera Stratix IV

- Shipped in 2008
- **First 40 nm FPGA** & one of the first 40 nm chips
  - FPGA designed simultaneously with 40 nm process
- **3 years & >\$200 million** to develop hardware + software + IP
- Process driver: large & regular; contains logic & RAM
- 40 nm allows integration of new hard (“ASIC”) functions

## ■ Pipelined development

- 28 nm underway for two years

# Altera Stratix IV Advances

| Feature                 | Stratix III (65 nm)                   | Stratix IV (40 nm)   |
|-------------------------|---------------------------------------|--|
| Logic Elements          | 340k                                  | 820k   |
| RAM bits                | 16 Mb + 4 Mb                          | 33 Mb + 8.5 Mb   |
| 18x18 multipliers       | 768                                   | 1360   |
| General I/O             | 1104                                  | 1104   |
| High-speed serial links | 0                                     | 48 transmit + 48 receive<br>@ 11.3 Gb/s                        |
| Hard PCIe blocks        | 0                                     | 4  |
| Clock generation        | 12 PLL(x10)                           | 12 PLL(x10) +<br>32 serial recovered +<br>+ 24 serial transmit |
| Clock distribution      | 16 Global + 88 Quadrant<br>+ 132 PCLK | 16 Global + 88 Quadrant<br>+ 132 PCLK                          |

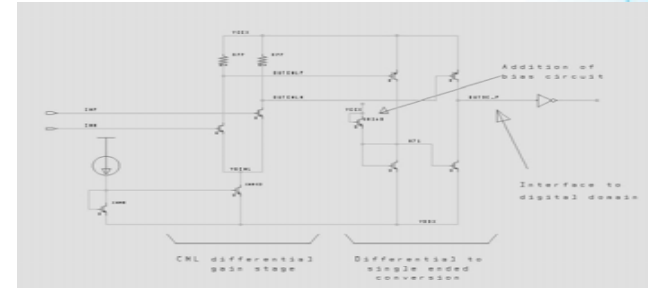
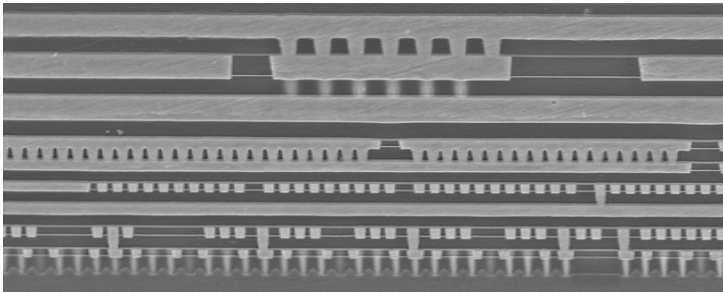
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# Technology Challenges



# FPGA Fabric: Converging Technologies

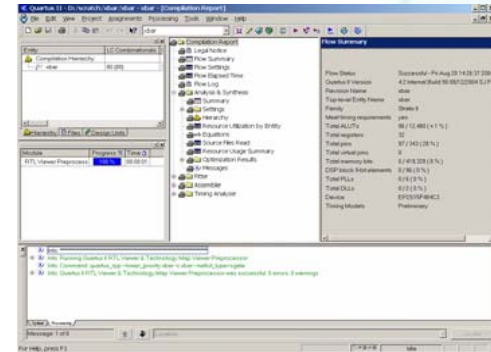
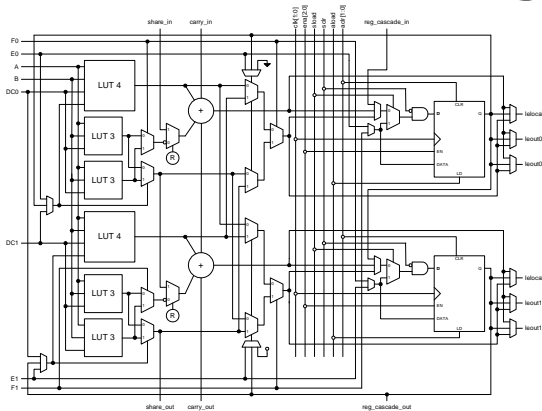
- Huge space → no one can optimize by instinct
- \$200 M + 3 years to implement your ideas



**Process Technology**

**Circuit Design**

**Optimize**



**FPGA Architecture**

**Software**

# Architect via Virtual Prototyping



**FPGA Arch. Spec (150 pages)**

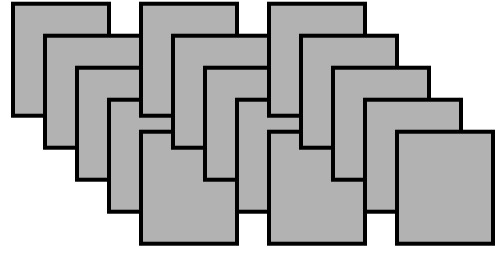
**VPR++**

**FPGA Database (1 GB)**

```

# User-specified parameters
archdefn_arch_name = "archdefn_arch_name"
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Customer Designs  
IP, Reference Designs

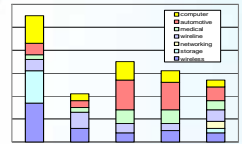
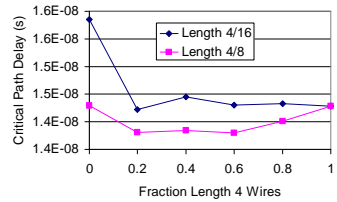


**Parameterized Quartus Synthesis**

**VPR++ Place & Route**

**Timing, Area, Power Models**

**VPR++ Analysis: Speed, Area, Routability, Power**



# Major Innovations

| Family                 | Major Innovation                                     | Benefit   |
|------------------------|--|---|
| Stratix<br>(130 nm)    | 100% Direct-drive,<br>Optimized<br>segmented routing | +40% Fmax,<br>-40% area vs. APEX<br><i>(not including process adv.)</i>   |
| Stratix II<br>(90 nm)  | Adaptive Logic<br>Module                             | +26% Fmax,<br>-7% area vs. Stratix<br><i>(not including process adv.)</i> |
| Stratix III<br>(65 nm) | Programmable<br>Power                                | Full speed of 65 nm process, ½<br>leakage power of 90 nm                  |

# I/O Bandwidth

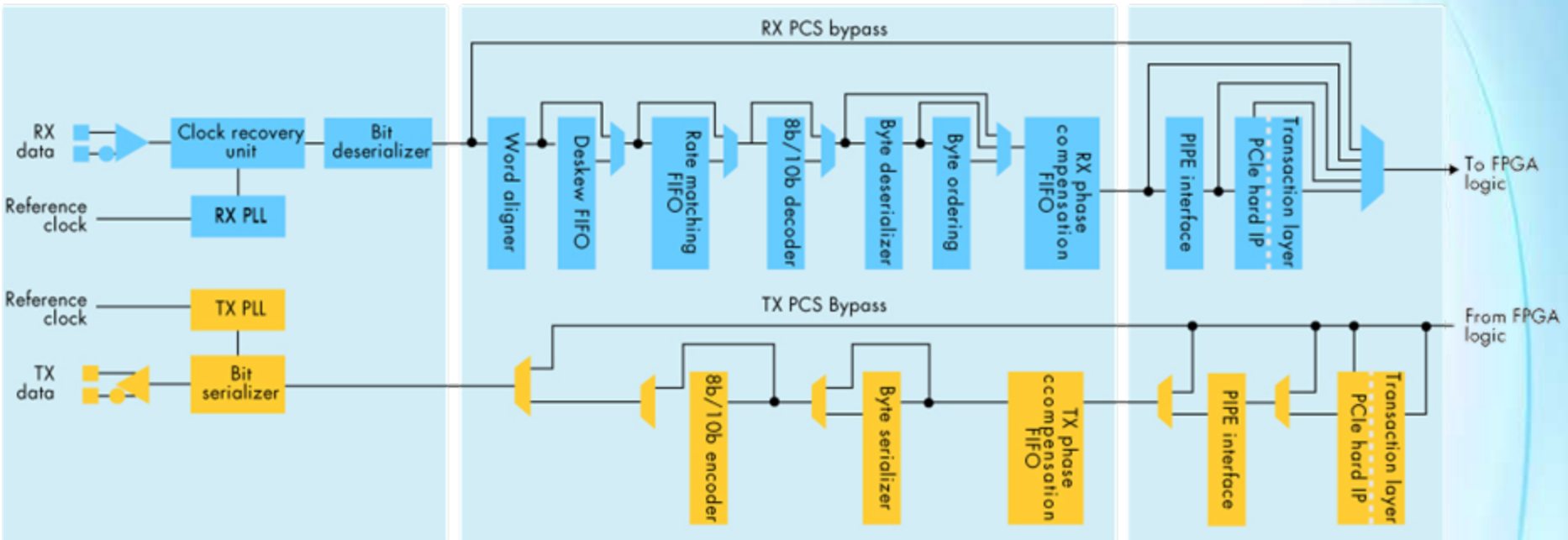
- Processing elements scale
  - ~2X more logic, RAM, DSP each generation
  - Stratix IV on-chip RAM bandwidth ~10 TB/s!
- I/O transistors, PCB traces, package balls don't scale
  - Roughly same number of I/Os per device
- Need: higher speed I/Os to keep datapath fed
  - 8.5 (SIVGX) to 11.3 (SIVGT) Gb/s serial transceivers
  - 1.067 Gb/s (533 MHz) memory interfaces
  - Total: ~150 GB/s bandwidth
- Challenges
  - Circuit speed & timing closure
  - Signal integrity

# Stratix IV GX Embedded Transceivers

## PMA (Analog)

## PCS (Digital)

## PCIe Protocol

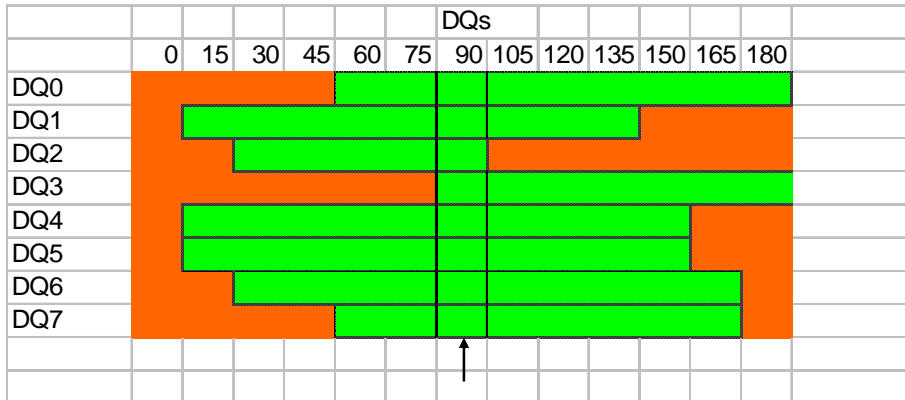


- Up to 48 receive + 48 transmit transceivers
  - 3 Gb/s to 11.3 Gb/s
  - Clock recovered from data stream
- Very high speed analog
- Many protocols → highly configurable analog & digital logic

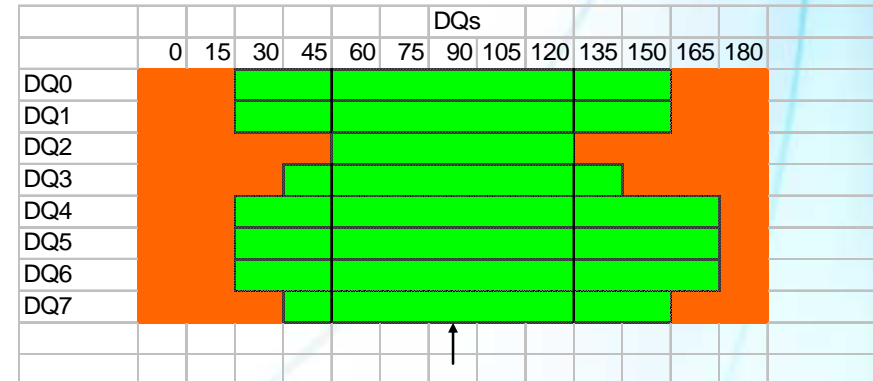
# Memory Interfaces (DDR2, DDR3, ...)

- Strobe (DQS) sent with several bits of data (DQ)
- Challenge: narrow data-valid window
- Solution:
  - Minimize jitter
  - Harden data capture logic, carefully match delays
  - **Calibrate** by modifying programmable delays for each DQ bit & DQS

Before de-skew -- small valid capture window



De-skew maximizes valid capture window

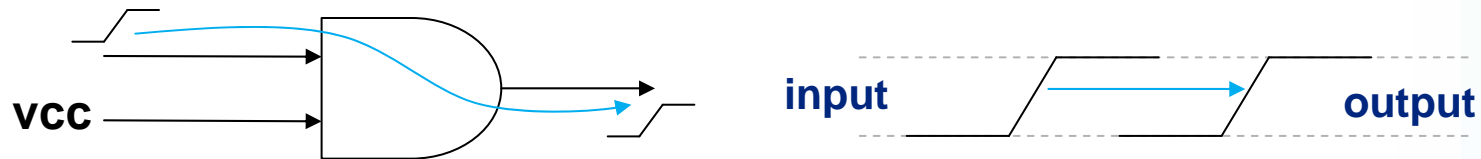


# Device Modeling Challenges

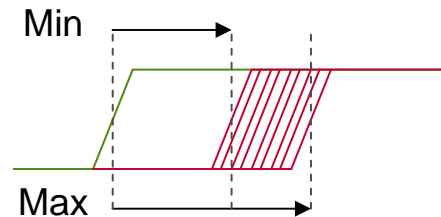
- Smaller transistors
  - More process variation
- Lower operating voltage, with little  $V_{th}$  scaling
  - Increased sensitivity to power supply noise
- Faster clock speeds and edge rates
  - Less ability to guardband
  - Increased importance of jitter & signal integrity models
- Still need fast, easy-to-interpret analysis

# ASIC Class Timing Analysis (Timequest)

- Model rise-rise, rise-fall, fall-rise, fall-fall delays
  - Propagate rise and fall delays through circuit

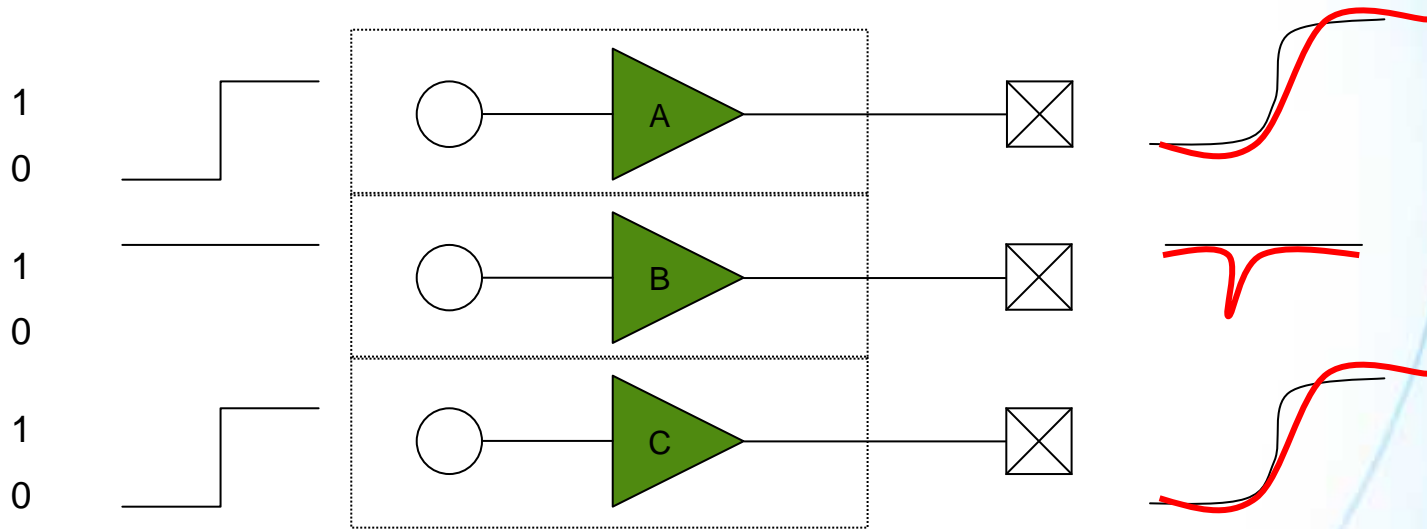


- Each delay is a min-max range
  - Covers on-die variation, transistor aging effects



# Simultaneous switching noise (SSN)

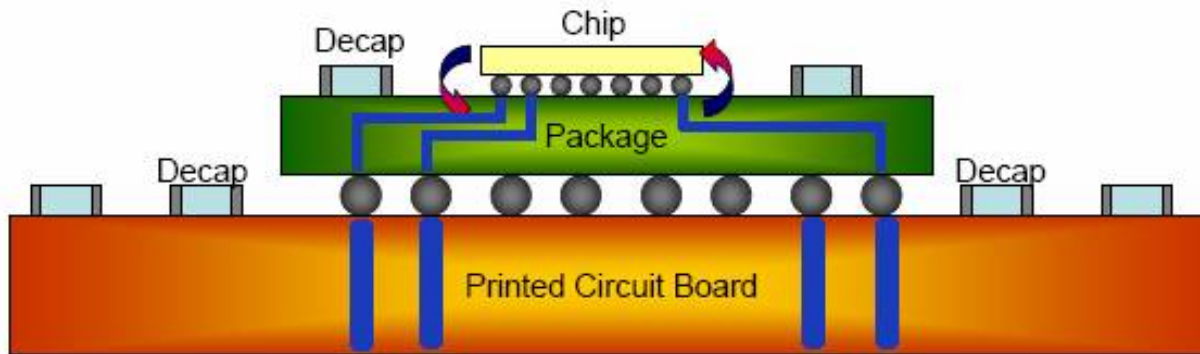
- Noise induced on *victim* I/O due to switching of other *aggressor* I/Os



- Faster edge rates & higher I/O density worsen
- Reduce with FPGA & package design
- But cannot eliminate failures for all designs, on all boards

# Quartus II SSN Analyzer

- Models FPGA, package and board



- HSPICE (full design): 1 week
- SSN Analyzer: 30 minutes
- Displays signal margin & problem pins
- Enables analysis of mitigation techniques



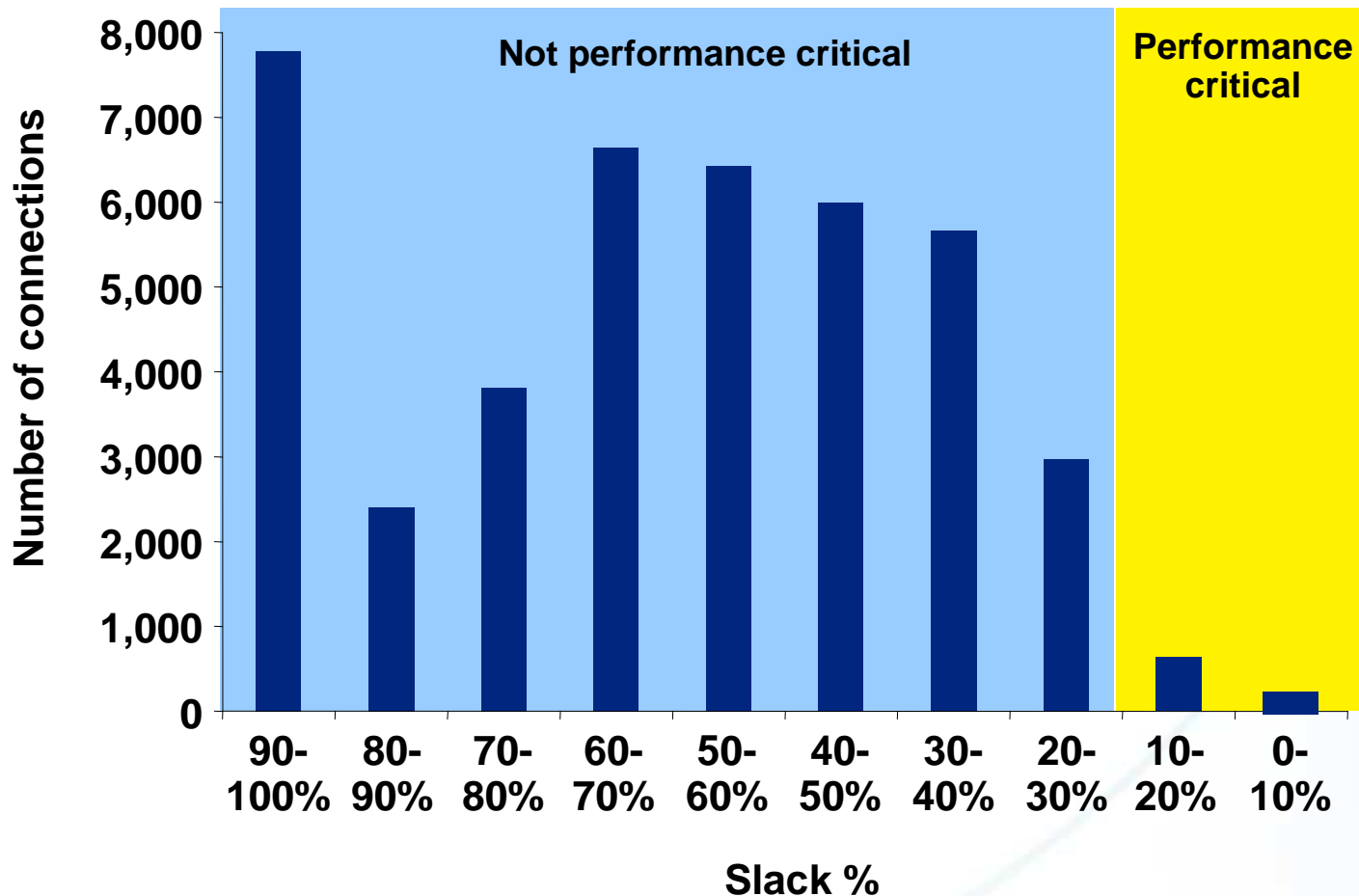
# Power

- Twice as many transistors
  - Naturally more leaky
  - But power budget per device fixed
    - About 2 – 20 W for high-end FPGAs
- Innovate to control power while sacrificing minimum performance

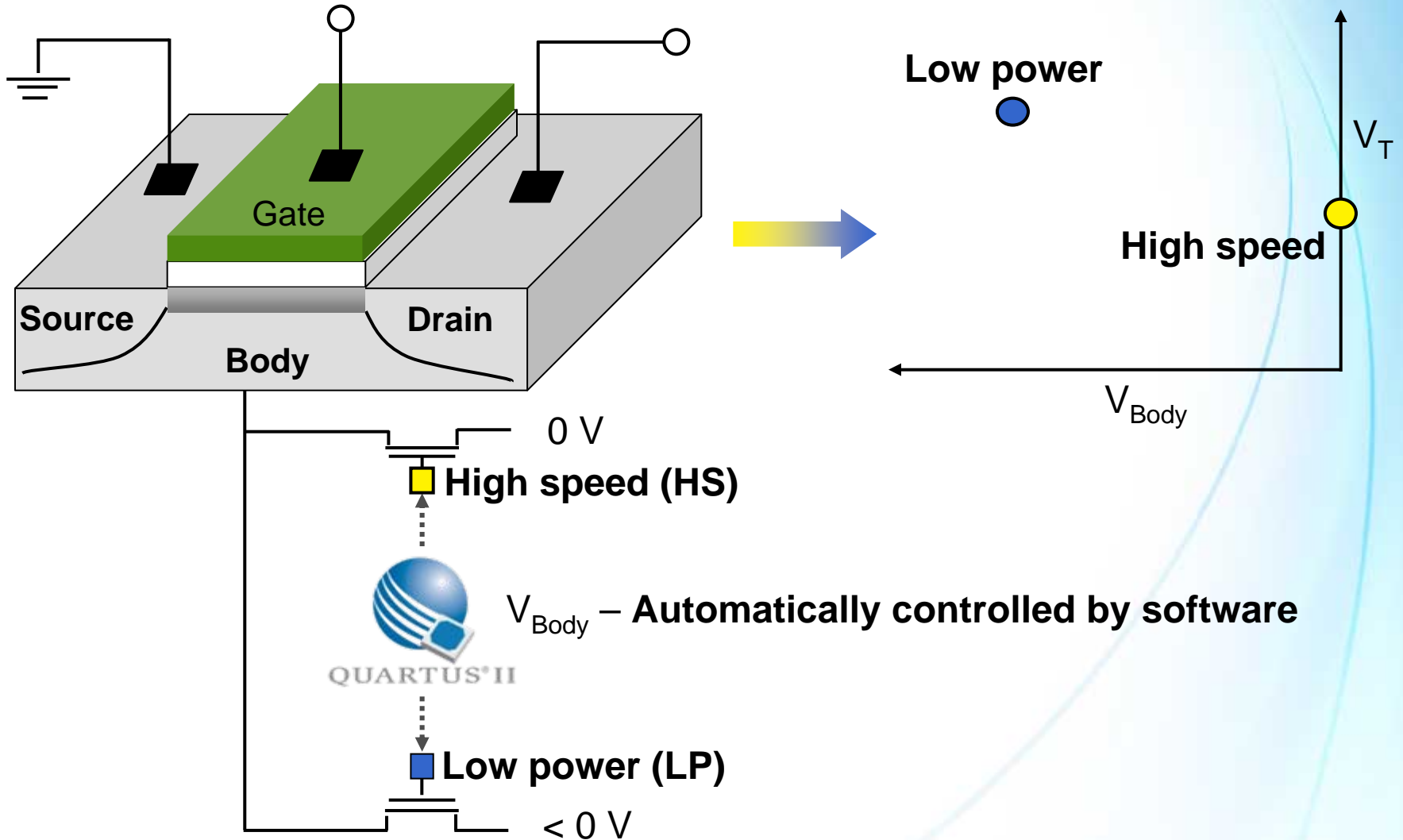
# Design-Specific Power Optimization

- Only a small fraction of logic is performance critical

## Slack Histogram

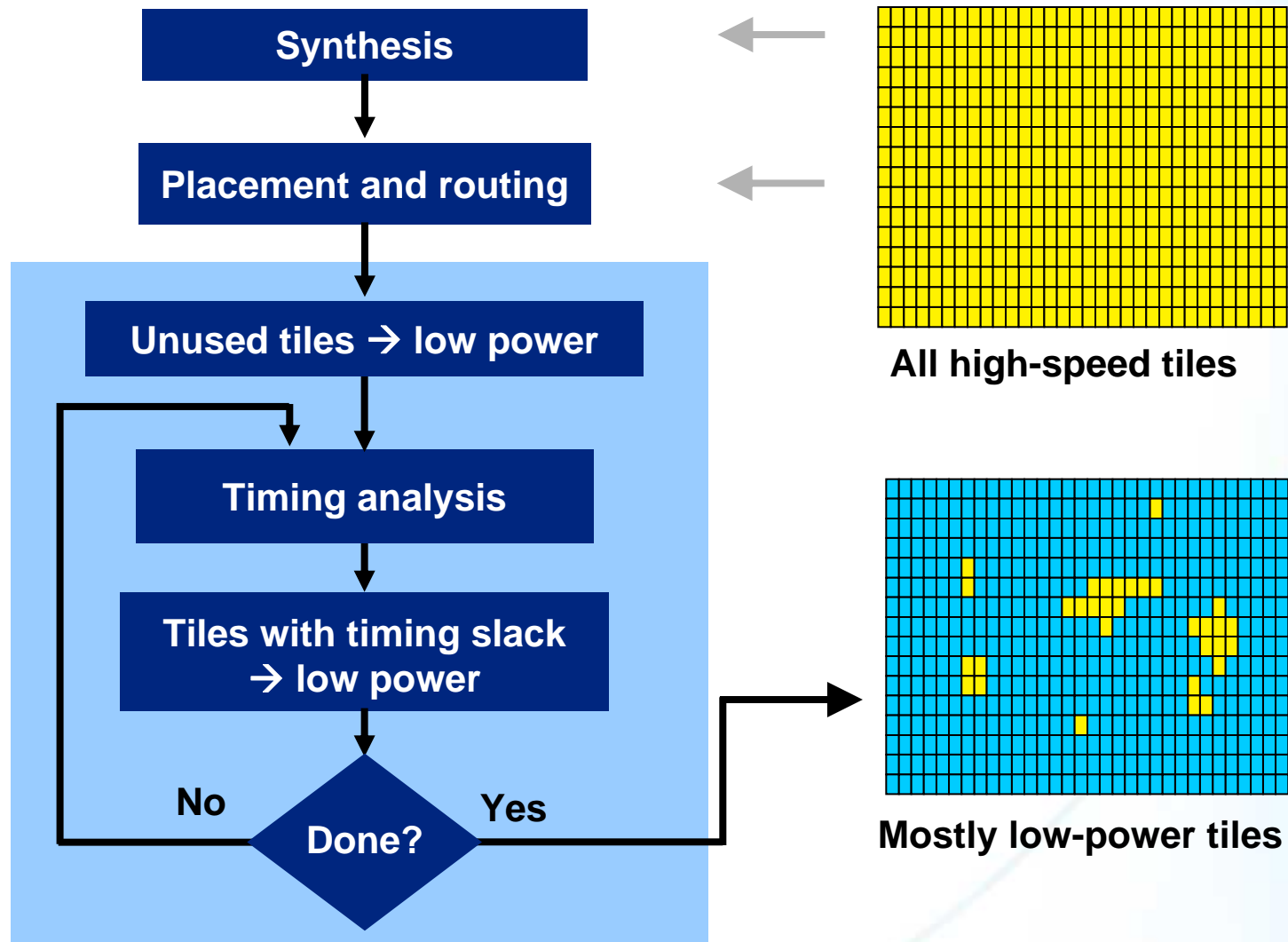


# Programmable Speed vs. Leakage



Note: A simple “model” showing Programmable Power Technology. Actual implementation varies and is patented.

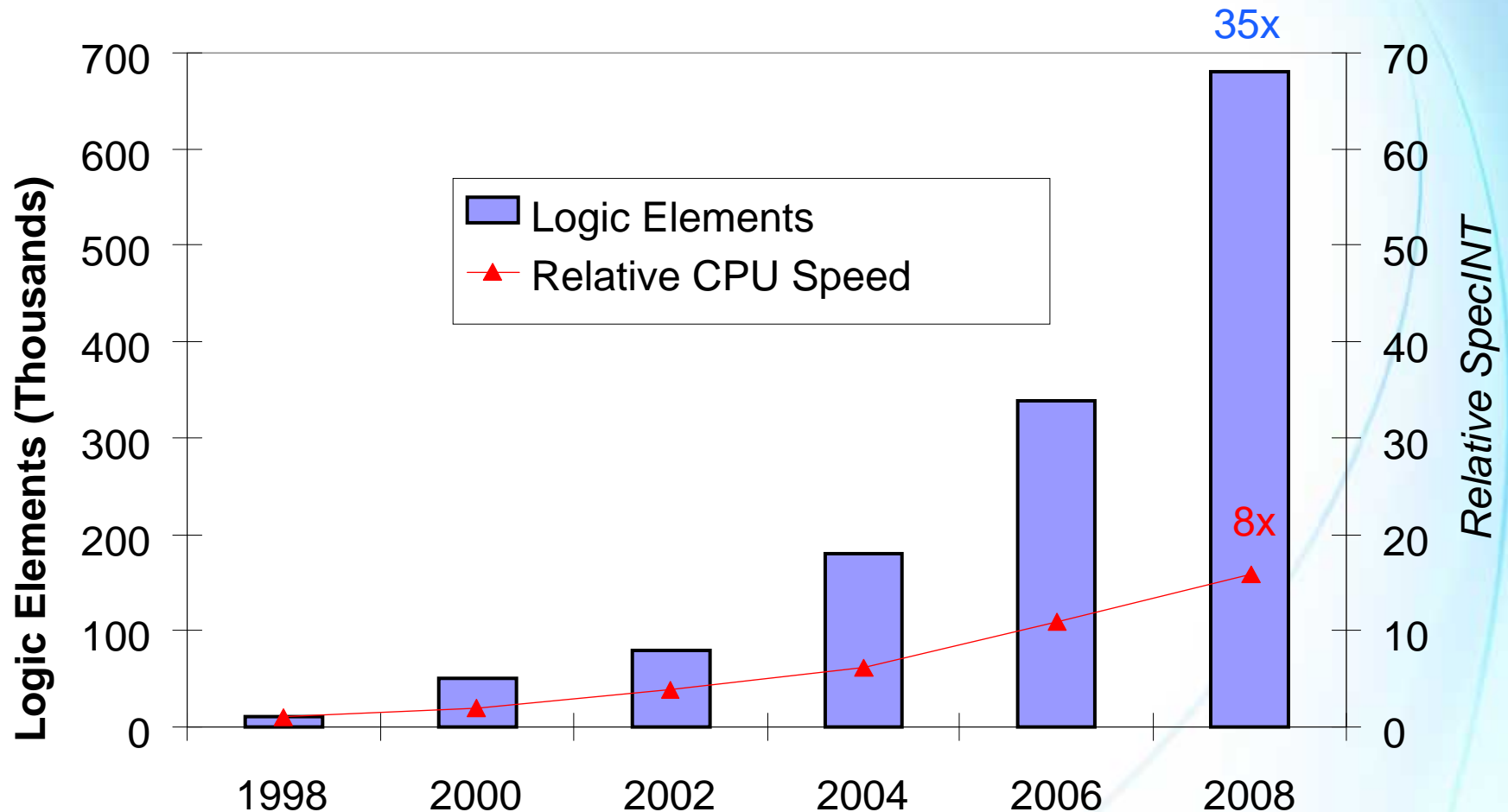
# Automated by Quartus II



# Designer Productivity

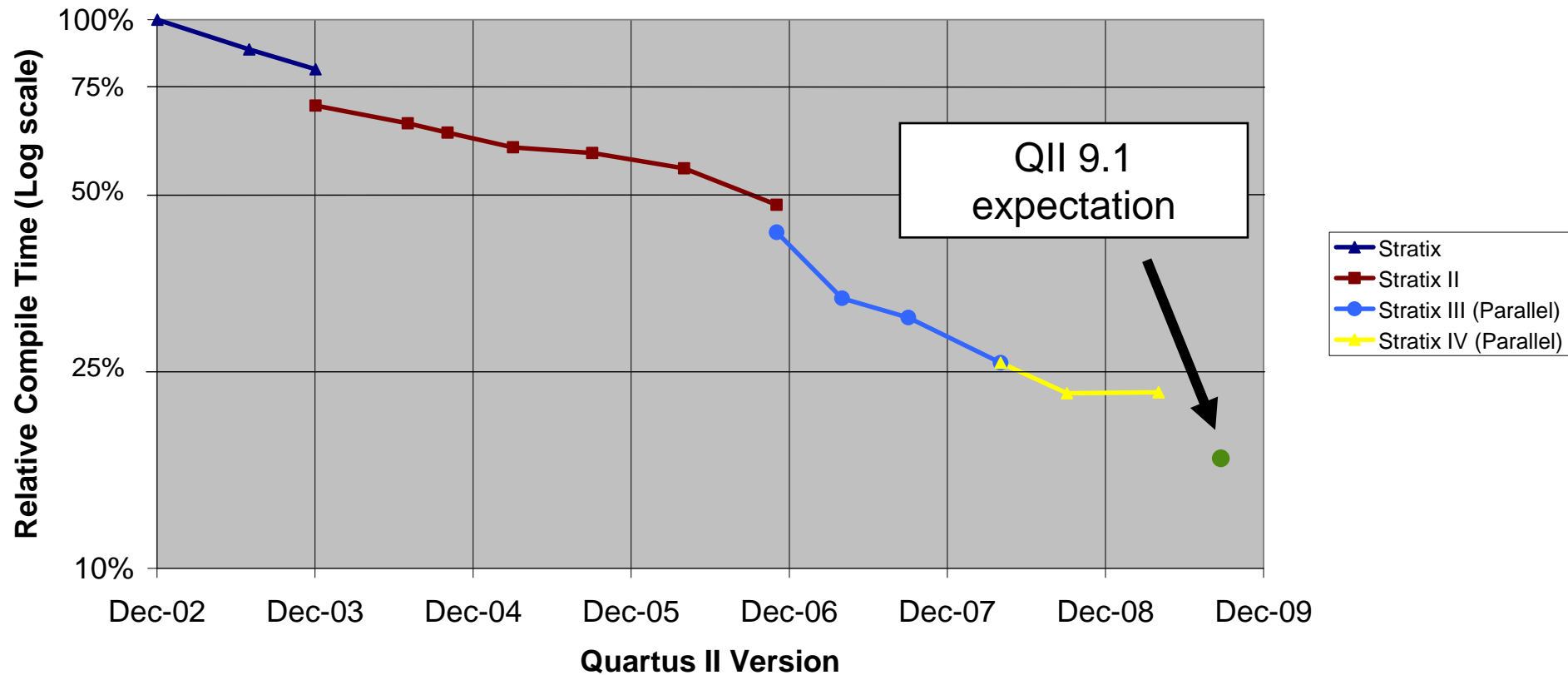
- When FPGA density doubles
  - CAD problem size doubles
  - FPGA user needs to create 2X the logic
  - But computer speed is not increasing as quickly
    - Need faster FPGA CAD algorithms!
    - Need better design flows (higher level)

# The Compile Time Challenge

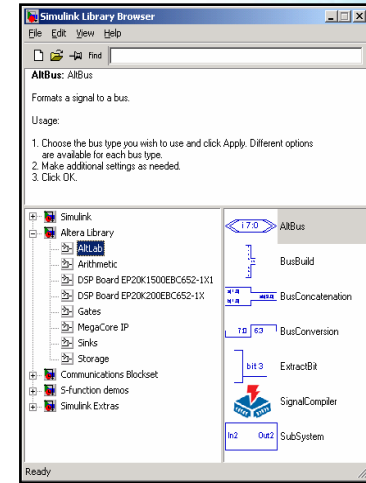
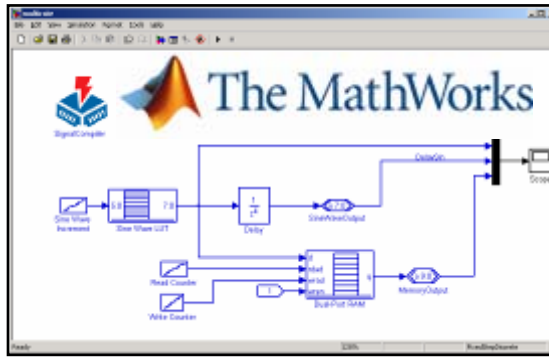
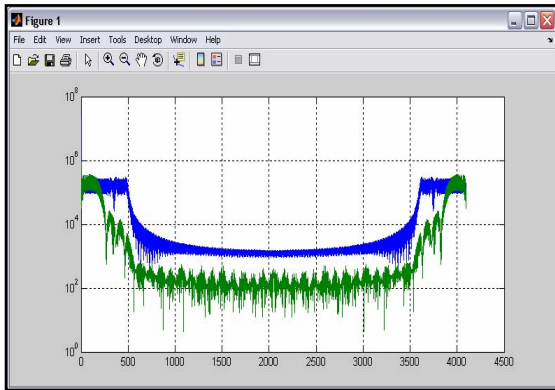


# Improvements More than Bridge the Gap

Quartus II Compilation Time History  
(Relative time for a fixed design, on a fixed CPU)



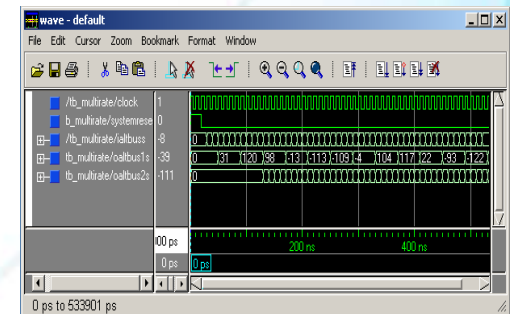
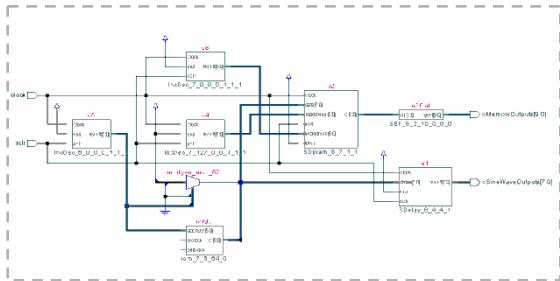
# DSP Builder Design Flow



**Matlab/Simulink domain  
(System simulation and verification)**



**HDL/hardware domain  
(Hardware implementation/RTL simulation)**



# Higher-Level Languages to HW

- Need better results from tools like
  - Catapult C
  - Altera C2H
  - Impulse C
  - AutoPilot
- Plus novel debug tools
- Plus good incremental design technology

# Summary

## ■ Scaling favours the programmable

- FPGAs
- Processors
- Can ASICs embed enough programmability?

## ■ Challenges

1. Architecture: fabric and configurable hard blocks
2. I/O bandwidth
3. Device modeling
4. Power & signal integrity
5. Keeping designers productive: compile time, new design & debug tools

**Thank You**

**Stratix IV GX  
2.5 billion transistors**

