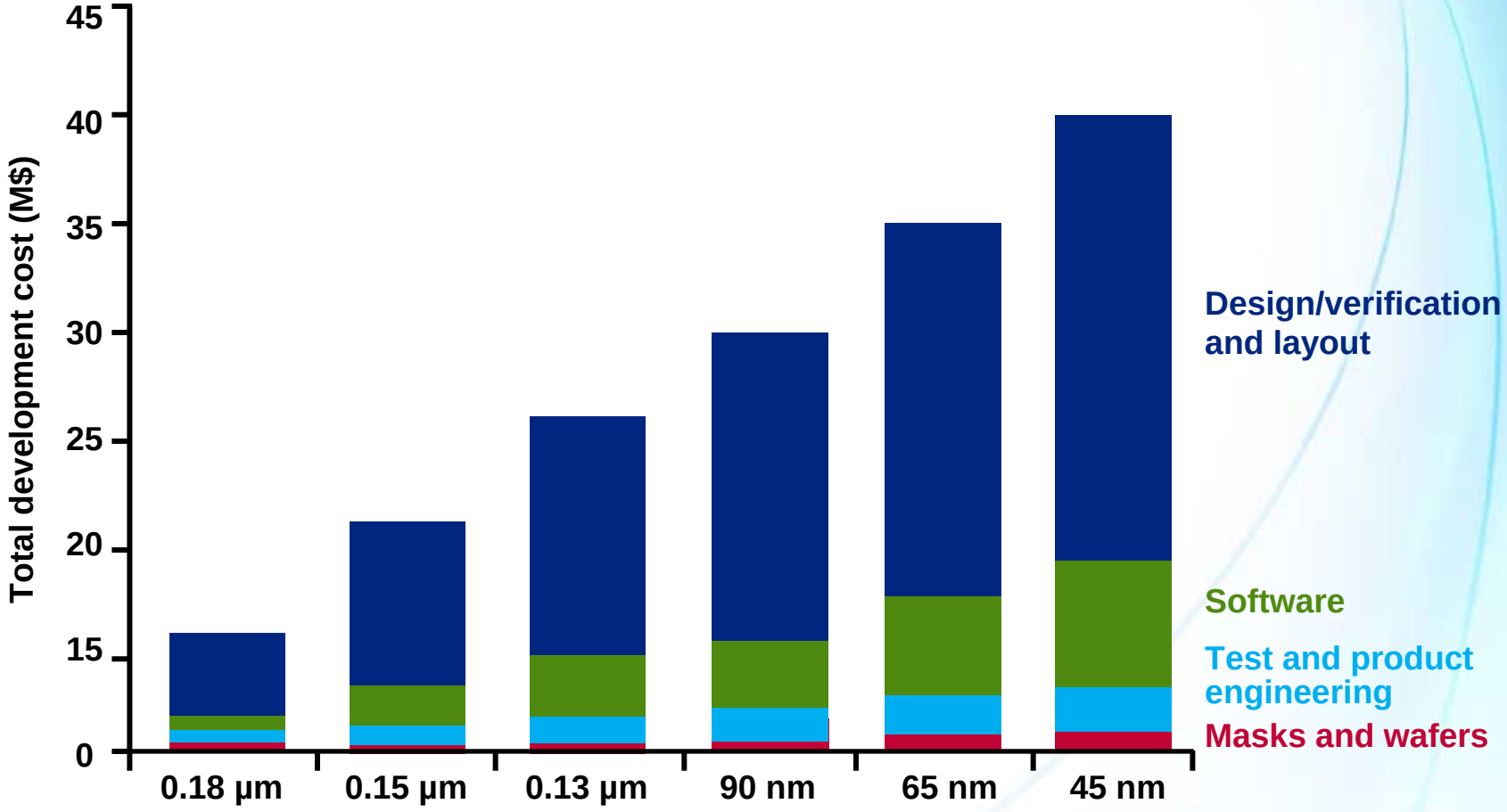
Development of Semiconductor Industry & Altera Product

Eric Law
FAE Director, Asia Pacific

State of the Semiconductor Industry

Rapidly Rising Custom Logic Development Cost



Source: Gartner Dataquest & Altera Estimates

Return on Investment Analysis

ASIC/ASSP (90nm) Development cost **$30M**

20% of revenue on R&D

Revenue target **$150M**

10% Market share

Market size ***$1.5B***

Justification of ASIC/ASSP development requires $1B+ market opportunity

ASIC % Design Starts by Technology

Integration, lower cost, performance ↑

Process node	2002 %	2003 %	2004 %	2005 %	2006 %	2007 %	2008 %	2009 %	2010 %	2011 %	Dev. Costs $M
0.022 µm	0	0	0	0	0	0	0	0	0	0	110
0.032 µm	0	0	0	0	0	0	0	1	ALTERA.	ALTERA.	80
0.045 µm	0	0	0	0	0	1	ALTERA.	ALTERA.	6	7	60
0.65 µm	0	0	0	1	2	ALTERA.	8	10	13	15	55
0.09 µm	0	1	8	ALTERA.	ALTERA.	23	23	24	24	24	30
0.13 µm	ALTERA.	ALTERA.	ALTERA.	29	29	27	27	25	24	24	20
0.18 µm	38	27	23	20	17	14	12	10	10	8	13
0.25 µm	16	15	12	12	11	9	9	8	7	6	5
0.35 µm	21	16	12	12	11	10	8	8	6	5	3
0.5 µm	5	4	3	7	7	6	6	5	4	4	2
L>0.5 µm	1	1	0	6	6	6	5	5	5	5	<1
Total	100	100	100	100	100	100	100	100	100	100	

Increased risks and development cost ↑

#1 ASIC design technology

ALTERA. #1 PLD design technology

Source: Altera & Gartner Nov 07

Semiconductor Industry Reaction to Rising Costs

- Move engineering base to lower cost locations
  - One time benefit, only delays inevitable
  - Rising costs in many low-cost locations quickly offset benefits
- Utilize older process nodes for lower up front costs
  - No production cost decreases possible on mature technology
- Fewer products developed for low to medium volume infrastructure markets
- Fewer semiconductor start-ups funded
  - Poor return on investment for venture capitalists
  - Most systems companies favor large companies for approved supplier list

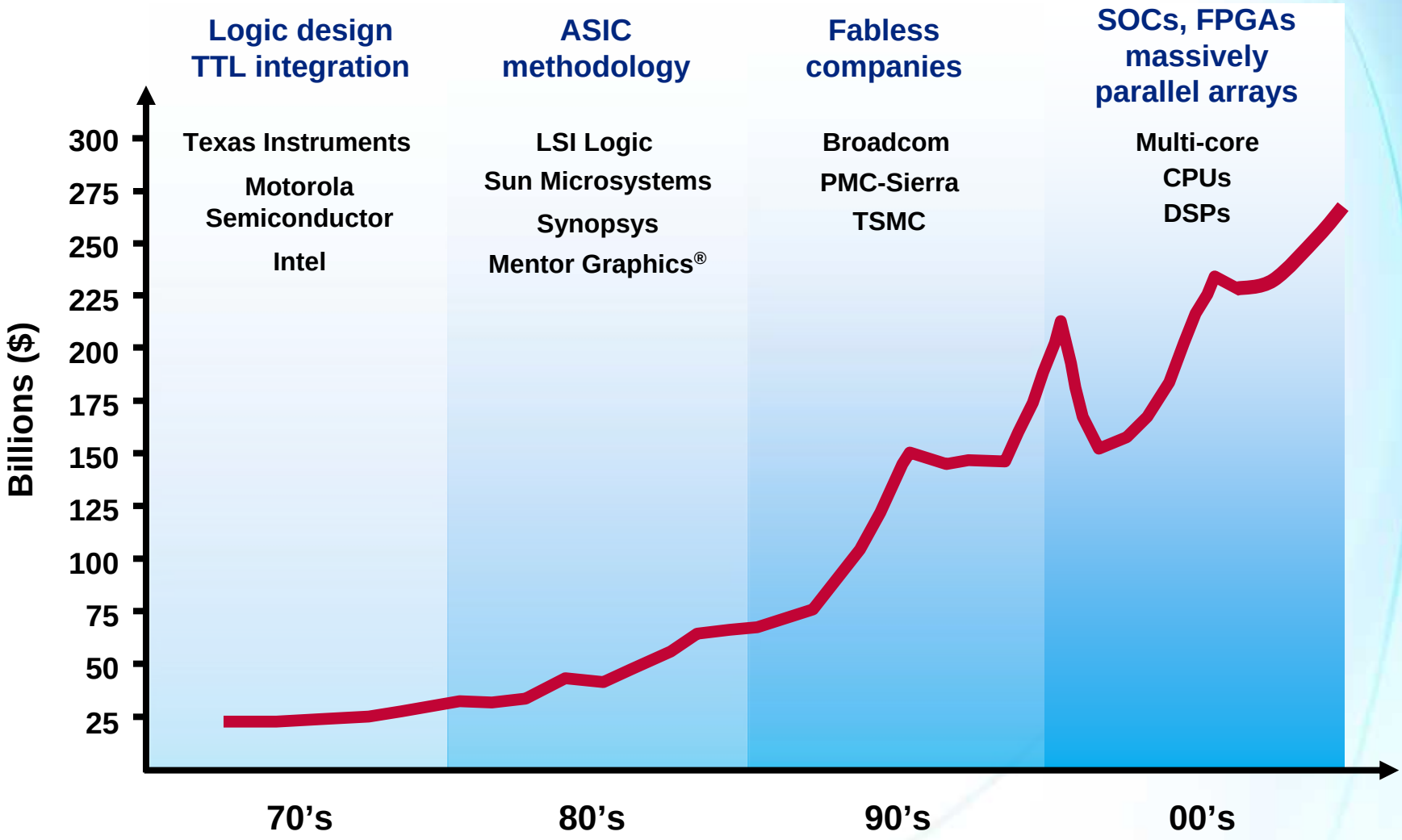
Changing Semiconductor Landscape

Rising Development Costs and Slowing Growth

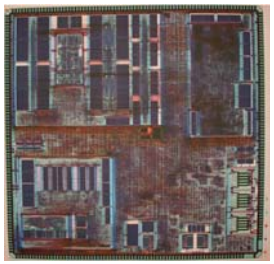
- Industry consolidation around product lines
  - Increase in market share makes R&D affordable
  - Two to three players per major product category
  - Consolidation will effect product roadmaps and existing product support
- Successful companies offer more than just devices
  - Calls for an earlier and different engagement model – view as an extension of customer's R&D
- Moore's law favors programmable products
  - Leverage large customer base for single part to provide ROI

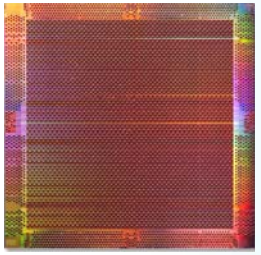
Programmable Solutions: A Continued Evolution

This Decade: Programmable Solutions



Programmable Solutions: 1985-2002



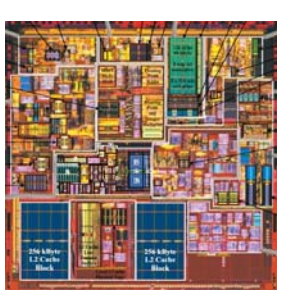


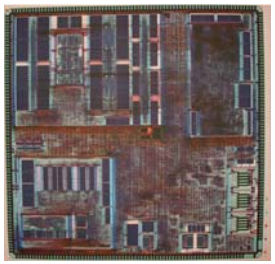
CPUs DSPs FPGAs

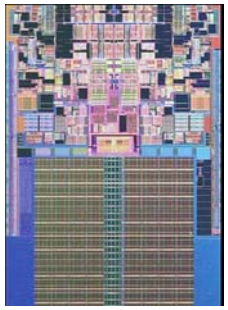
Single cores

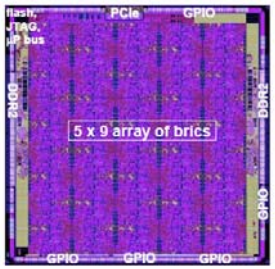
Fine-grained arrays

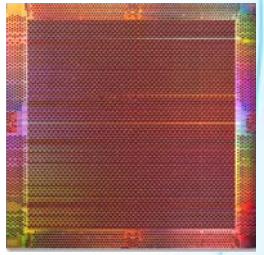
Programmable Solutions: 2002-20XX











CPUs | DSPs | Multi-cores | Arrays | FPGAs

Single cores

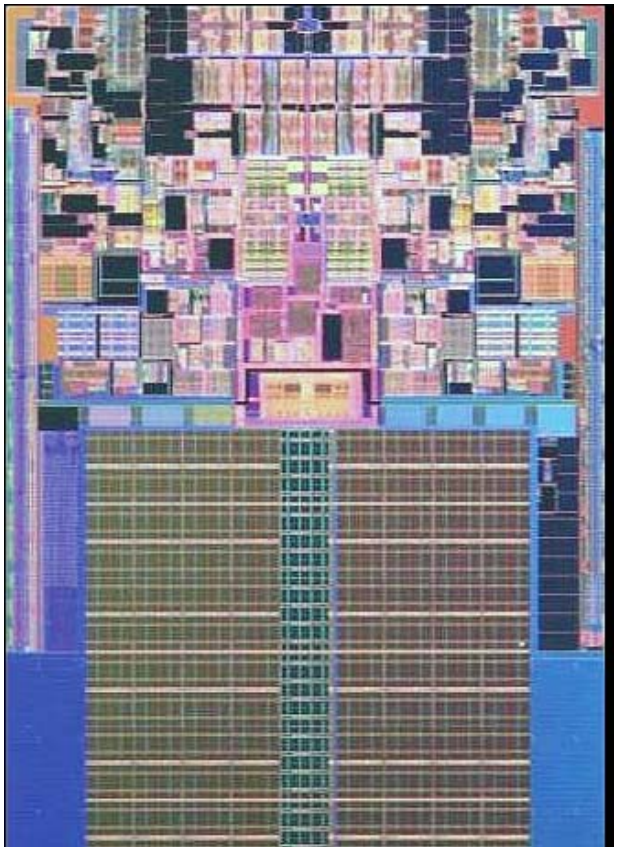
Multi-cores Coarse-grained CPUs and DSPs

Coarse-grained massively parallel processor arrays

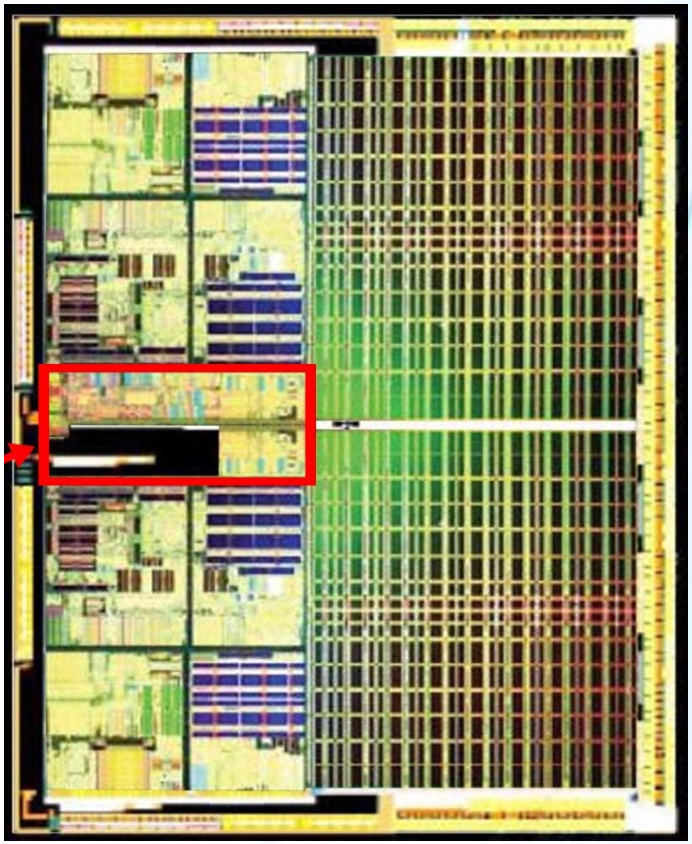
Fine-grained massively parallel arrays with embedded hard IP blocks

Broadly Used Dual-Core Processors

Intel's Penryn

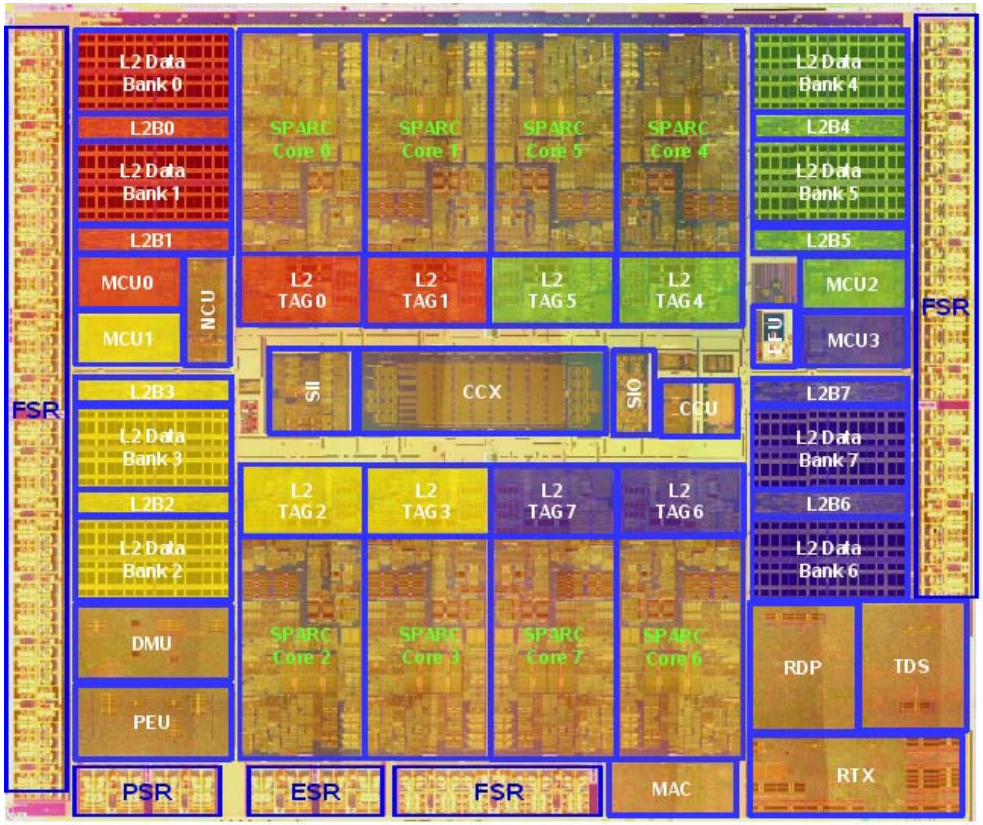


Dual-core AMD64



Sun's UltraSPARC T2

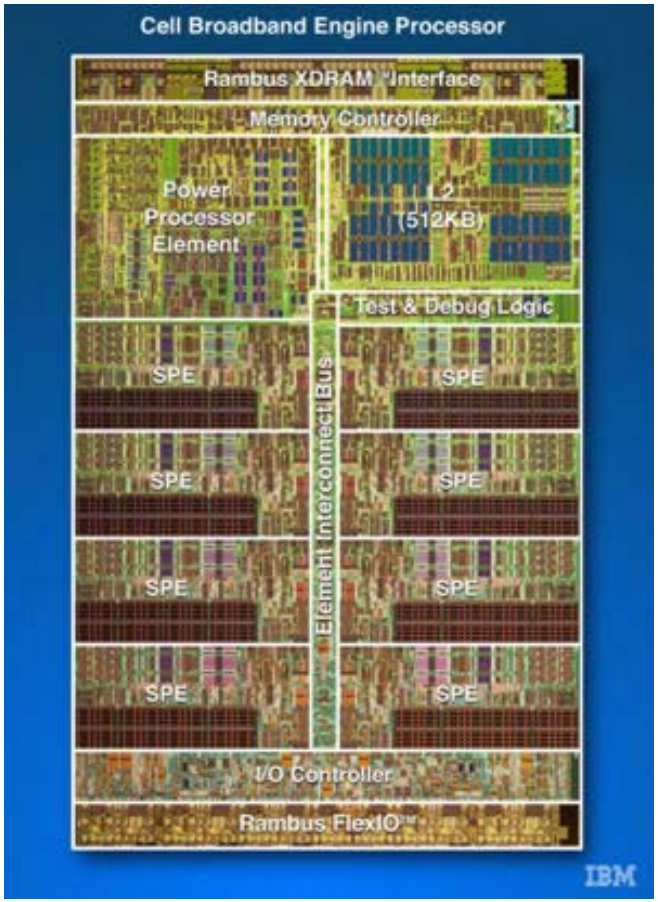
- Eight cores, eight threads per core
- Sixteen-core processor due in 2008



Other Multi-Core Examples

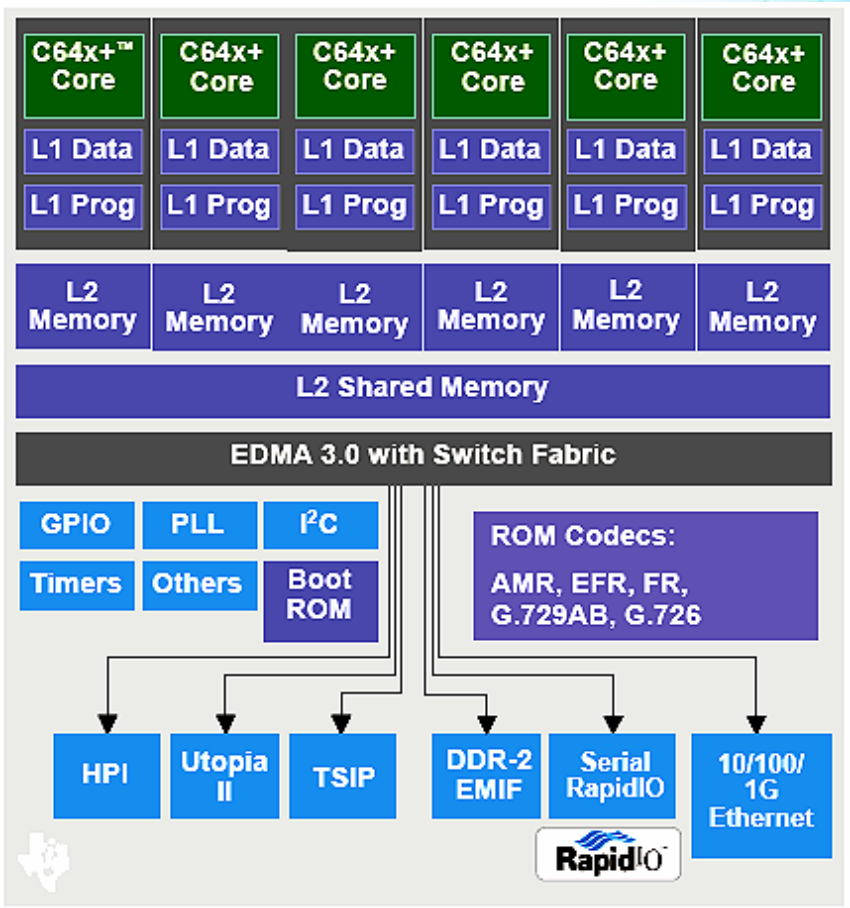
Cell BE

PPC + 8-core engine



Texas Instruments

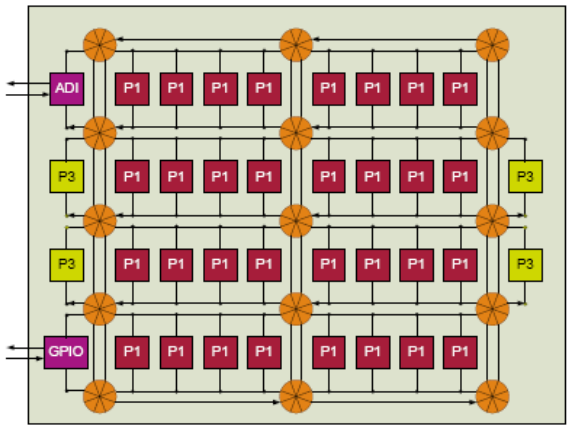
TNETV 3020



Processor Arrays

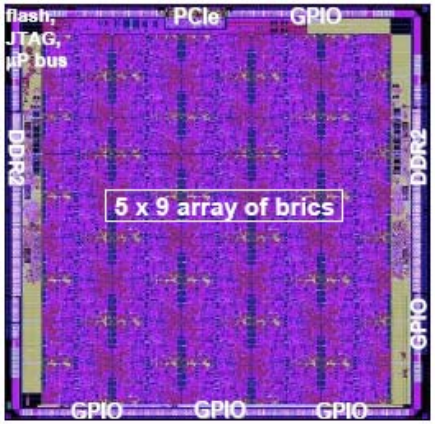
picoChip

248 processors
Heterogeneous
Wireless applications



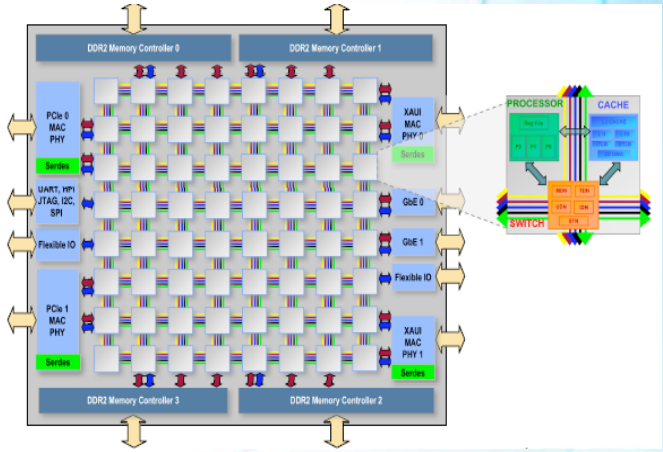
Ambric

360 processors
CSP programming model
Video applications



Tilera

64 tiles
2D Mesh
Video applications

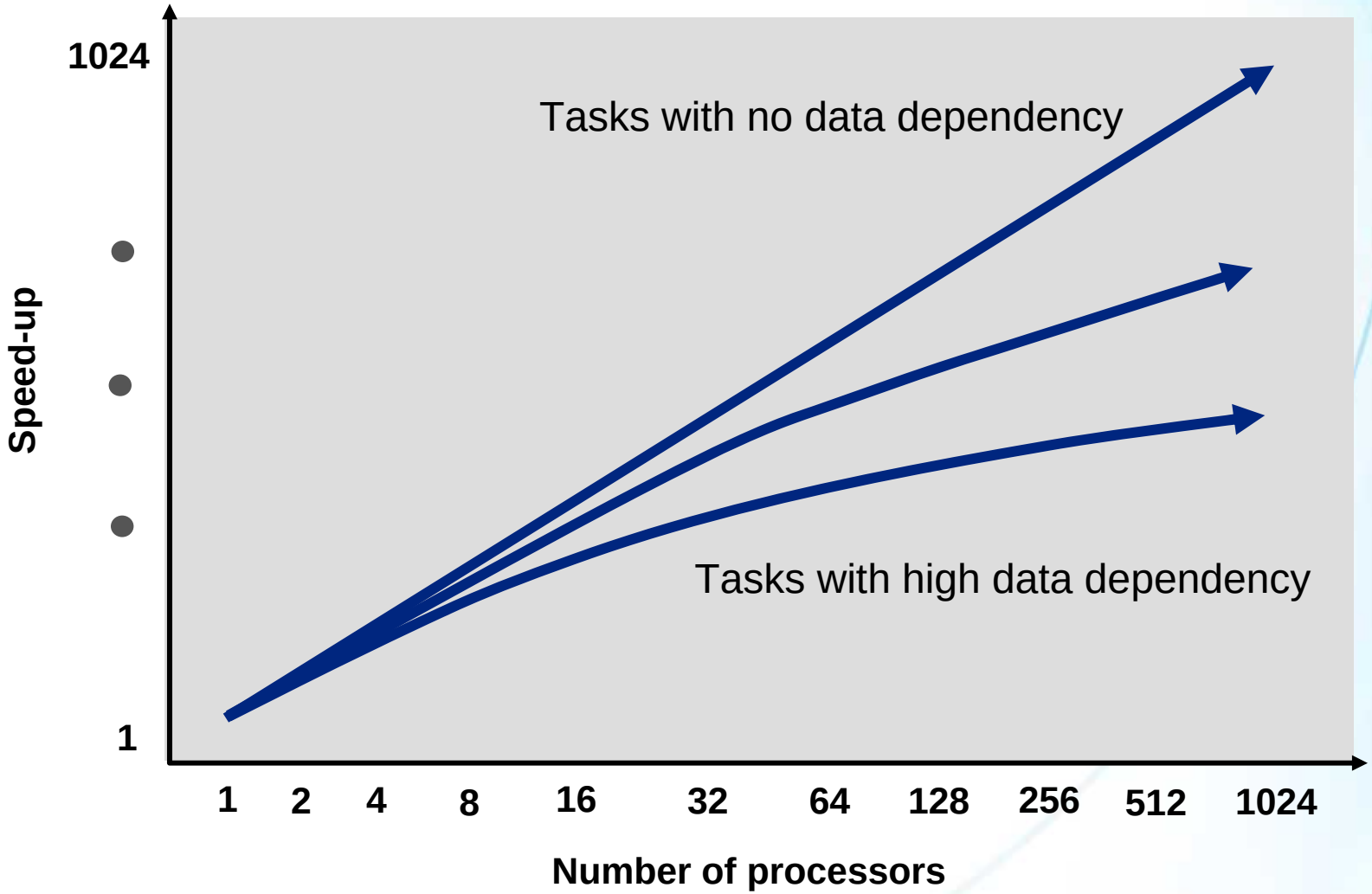


Parallel Programming Challenge

- If all processors become multi-core,
- If all computers become massively parallel,
- How will all programmers write and debug parallel programs?
- The hardware guys are done, now it is just software…

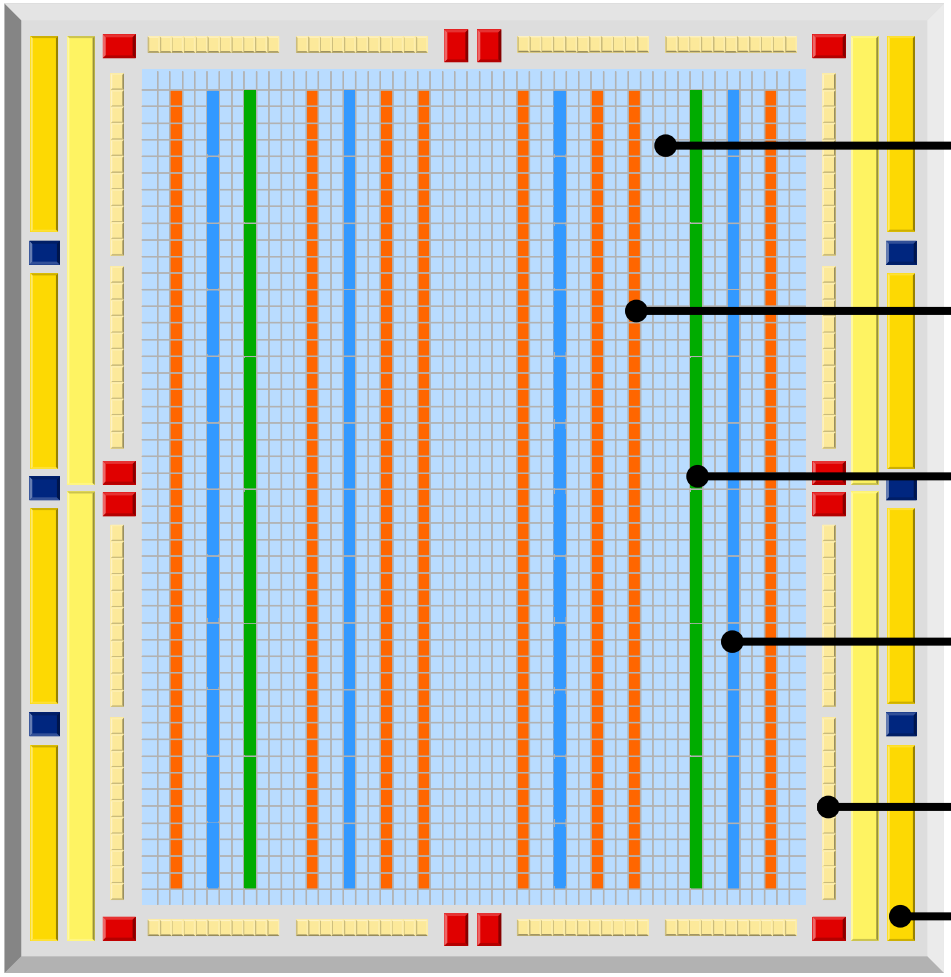
Courtesy: RapidMind

Multi-Core Parallel Speed-Up: A Realistic View



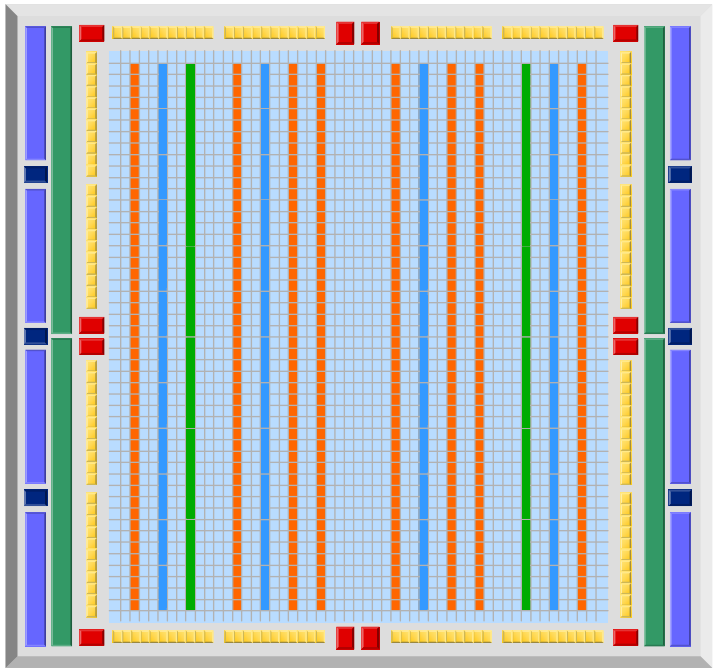
Modern FPGAs: Massively Parallel

Stratix® IV device

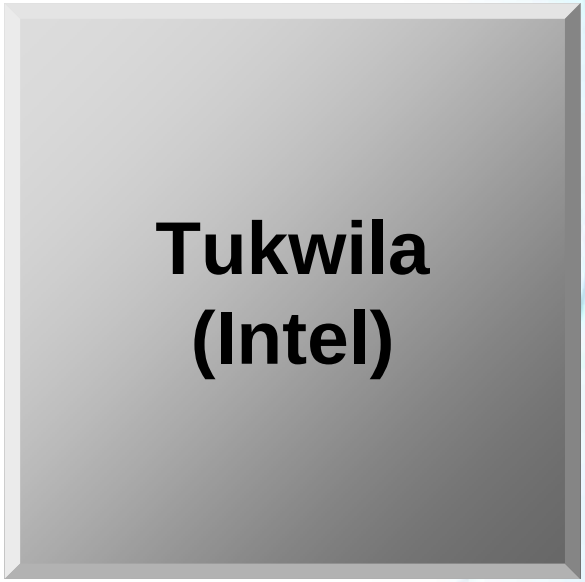


- 680,000 logic elements
- 1,500 9-kbit memory blocks
- 64 144-k bits memory blocks
- 1,300 DSP blocks
- 1,100 programmable I/O blocks
- 48 transceivers

Low-Power, High-Performance Chips



Stratix IV EP4SGX530 FPGA
2.5 billion transistors
10 to 20 W



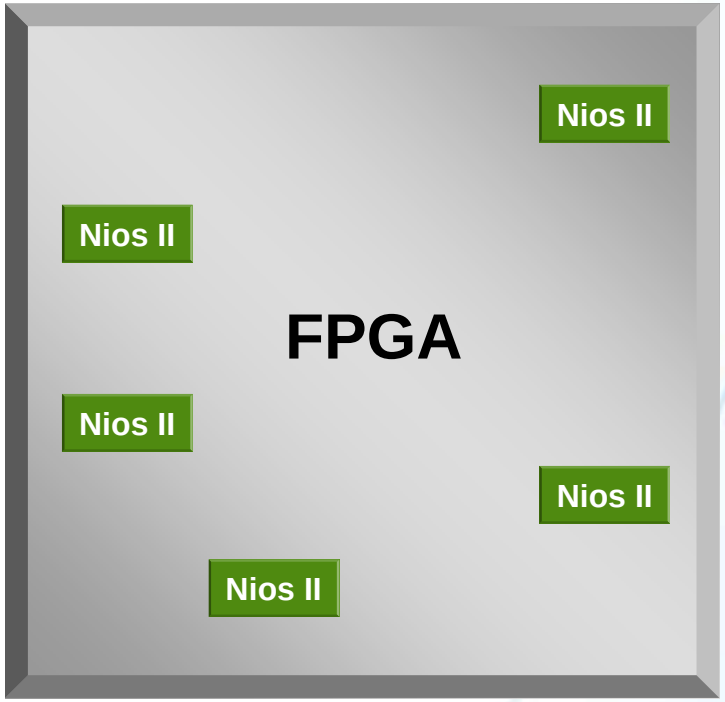
Intel Tukwila Device
2.05 billion transistors
130 to 170 W

Embedded Soft CPUs Are Affordable

Small Cyclone® III
FPGA 10,000 LEs

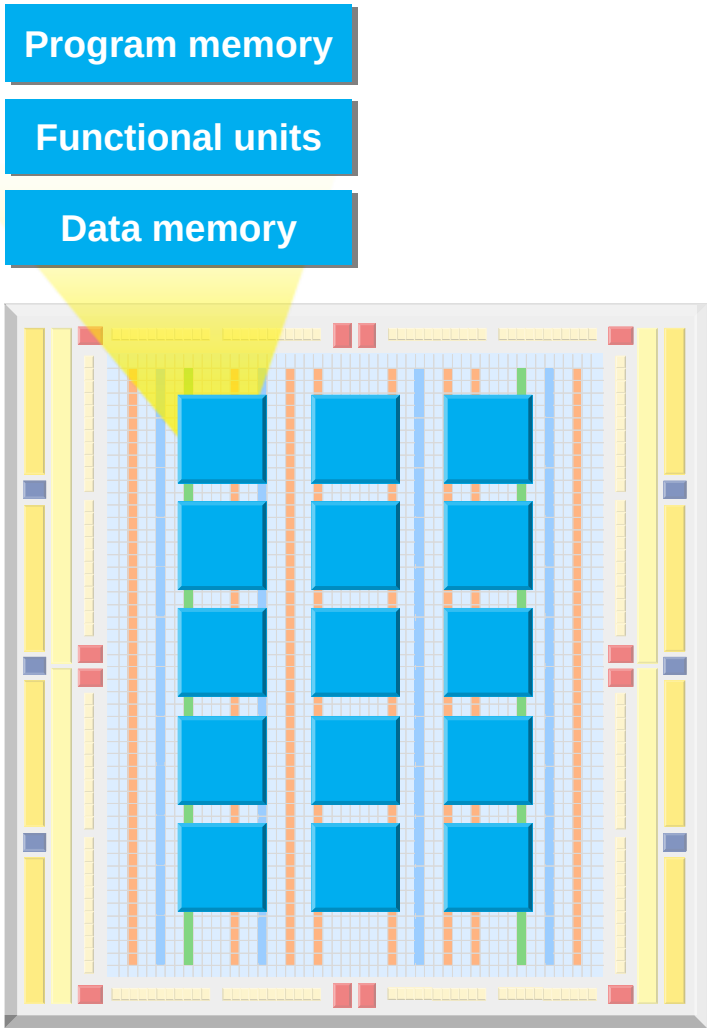
600 Logic Elements (LEs)
5% of FPGA
Nios® II/e "Economy"

Largest Stratix IV FPGA
680,000 LEs



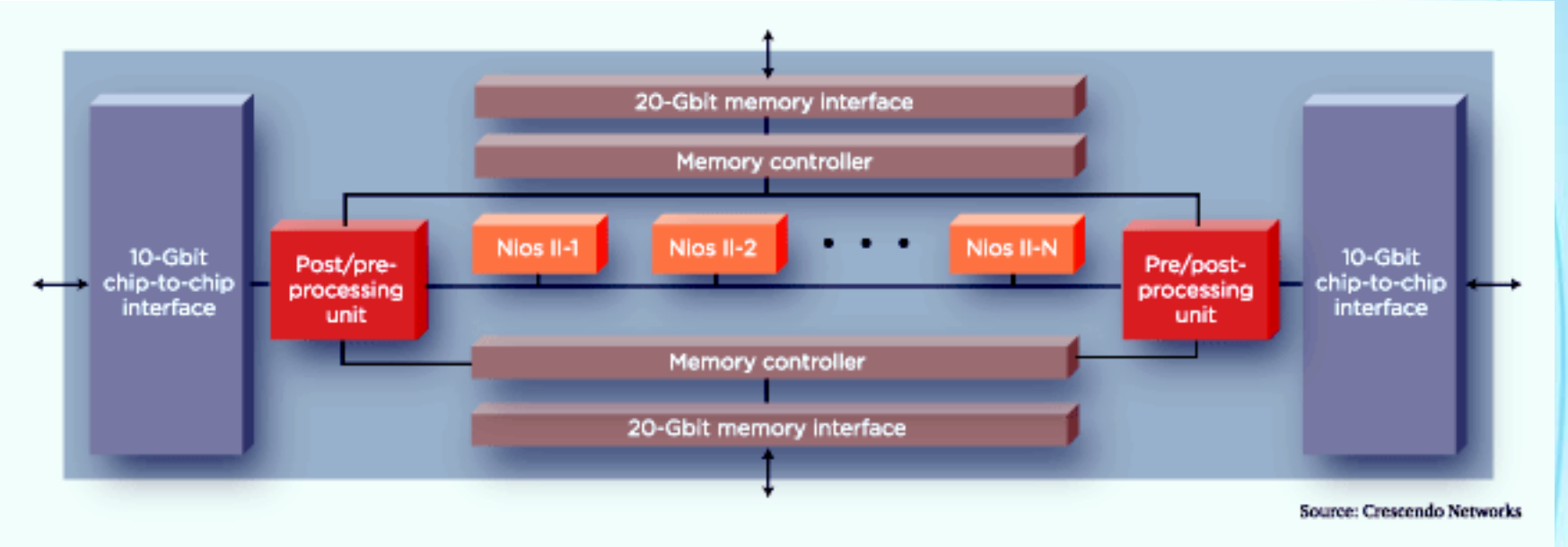
1,800 LEs, 0.3% of FPGA
Nios II/f "Fast"

Multi-Core Systems on FPGAs



- Many programmable coarse-grained processors
  - Soft blocks in FPGA fabric
  - Each with local memory
  - Homogeneous or
  - Heterogeneous
- Programmable interconnect
- Software defined
  - C Compilation to Microcode

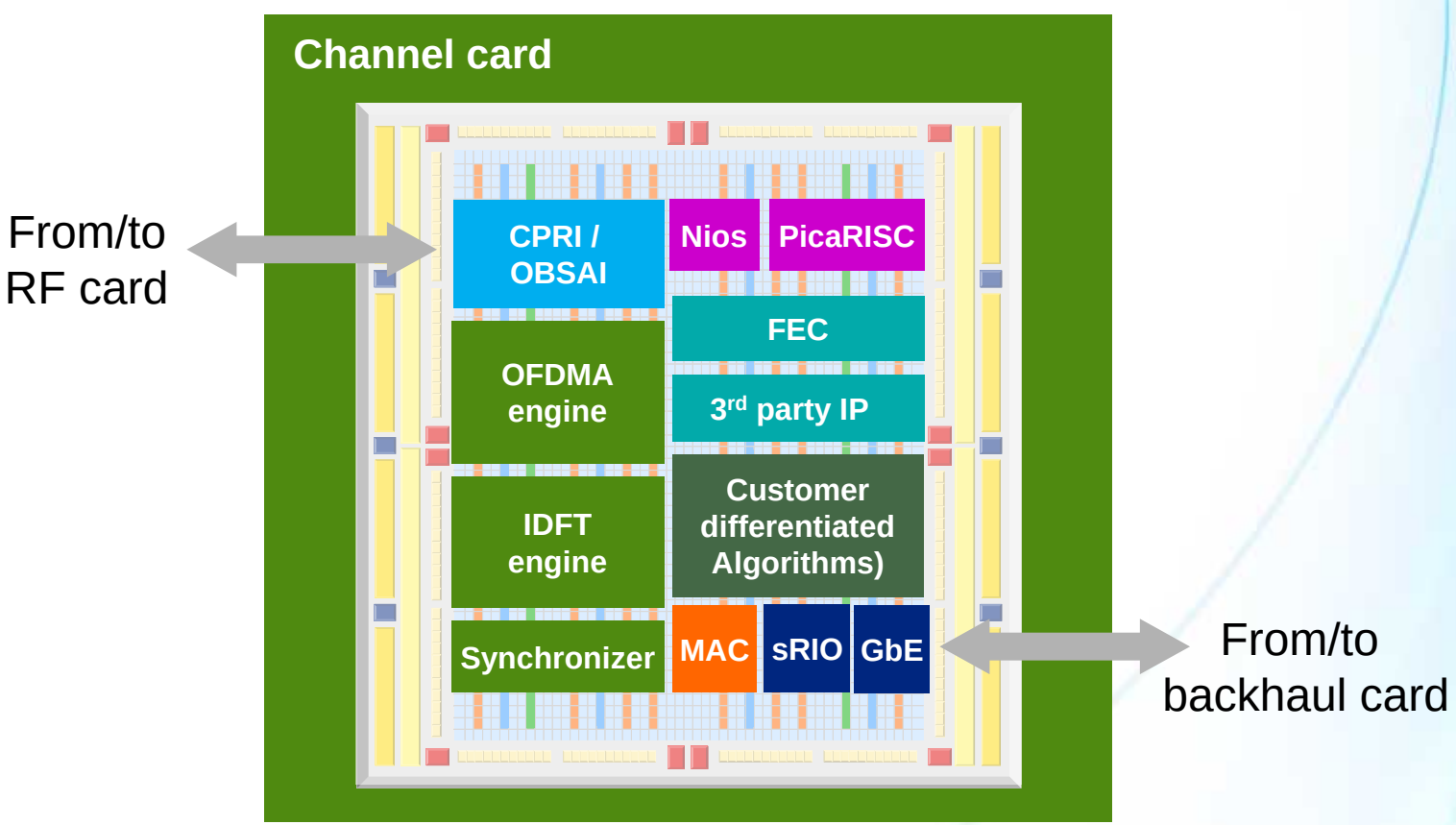
Multi-Cores on FPGAs: Crescendo Networks



- A programmable eight-processor architecture
- Using embedded Nios II soft processor
- On a single Stratix II chip
- For layer 4/7 applications

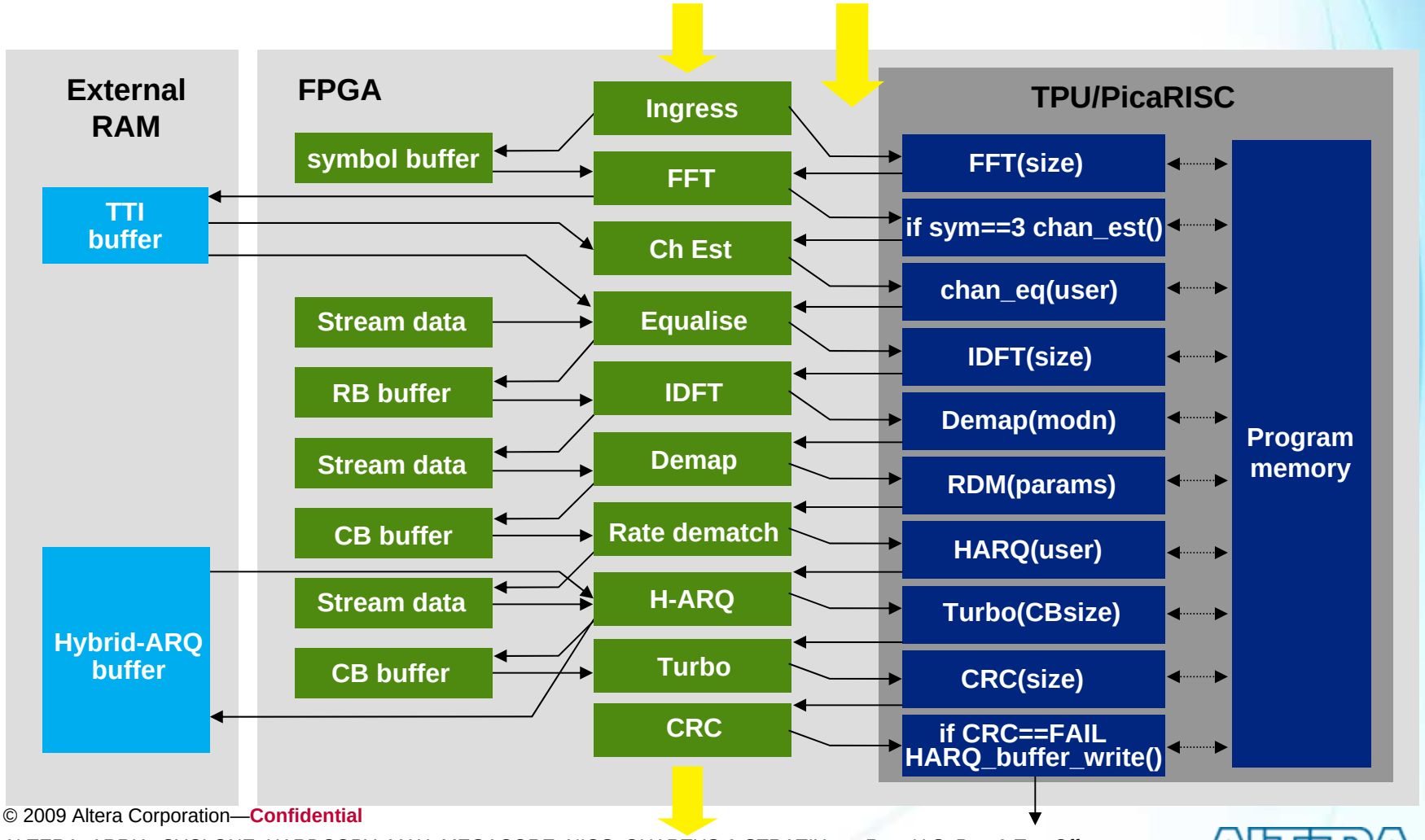
Application-Customized Multi-Cores on FPGAs

- Wireless BTS channel card architectural template



Embedded Software View

- Example: Wireless base-station channel card

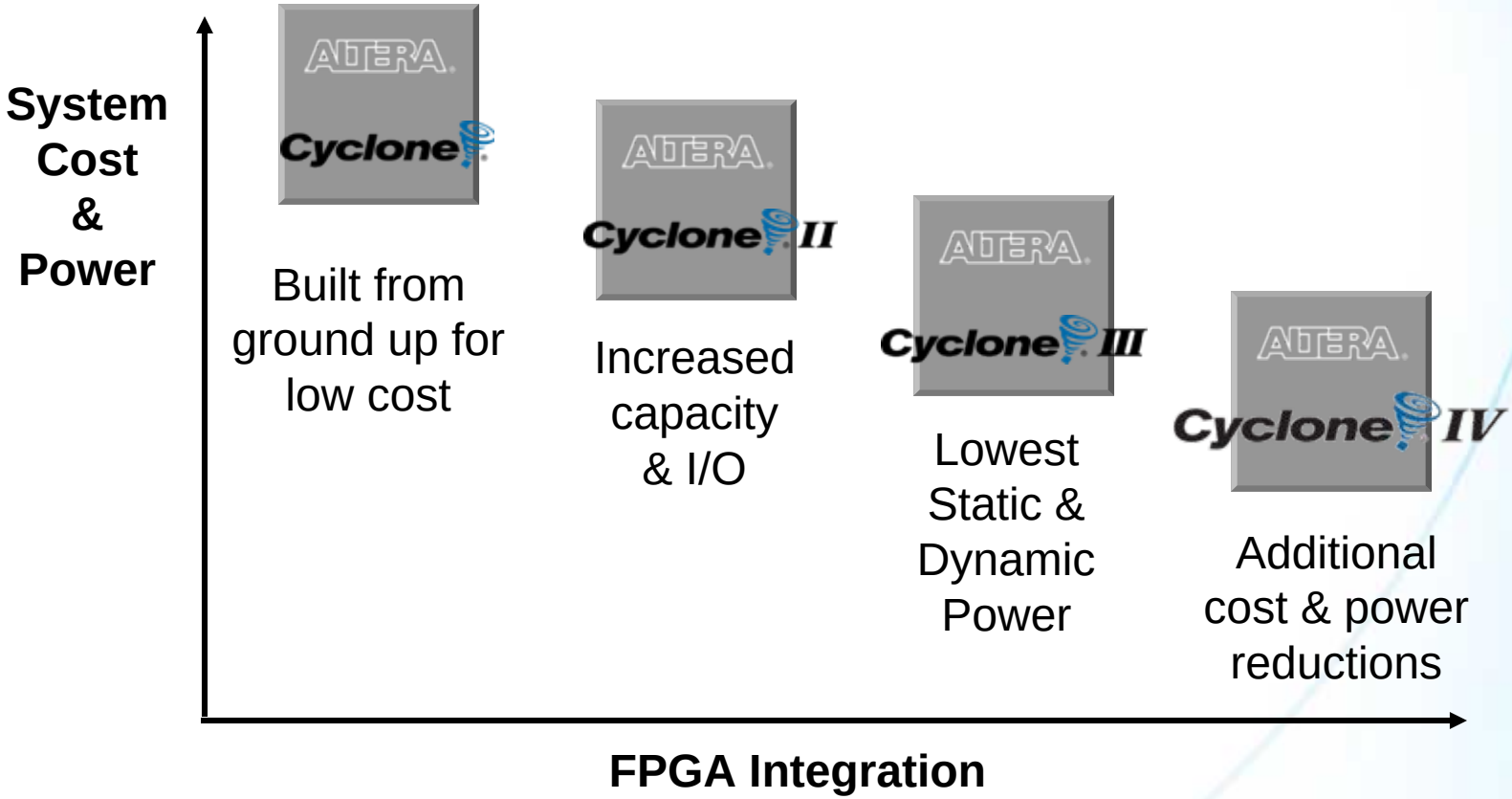


Summary

- A new era focused on reducing power
  - From handheld applications to infrastructure applications
- The era of programmable solutions
  - All processors will be multi-core
- The era of innovation
  - Massively parallel programmable solutions
- FPGA architecture enables lower power, higher performance solutions

Introducing Cyclone IV FPGAs

Integration Lowers Cost & Power



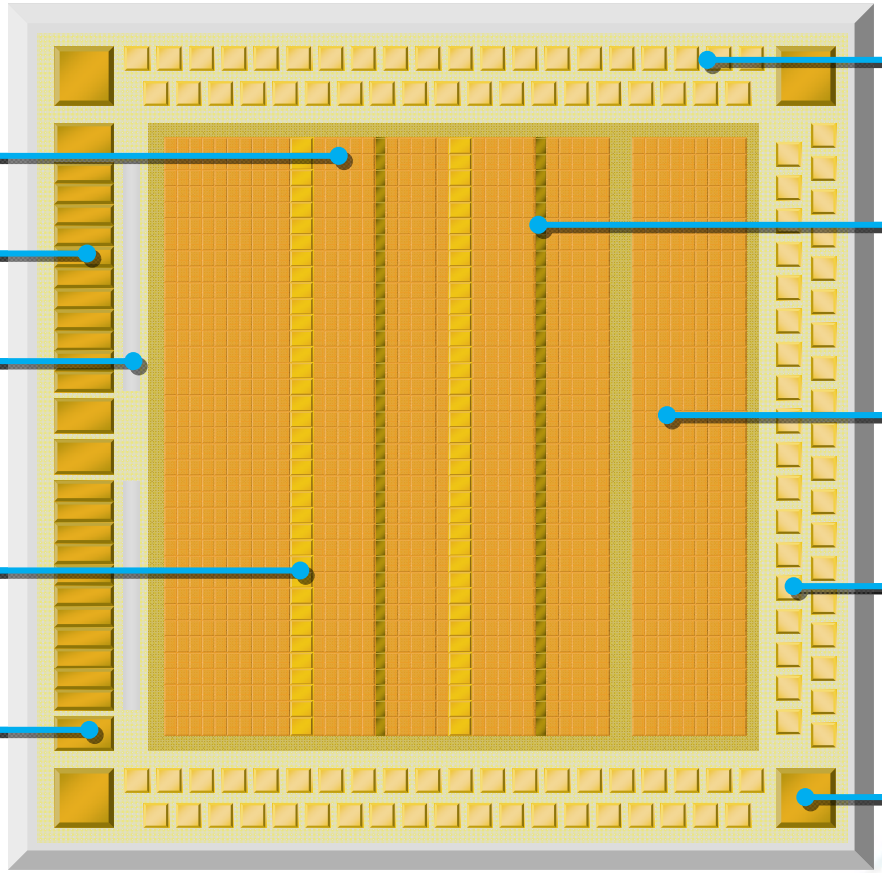
Introducing Cyclone IV FPGAs

- **Logic only (E) & transceiver (GX) variants**
- **Lowest system cost**
  - Hard IP blocks: transceivers, PCIe, DSP
  - Mainstream 3G serial protocols
  - 2 power supplies
- **Lowest power**
  - Optimized low-power fabrication process
  - PCIe to GbE bridge for <1.5W
- **High functionality**
  - Up to 150K Logic Elements
  - Up to 6.5 Mb RAM, 360 Multipliers
  - Up to 8 integrated 3.125Gbps transceivers

Lowest cost, lowest power FPGAs with transceivers

Key Architectural Features

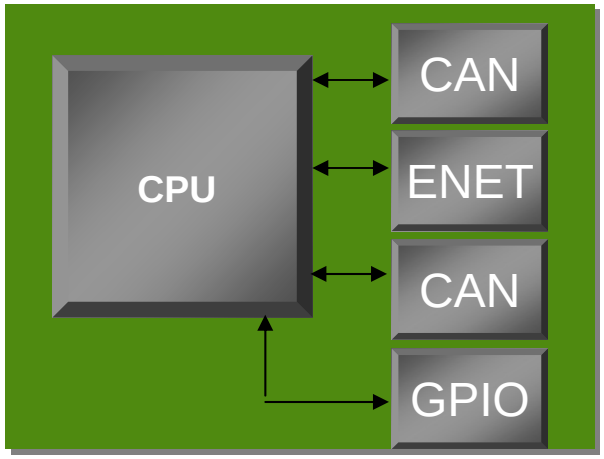
Same 4-LUT, M9K, Embedded Multipliers as Cyclone IIII FPGAs

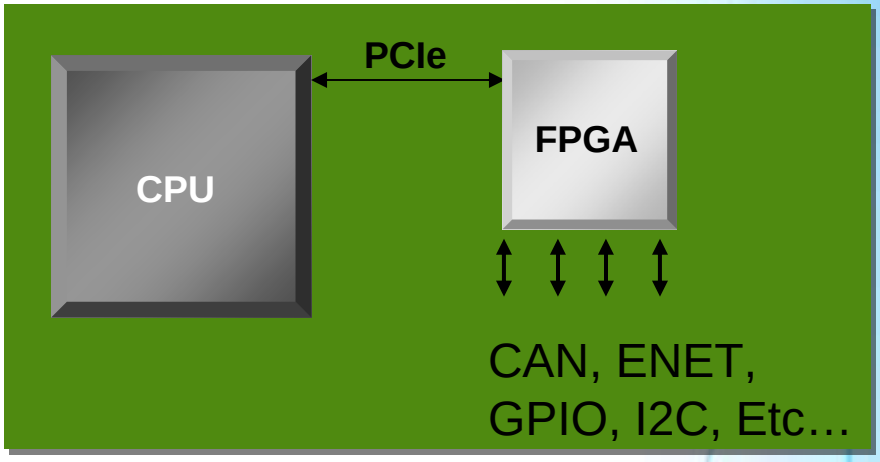


- Up to 150K LEs
- Up to 8 transceivers, up to 3.125 Gbps
- PCIe Hard IP block
- Up to 6-Mbit embedded memory
- Up to 4 MPLLs
- 400-Mbps external memory interfaces
- Up to 360 embedded multipliers
- 60-nm low-power process
- Up to 475 flexible user I/O pins
- Up to 4 PLLs

MPLL – Multi-Purpose Phase Locked Loop for transceivers

Bridging and IO Expansion





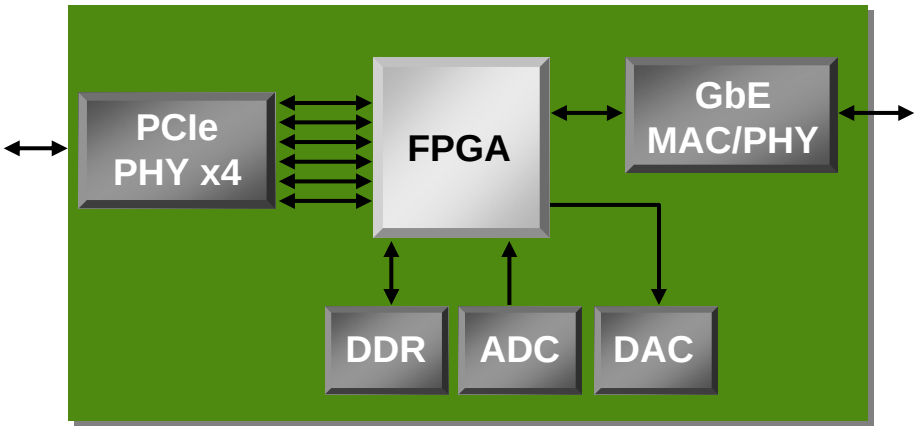
Next-generation challenges

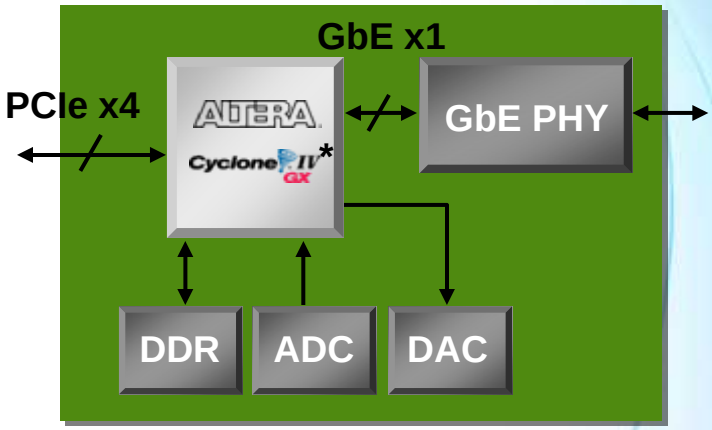
- Finding CPU with right mix of peripherals at right time
- Obsolesence risk
- Low cost, high bandwidth interface

Solution

- Reduce costs through FPGA integration and simplified PCB
- Simplified power management
- Differentiate product with custom peripheral mix
- Remove obsolescence risk

Lower System Costs Through Integration





PCIe PHY

PCIe in logic (~15K LEs)

GbE chipset

PCIe licensing fee

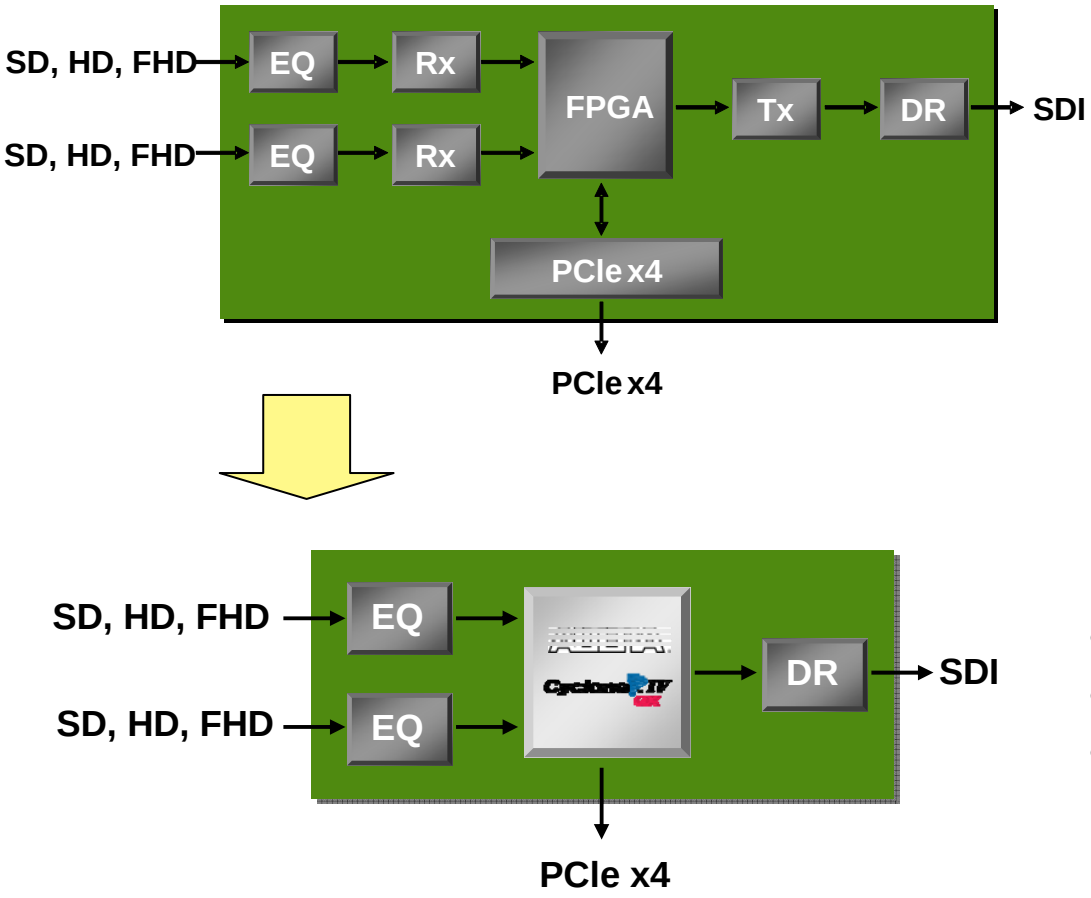
GbE PHY

GbE PHY not needed for chip-to-chip applications

Significant savings through integration

*** Requires only 2 power supplies**

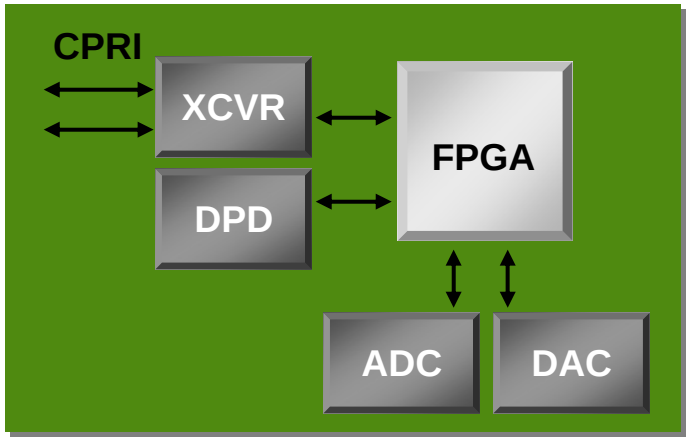
Lowest System Cost – Video Capture Card Example

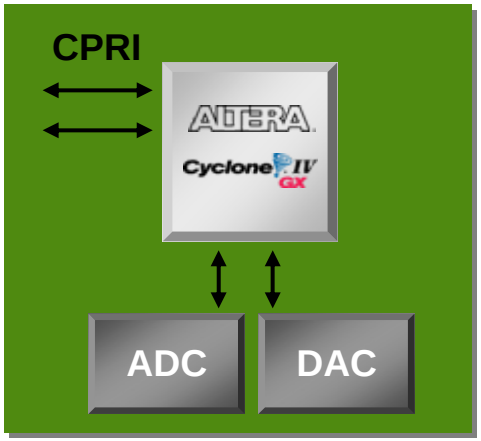


- Lower or no cost for ASSPs
- Cheaper PCB
- Smaller, lower cost FPGA

Save over 30% in system cost

Wireless Remote Radio Head Example





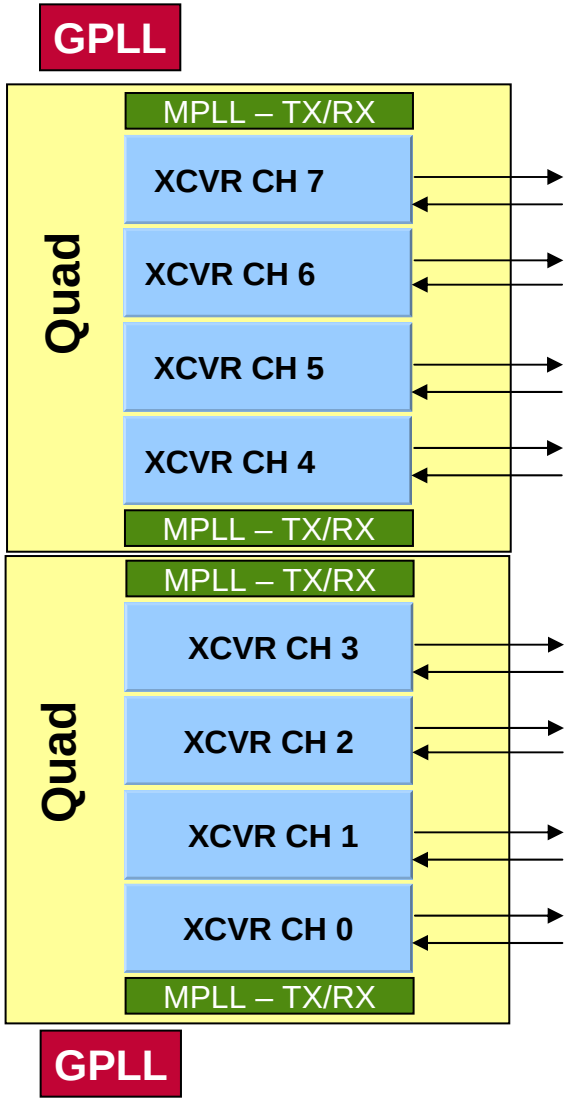
Next-generation challenges

- Reducing system costs
- Meeting power budgets
- Support for evolving standards and new functionality
- Time to market

Solution

- Reduce costs through FPGA integration and simplified PCB
- Simplified power management
- FPGA supports evolving air interface standards
- Get to market fast with pre-built reference designs and examples

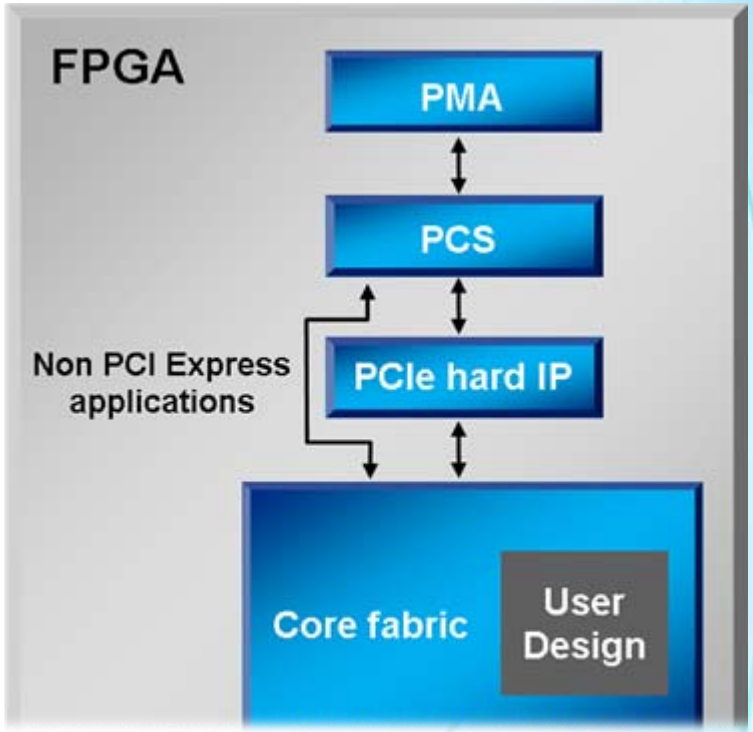
Transceiver Block – Up to 8 Transceivers



- Quad based
  - Each quad has four channels
  - 2 MPLLs per quad
- Spread spectrum clocking circuitry designed into the EP4CGX50 and larger
  - Enables V-by-one, DisplayPort and SATA
- Flexible clocking enables multiple protocols in a single quad
  - Can borrow GPLL, neighboring MPLL on EP4CGX50 and larger

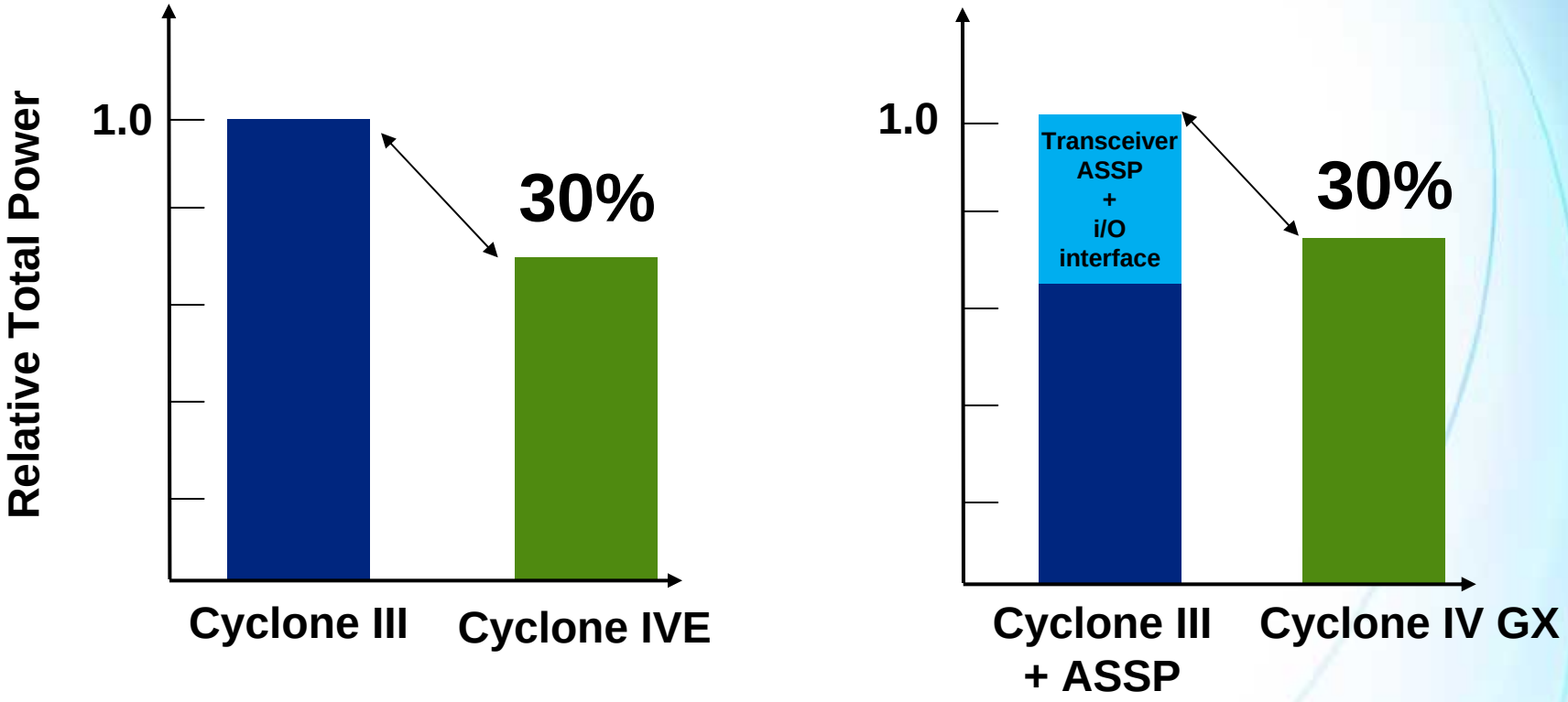
Accelerate PCI Express Designs

- Minimize effort
  - Built-in, pre-verified PCIe Gen1.1 hard IP block
  - Guaranteed timing
- Flexible
  - x4, x2, x1
  - Rootport and endpoint
  - Easy design entry with MegaWizard™
  - Reusable design example
- Reduce costs
  - Saves up to 15K LEs
  - No license fees



Proven PCIe Hard IP Solution

Lowest Power



Continued focus on lowering power

Cyclone IV Family

Variant	Device	LEs	Transceivers	Memory (Kbits)	Multipliers (18x18)
Cyclone IV E devices 1.0V	EP4CE6	6,272	-	270	15
	EP4CE10	10,320	-	414	23
	EP4CE16	15,408	-	504	56
	EP4CE30	28,848	-	594	66
	EP4CE40	39,600	-	1,134	116
	EP4CE55	55,856	-	2,340	154
	EP4CE75	75,408	-	2,745	200
	EP4CE115	114,480	-	3,888	266
Cyclone IV GX devices 1.2V	EP4SG15	14,400	2	540	0
	EP4SGX22	21,280	4	756	40
	EP4SGX30	29,440	4	1,080	80
	EP4SGX50	49,888	8	2,502	140
	EP4SGX75	73,920	8	4,158	198
	EP4SGX110	109,424	8	5,490	280
	EP4SGX150	149,760	8	6,480	360

Cyclone IV Devices - Package Options

Package	E144	QN148	F169	F256	F324	F484	F672	F780	F896	Quartus II software
Area, Pitch	**0.5mm 20 x 20**	**0.5 mm 11 x 11**	**1.0 mm 14 x 14**	**1.0mm 17 x 17**	**1.0 mm 19 x 19**	**1.0 mm 23 x 23**	**1.0 mm 27 x 27**	**1.0mm 29 x 29**	**1.0 mm 31 x 31**	
Product Line	**Maximum User I/O (Transceiver I/Os)**									
EP4CE6	94			182						v9.1 SP1
EP4CE10	94			182						v9.1 SP1
EP4CE15				168		346				v9.1 SP1
EP4CE30						331		535		v9.1 SP1
EP4CE40						331		535		v9.1 SP1
EP4CE55						327		377		v9.1 SP1
EP4CE75						295		429		v9.1 SP1
EP4CE115						283		531		v9.1 SP1
EP4CGX15		72 (2)	72 (2)							v9.1
EP4CGX22			72 (2)		150 (4)					v9.1
EP4CGX30			72 (2)		150 (4)					v9.1
EP4CGX50						290 (4)	310 (8)			v9.1 SP1
EP4CGX75						290 (4)	310 (8)			v9.1 SP1
EP4CGX110						290 (4)	310 (8)		475 (8)	v9.1 SP1
EP4CGX150						290 (4)	310 (8)		475 (8)	v9.1 SP1

Protocol Support

Protocol	Max. Bandwidth (Gbps)	EP4CGX15 - 30	EP4CGX50 - 150	IP support
PCIe Gen1.1	2.5	Yes	Yes	Embedded within FPGA
GbE	1.25	Yes	Yes	Altera
Basic (proprietary)		Up to 2.5	Up to 3.125	N/A
CPRI	3.072		Yes	Altera
XAUI	3.125		Yes	Altera
3G Triple Rate SDI	2.97		Yes	Altera
Serial RapidIO	3.125		Yes	Altera
SATA	3.0		Yes	Altera
V-by-one	3.0		Yes	3rd Party
DisplayPort	2.7		Yes	3rd Party

Cyclone IV Rollout Schedule