

Introduction

This design example shows how to use Altera® MAX® II CPLDs to implement voltage level shifters between different devices in a mixed-voltage design environment.

Multi-Voltage Systems

Devices on one circuit board can potentially use many different supply voltages, such as 5V, 3.3V, 2.5V, 1.8V and 1.5V. Therefore, the buses connected to a system can have different voltage standards that can lead to voltage-level conflicts. MAX II CPLDs are designed to interface directly with 1.5-V, 1.8-V, 2.5-V, and 3.3-V signals and can be used to eliminate these conflicts.

MAX II CPLDs can interface with other devices using different voltage levels because the core power supply voltage (V_{CCINT}) is separate from the CPLD output voltage (V_{CCIO}). A few applications for voltage level shifting are:

- Interfacing microprocessors with peripheral devices, timers, and transceivers that are operating at different I/O standards and levels
- Driving more than one set of GPIO pins having different I/O standards

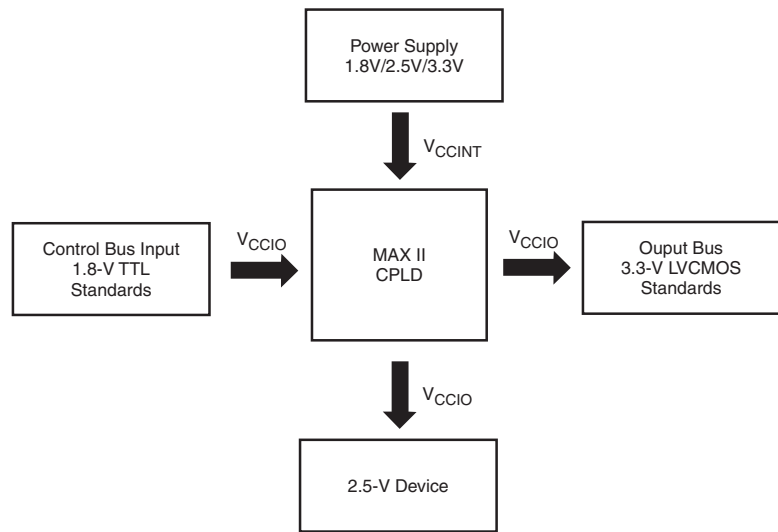
Using MAX II CPLDs as Level Shifters

MAX II CPLDs are designed to tolerate all types of power-on sequences making them ideal for multiple voltage systems where it is critical to maintain a particular power-on sequence.

You can configure each I/O bank to operate at a particular voltage using its V_{CCIO} pin. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces and each individual bank can support a different standard. In addition, each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. The number of I/O banks for a particular MAX II device depends on its part number. An internal LDO voltage regulator provides the necessary 1.8-V internal voltage supply to the device (except in MAX IIG and MAX IIZ devices). The voltage regulator supports 3.3V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage.

Figure 1 shows implementation of a multi-voltage system by voltage level shifting.

Figure 1. Implementing a Multi-Voltage System by Voltage Level Shifting

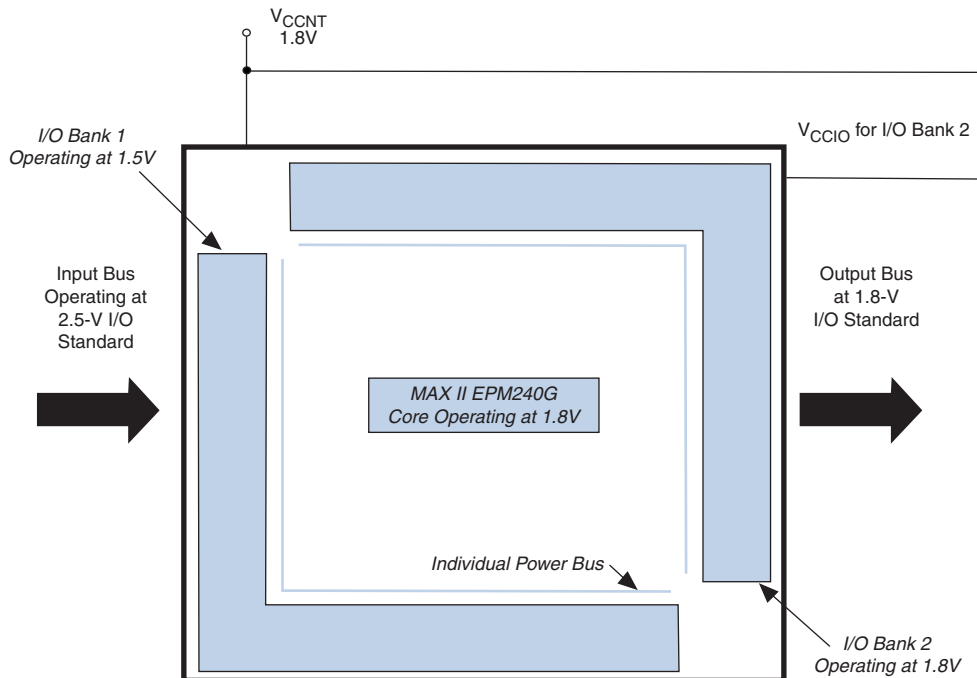


The I/O buffer of MAX II devices is programmable and supports a wide range of I/O voltage standards. Each I/O bank can be programmed to comply with a different I/O standard, such as the following:

- 3.3-V LVTTTL/LVCMOS
- 2.5-V LVTTTL/LVCMOS
- 1.8-V LVTTTL/LVCMOS
- 1.5-V LVCMOS

In addition to these standards that are supported by all MAX II devices (on the EPM1270 and EPM2210 devices) I/O Bank 3 also includes a 3.3-V PCII/O standard interface capability. MAX II devices with MultiVolt core I/O operation capability allow the core and I/O blocks of the device to be powered up with separate supply voltages. The V_{CCINT} pins supply power to the device core and the V_{CCIO} pins supply power to the device I/O buffers. You can power up the V_{CCINT} pins with 1.8V for MAX IIG devices or 2.5V/3.3V for MAX II devices. Therefore, MAX II CPLDs can receive inputs from, or drive outputs to devices with different voltage levels by shifting from one value on one I/O bank to a different value on another I/O bank.

Figure 2. Voltage Level Shifter Demonstration Circuit



Implementation

You can implement this design with an EPM240 device or any other MAX II CPLD, all of which have more than one I/O bank. Figure 2 shows the implementation of a simple voltage level shifter using an EPM240G device that has two I/O banks. Eight inputs are powered at 2.5V and eight outputs are powered at 1.8V to achieve 2.5V to 1.8V level translation. This design example is implemented in three basic steps that involve determining the physical pins (pin assignments), setting pin attributes in the Quartus® II software and relevant buffers assignment, and signal paths between input pins and output pins (this is accomplished by the source code).

Table 1 shows the implementation of this design example on the MDN-B2 demo board.

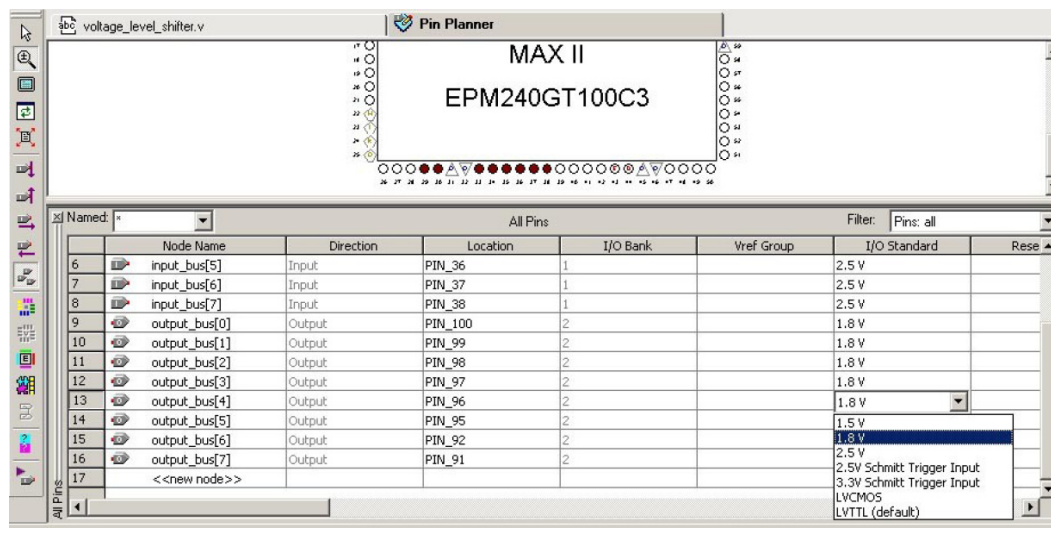
Table 1. EPM240G Pin Assignment

Signal	Pin	Signal	Pin
input_bus [7]	Pin 38	input_bus [6]	Pin 37
input_bus [5]	Pin 36	input_bus [4]	Pin 35
input_bus [3]	Pin 34	input_bus [2]	Pin 33
input_bus [1]	Pin 30	input_bus [0]	Pin 29
output_bus [7]	Pin 100	output_bus [6]	Pin 99
output_bus [5]	Pin 98	output_bus [4]	Pin 97
output_bus [3]	Pin 96	output_bus [2]	Pin 95
output_bus [1]	Pin 92	output_bus [0]	Pin 91

Unused pins are assigned As **input tri-stated** in the **Device and Pin Options** dialog box in the Quartus II software prior to compilation.

Figure 3 shows I/O standard assignments to I/O pins in the Pin Planner. Input pins, assigned on I/O bank 1 are assigned a 2.5-V I/O standard. Output pins on bank 2 are assigned a 1.8-V I/O standard by clicking in the cell of the **I/O Standard** column and selecting **1.8V**.

Figure 3. I/O Standards to I/O Pins in the Pin Planner in the Quartus II Software



Refer to the following demo Notes (to demonstrate this design on the MDN-B2 demo board):

- Set voltage jumpers on the MDN-B2 demo board corresponding to the voltage-level translation voltages; that is, V_{CCIO1} voltage is set to 2.5V with jumpers on JP9 and V_{CCIO2} voltage set to 1.8V using a jumper on JP7 of the demo board.
- Switch on power to the MDN-B2 demo board (using slide switch SW1).
- Download the design on to the MAX II CPLD through the JTAG header JP5 on the MDN-B2 demo board and a conventional programming cable such as ByteBlaster™ II or USB-Blaster™. Keep SW4 on the demo board pressed as you begin the programming process. Turn off power after the programming.
- Switch on SW1 (power) and set any 8-bit data on the input bus by using the DIP switch SW3 on the demo board. These switches switch to logic 0 in their ON position and vice versa.
- Observe and measure shifted voltage levels from V_{CCIO1} levels (2.5-V logic high level) on the input bus to V_{CCIO2} (1.8-V logic high level) and on the output bus on JP8. Map the DIP switch positions 1, 2, 3, 4, 5, 6, 7, and 8 to the output pins 20, 18, 16, 14, 12, 10, 8 and 6 on the output header JP8, respectively.

Source Code

This design example is implemented in Verilog HDL and successful operation is demonstrated with the MDN-B2 demo board. The source code, testbench, and complete Quartus II project are available at:

www.altera.com/literature/an/an490_design_example.zip

Conclusion

As shown in this application note, MAX II CPLDs are an excellent choice to implement voltage level shifters. Their low power and ability to tolerate all types of power-on sequences on their core and I/O banks make them ideal for voltage level translator applications. Specifically, this applies to multi-level voltage systems where it can be critical to maintain a specific power-on sequence of the multiple voltages involved.

Additional Resources

The following list contains additional resources:

- MAX II CPLD homepage:
www.altera.com/products/devices/cpld/max2/mx2-index.jsp
- MAX II Device Literature:
www.altera.com/literature/lit-max2.jsp
- MAX II Power-Down Designs:
www.altera.com/support/examples/max/exm-power-down.html
- MAX II App Notes:
AN 428: MAX II CPLD Design Guidelines
AN 422: Power Management in Portable Systems Using MAX II CPLDs

Revision History

Table 2 shows the revision history for this application note.

<i>Table 2. Revision History</i>		
Date and Document Version	Changes Made	Comments
December 2007 v1.0	Initial release.	—



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