

Introduction

A power component's ability to switch off and on is a valuable power saving technique. Altera® MAX® II CPLDs are well suited for this technique because of their simple power sequencing and proprietary features. This application note discusses a simple method for implementing Auto Start.



For more information about using the unique internal oscillator in MAX II CPLDs to accomplish an Auto Stop function, refer to [AN 422: Power Management in Portable Systems Using MAX II CPLDs](#)

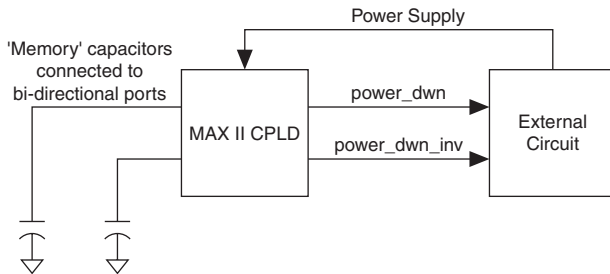
Power Saving

Many consumer and industrial application systems do not require the CPLD to be powered on at all times. It is preferred to have a design in which the CPLD powers on intermittently, remaining off for most of the cycle. This is especially useful in portable battery-operated systems which can function on a non-continuous periodic task.

Because MAX II CPLDs do not require a special power-on sequence, they can be switched on quickly (typically 200 μ s, depending on the logic density). The ability to switch on and off quickly allows you to completely switch off the CPLD and switch it back on using external circuitry. The external circuitry can be a simple RC timer designed for the required delay.

However, if you implement considerable power off time, such a simple RC timer circuit is not practical. This requires very large values of R & C. A counter utilizing capacitors as memory elements extends the power-down period. The CPLD turns on for a very small duration during this power -down period, reads the value in these capacitors, increments the count, and stores them back again before powering down. This cycle repeats itself until the desired count is reached, at which time the CPLD switches on completely. When it switches on in the power-on period, the CPLD executes the task it was designed to accomplish.

The CPLD uses the power down signals (`power_dwn` and its complement) to trigger the external circuit and power down the CPLD. After the designed delay, the external circuit powers on the CPLD. The memory capacitors are connected to the bidirectional pins of the CPLD and are used as non-volatile memory elements. [Figure 1](#) shows the basic block diagram of an Auto Start system.

Figure 1. Basic Block Diagram of an Auto Start System

Auto Start Using MAX II CPLDs

Figure 2 shows the flow of this design in the time period labeled as 't' in Figure 3. As soon as the CPLD is powered on, it goes into the read state. The value on the capacitors is read and stored in registers. This implementation uses two capacitors that allow you to store four different values. One of the four LEDs used is switched on after the read operation that corresponds to the value read from the capacitors. This value or count is incremented and stored back into the capacitors, which act as non-volatile memory elements. Power down is then initiated by setting the `power_dwn` pin high. When power down is complete, the external RC circuit acts as a timer and activates the CPLD. This is repeated until the desired delay is obtained (desired count is reached) and the complete effective stretching of the power-down time is achieved (four times in this case). The duty cycle of operation of the CPLD can be controlled, resulting in a longer power-down period and thereby decreasing the overall power consumption.

Figure 2. Auto Start Operation Flowchart

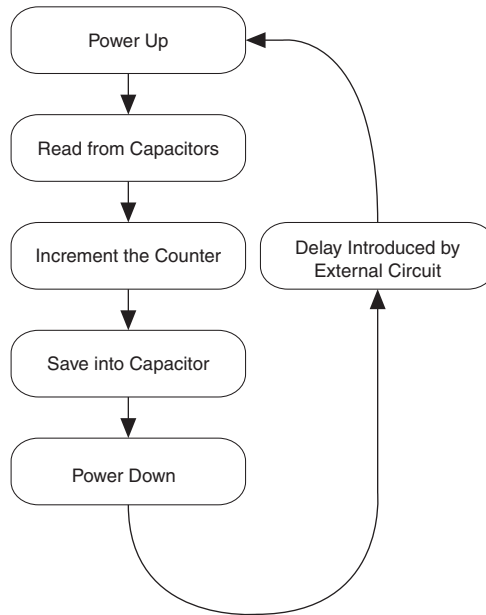


Figure 3. CPLD Power Cycle Waveform

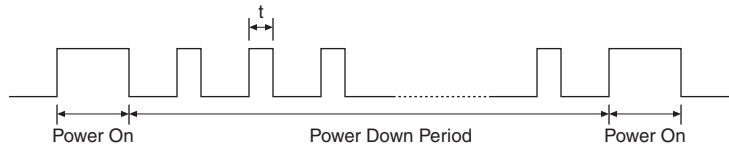
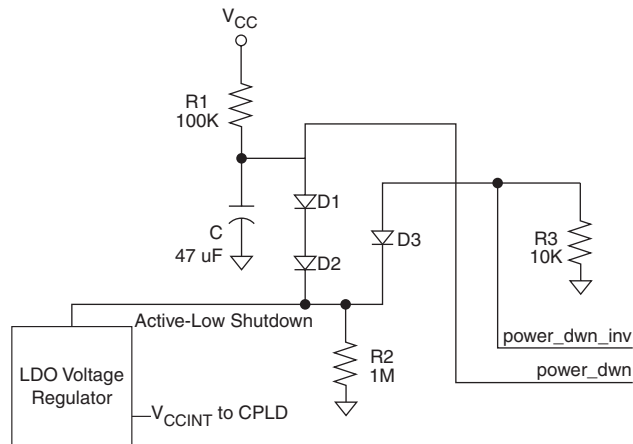


Figure 3 shows the CPLD's cycle of operation. Each cycle consists of a 'Power On' and a 'Power Down' period. In the 'Power Down' period the CPLD regularly switches on for a very small period of time 't', increments the counter, and switches off. When the desired count is reached, the CPLD enters into the Power On period and reinitializes the value of the counter. It then performs the desired functions. At the end of the 'Power On' period, the capacitors contain the reinitialized value. When the CPLD is powered on again, it increments the counter and shuts down after the period 't', and the count is restarted.

Figure 4 shows how the external circuit works. When the `power_dwn` signal is low (`power_dwn_inv` is high), the voltage regulator (which has an active low shutdown control) is switched on and the capacitor C discharges. Whenever the CPLD wants to switch off, it makes the `power_dwn` signal high (`power_dwn_inv` is low). This switches off the voltage regulator, cutting off the power to the CPLD.

Figure 4. External Circuitry



When all the I/O pins of the CPLD are tri-stated, the capacitor starts charging. It charges until the voltage across the CPLD remains less than the threshold potential of the regulator's shutdown control (enhanced by diodes D1 and D2). When the threshold is exceeded, the voltage regulator is switched on. The cycle repeats itself.

Implementation

You can implement this design example with an EPM240 (or any other MAX II CPLD), supporting external RC circuitry, a power supply that is capable of shut down, and two capacitors on the GPIO pins to act as 'memory' devices that save previous states. Implementation involves using the design example source code and allocating the appropriate signals and control lines to the GPIO lines of the MAX II device, along with its support circuitry. The MDN-B2 demo board has a built-in support circuitry.

To demonstrate the control of the power cycle, two capacitors (C9 and C10 on the MDN-B2 demo board) and four LEDs (D2, D3, D5, and D6) are used. This design reads the values from the capacitors as soon as the MAX II CPLD is powered on. Table 1 shows the read values that are displayed on the LEDs.

Table 1. LED Mapping

Capacitor C9	Capacitor C10	LED
0	0	D2
0	1	D3
1	0	D5
1	1	D6

For each set of values, the corresponding LED glows. The CPLD then increments the count and writes back this value to the capacitors. The write cycle continues for some time to ensure sufficient charging of the capacitors. The power down and its complement signals are made high and low, respectively, resulting in complete power down.

Upon subsequent power on after a period of time determined by the external RC, the MAX II CPLD repeats the cycle of reading, LED display, and updating the capacitor states before powering down again. Observing the LED counting up demonstrates the Auto Start feature of this design.

Table 2 shows the implementation of this design example on the MDN-B2 demo board:

Table 2. EPM240G Pin Assignments

Signal	Pin	Signal	Pin
cap_a	Pin 83	cap_b	Pin 84
led1	Pin 69	led2	Pin 70
led3	Pin 71	led4	Pin 72
pwr_dwn	Pin 14	pwr_dwn_inv	Pin 12

Unused pins are assigned As input tri-stated in the Device and Pin Options dialog box in the Quartus II software prior to compilation.

Refer to the following demo notes (to demonstrate this design on the MDN-B2 demo board):

- Ensure that V_{CCIO} voltages on both banks are set to 2.5V (jumpers on JP9 and JP7 on the demo board are set to 2.5V).
- Turn on the power to the demo board (using slide switch SW1) and download the design on to the MAX II CPLD through the JP5 JTAG header and a conventional programming cable such as the ByteBlaster™ II or USB-Blaster™. Keep SW4 on the board pressed as you begin the programming process. Turn off power to the board and remove the JTAG connector after programming.
- Turn on the power to the demo board. Using a voltmeter between TP3 and GND on the demo board, observe V_{CCINT} being powered down and powered up cyclically. Repeat observation for V_{CCIO} (between TP1 and GND on demo board). Also observe the 4 LEDs (D2, D3, D5, and D6) shift their position each time the power to the CPLD is restored. Each time the LED blinks, its position is based upon the previous LED position that blinked and in accordance to [Table 1 on page 5](#).

Source Code

This design example is implemented in Verilog HDL and successful operation is demonstrated with the MDN-B2 demo board. The source code, testbench, and complete Quartus II project are available at:

www.altera.com/literature/an/an491_design_example.zip

Conclusion

As shown in this design example, MAX II CPLDs are an excellent choice for implementing low power applications and when battery life extension are of importance. Their low power and unique feature of easy power on without the requirement of any power-up sequence enables them to incorporate Auto Start functionality in designs that can turn off the CPLD in between recurring system tasks.

Additional Resources

The following list contains additional resources:

- MAX II CPLD homepage:
www.altera.com/products/devices/cpld/max2/mx2-index.jsp
- MAX II Device Literature:
www.altera.com/literature/lit-max2.jsp
- MAX II Power-Down Designs:
www.altera.com/support/examples/max/exm-power-down.html

- MAX II Application Notes:
 - AN 428: MAX II CPLD Design Guidelines*
 - AN 422: Power Management in Portable Systems Using MAX II CPLDs*

Revision History

Table 3 shows the revision history for this application note.

Date and Document Version	Changes Made	Comments
December 2007 v1.0	Initial release.	—



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