

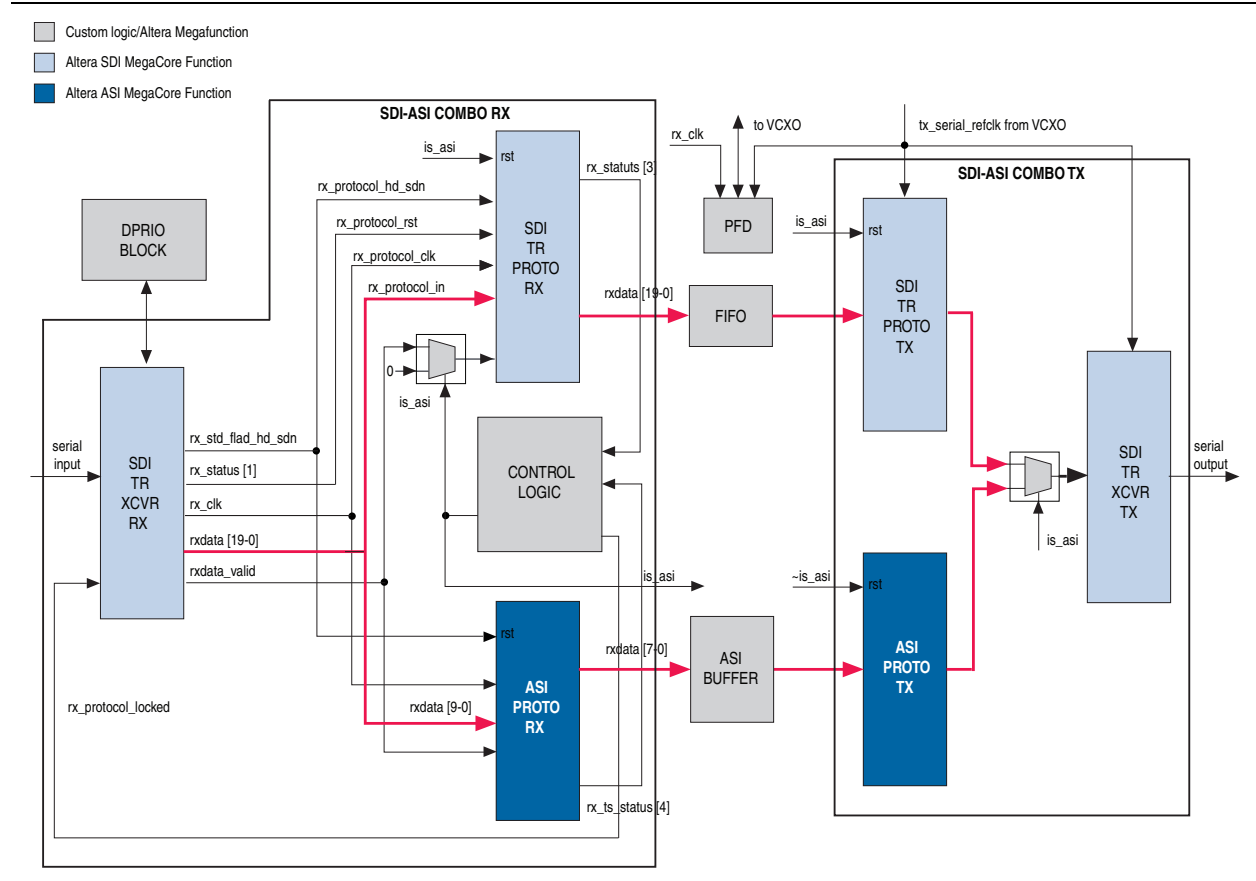
Introduction

This application note describes the SDI-ASI auto protocol detector reference design based on the combination of the current Altera SDI and ASI MegaCore® functions, and shows how to demonstrate the SDI-ASI combo block with the Stratix® II GX audio video development board.

Functional Description

Figure 1 shows a high level block diagram of the SDI-ASI auto detect combo which includes a combo receiver block and combo transmitter block. The combo block shows one channel input and one channel output.

Figure 1. SDI-ASI Auto Detect Combo Block Diagram



The following sections describe the various elements in the combo block in [Figure 1 on page 1](#).

SDI-ASI Combo Receiver

To implement the SDI-ASI combo receiver, you must instantiate the SDI triple-rate transceiver receiver (`SDI_TR_XCVR_RX`), SDI triple-rate protocol receiver (`SDI_TR_PROTO_RX`), and the ASI protocol receiver (`ASI_PROTO_RX`). The instantiation exposes the parallel data between the SDI transceiver and the SDI protocol layer for further ASI manipulations. Since the data rate of the ASI MegaCore function and the SD mode SDI MegaCore function are the same (270 Mbps), they can share a single SDI triple-rate transceiver. The control logic block asserts the ASI indication signal (`is_asi`) when it receives the ASI packet lock signal from the ASI protocol receiver. Otherwise, the `is_asi` signal is held low. You can use this signal to route the correct decoded parallel data into the respective signal processing blocks. This signal also controls and selects the correct MegaCore type for the retransmission.

SDI-ASI Combo Transmitter

To implement the SDI-ASI combo transmitter, you must instantiate the SDI triple-rate transceiver transmitter (`SDI_TR_XCVR_TX`), SDI triple-rate protocol transmitter (`SDI_TR_PROTO_TX`), and the ASI protocol transmitter (`ASI_PROTO_TX`). The combo transmitter block retransmits the decoded and buffered received data. The transceiver transmitter selects the output parallel data of the SDI/ASI protocol blocks based on the `is_asi` signal.

DPRIO Block (Reconfiguration Control Logic)

The reconfiguration control logic handles the reconfiguration of the receiver in the design. The reconfiguration control logic consists of several subblocks.

Phase Frequency Detector (PFD)

The PFD takes in the clock data recovery (CDR) and the transmitter reference clock, and compares the phase and frequency. It then adjusts the external transmitter reference clock source, so that the signals match in phase and frequency. The PFD allows you to lock a low jitter transmit reference clock to the recovered clock from the SDI input.

FIFO

A FIFO is placed in the SDI data path to cater for the PFD tracking time. When the SDI receiver is locked, the receiver data is written to the FIFO buffer. When the FIFO buffer is half full, the transmitter starts reading, encoding, and transmitting the data.

ASI Buffer

An ASI buffer is placed in the ASI data path to retime the parallel data from the receiver clock domain (148.5 MHz) to the transmitter clock domain (27 MHz).

Getting Started

This section discusses the requirements and related procedures to demonstrate the SDI-ASI auto protocol detector reference design with the Stratix II GX audio video development board. This section contains the following topics:

- [Hardware and Software Requirements](#)
- [Obtain the Design](#)
- [Demonstrate the Reference Design with Stratix II GX Audio Video Development Board](#)
- [Compilation Support for Other GX Devices](#)

Hardware and Software Requirements

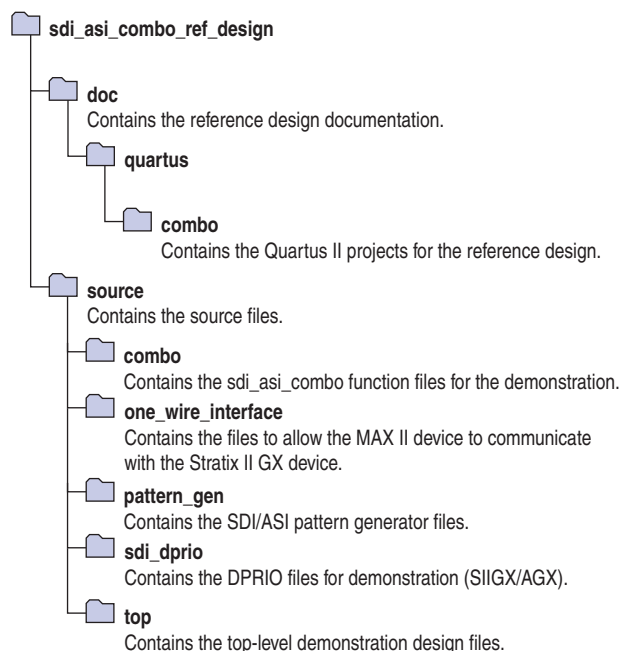
The demonstration requires the following hardware and software:

- Stratix II GX audio video development board
- SDI MegaCore function, version 8.0
- ASI MegaCore function, version 8.0
- Quartus® II software, version 8.0

Obtain the Design

Figure 2 shows the directory structure of the reference design.

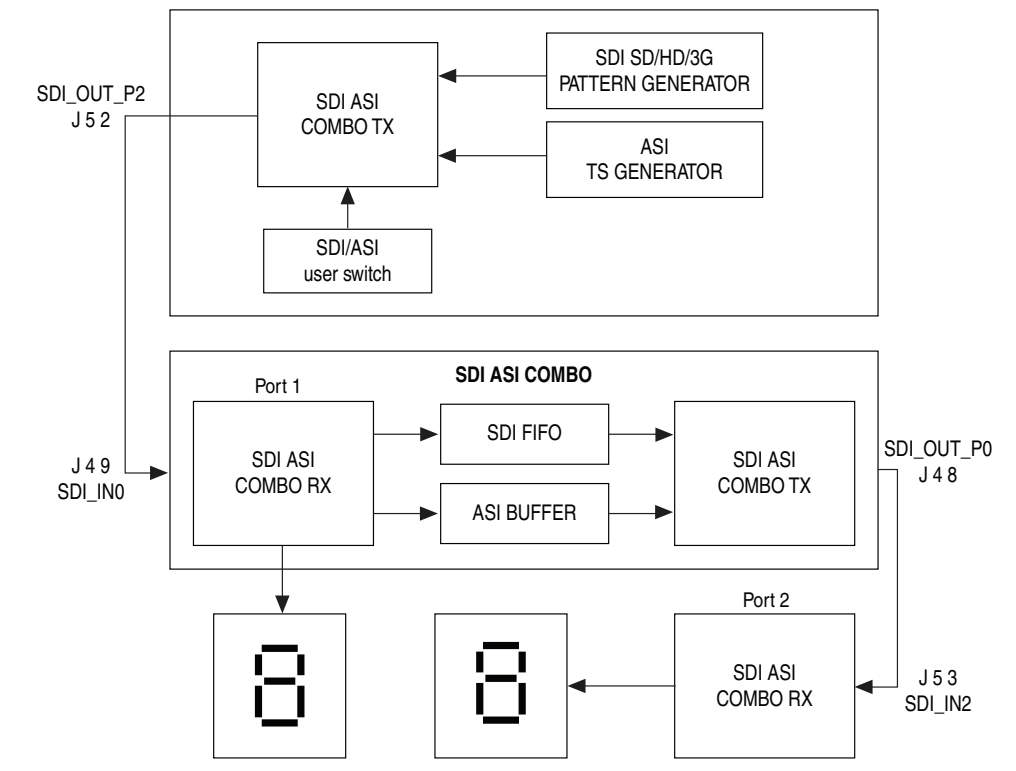
Figure 2. Directory Structure



Demonstrate the Reference Design with Stratix II GX Audio Video Development Board

Figure 3 shows the hardware setup for the demonstration.

Figure 3. Hardware Setup



To run the reference design, perform the following steps:

1. Set up the board connections.
 - a. Connect the test pattern transmitter output, *SDI_OUT_P2* (BNC J52), to the receiver input, *SDI_IN0* (BNC J49), of the SDI-ASI combo block.
 - b. Connect the transmitter output, *SDI_OUT_P0* (BNC J48), of the SDI-ASI combo block to another receiver input, *SDI_IN2* (BNC J53).
2. Launch the Quartus II software.
3. On the File menu, click **Open Project**, navigate to `/quartus/combo/sdi_combo_asi.qpf`, and click **Open**.
4. On the Processing menu, click **Start Compilation**.
5. Download the Quartus II-generated SRAM Object File (`.sof`), `/quartus/combo/sdi_combo_asi.sof`.

When you connect the transmitter output to the receiver port 1, the LEDs on the board indicate the following conditions:

1. LED7 illuminates when the SDI receiver is word aligned (`rx_status [2]`) at port 1.
2. LED6 illuminates when the SDI received line format (`rx_status [3]`) is stable at port 1.
3. LED5 illuminates when the SDI frame format (`rx_status [4]`) is stable at port 1.
4. LED4 flashes to indicate the presence of the receiver reference clock port 1.
5. LED7 and LED6 illuminate when the ASI receiver is locked to 188-byte packet (`rx_ts_status [5:4]`) at port 1.
6. The rotary encoder switch (`SW2`) allows you to select the SD-SDI output, HD-SDI output, 3-Gbps SDI output, or the ASI output for `SDI_OUT_P2`.
 - a. Based on the output selected, the first and second seven-segments from the left indicate the following information:
 - `tS` = SD-SDI 270-Mbps output
 - `tH` = HD-SDI 1.485-Gbps output
 - `t3` = 3-Gbps SDI 2.970-Gbps output
 - `tA` = ASI 270-Mbps output
 - b. Based on the output selected, the third seven-segment display from the left indicates the following information:
 - `-` = unlocked
 - `S` = the combo receiver port 1 locked to SD-SDI signal
 - `H` = the combo receiver port 1 locked to HD-SDI signal
 - `3` = the combo receiver port 1 locked to 3-Gbps SDI signal
 - `A` = the combo receiver port 1 locked to ASI signal

The SDI-ASI combo receiver port 2 is used to validate the data retransmission of the combo block. When you connect the transmitter output to the receiver port 2, the LEDs indicate the following conditions:

1. LED3 illuminates when the SDI receiver is word aligned (`rx_status [2]`) at port 2.
2. LED2 illuminates when the SDI received line format (`rx_status [3]`) is stable at port 2.
3. LED1 illuminates when the SDI frame format (`rx_status [4]`) is stable at port 2.
4. LED0 flashes to indicate the presence of the receiver reference clock port 2.
5. LED3 and LED2 illuminate when the ASI receiver is locked to 188-byte packet (`rx_ts_status [5:4]`) at port 2.

6. Based on the output selected, the fourth seven-segment display from the left indicates the following information:
 - - = unlocked
 - S = the combo receiver port 2 locked to SD-SDI signal
 - H = the combo receiver port 2 locked to HD-SDI signal
 - 3 = the combo receiver port 2 locked to 3-Gbps SDI signal
 - A = the combo receiver port 2 locked to ASI signal

Compilation Support for Other GX Devices

To compile the reference design with Arria® GX device, perform the following steps:

1. On the Quartus II Assignments menu, click **Device** and select **Arria GX** at **Device family** to change the device.
2. Click **OK**.
3. On the Tools menu, launch the **MegaWizard Plug-In Manager**.
4. Regenerate each SDI and ASI instance in the **sdi_asi_combo_ref_design/source/combo** directory:
 - a. Click **Edit an existing custom megafunction variation** and navigate to a MegaCore function wrapper file and click **Next**.
 - b. Make sure that **Arria GX** is selected in **Currently selected device family** and click **Finish**.
5. On the Processing menu, click **Start Compilation** to compile the design.

This reference design will further support the Arria GX and Stratix IV audio video development boards once the hardware is available.

Revision History

Table 1 shows the revision history for this application note.

Table 1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
November 2008 version 1.0	Initial Release.	—



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