

Altera's 28-nm Device Portfolio

Tailored to Your Design Needs

One Size Does Not Fit All

What do you do when system performance demands threaten to increase power consumption and cost? What happens if you've got the power you need but not the performance?

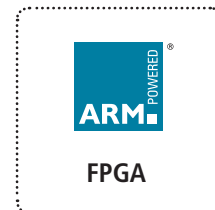
Wouldn't it be great if you didn't have to sacrifice one benefit to gain another?

That's the thinking behind Altera's 28-nm device portfolio. Whether you need the highest performance, the lowest cost, or something in between, our portfolio is tailored to your design needs. So you'll get just what you need to differentiate your products without any tradeoffs.

The portfolio includes:

- **Cyclone® V FPGAs:** lowest system cost and power for high-volume applications
- **Arria® V FPGAs:** optimal balance of cost, power, and performance for mid-range applications
- **Stratix® V FPGAs:** highest bandwidth, density, and performance at the lowest total power for high-end designs
- **HardCopy® V ASICs:** low-risk, low-power, and low-cost path to take your FPGA designs to volume production

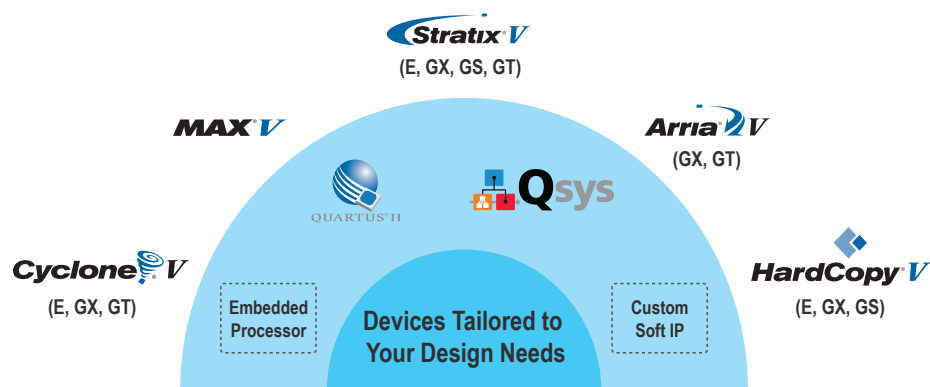
In our newest devices, you get abundant hard intellectual property (IP) blocks. You'll be able to reduce design time, related soft costs, and power, while getting the performance you need. What's more, you also get a broad set of soft and hard embedded processor cores from Altera (Nios® II processor), ARM® (Cortex™-A9MP), and Freescale (V1 ColdFire), all using a common FPGA design flow.



New Low-Cost CPLD Family

Also new to the Altera® family: MAX® V CPLDs. MAX V CPLDs provide the industry's best value with their mix of low price, low power, and robust features for general-purpose and portable applications. You'll get:

- A non-volatile architecture for fast performance of “boot loader” functions
- Up to 50 percent lower total power vs. competing CPLDs, with static power as low as 45 uW
- Packages as small as 20 mm²



Our latest programmable devices are supported by rich design resources and meet your unique needs.

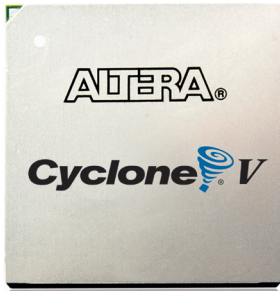
Why Process Matters

Using a single process has its limits. You simply wouldn't get a portfolio of devices capable of meeting a wide range of design requirements. That's why we decided to develop our 28-nm devices on two processes from Taiwan Semiconductor Manufacturing Corporation (TSMC). Each process is optimized for a specific set of advantages.

- TSMC's 28-nm Low Power (28LP) process is optimized for lowest power and cost, delivering up to 50 percent lower dynamic power vs. the previous generation. Cyclone V and Arria V FPGAs are manufactured on the 28LP process.
- TSMC's 28-nm High Performance (28HP) process is optimized for highest bandwidth without exceeding your power budget, yielding 35 percent faster devices vs. the 28LP process. Stratix V and HardCopy V devices are manufactured on the 28HP process.

FPGAs for All Your Needs

Process technology isn't the only area where we've innovated to create our unique device portfolio. We've also pushed the envelope in device architecture, transceiver technology, and hard IP blocks. The result? An array of differentiated devices to meet your design requirements.



Cyclone V FPGAs: Lowest Cost and Power

- 3.3-V I/Os
- Multifunction PCI Express® Gen2 x2
- Hard memory controllers for DDR3 (400 MHz), Mobile DDR2, and LPDDR2
- 3.125-Gbps and 5-Gbps transceivers
- Most designs under 5 watts



Arria V FPGAs: Balanced Cost, Power, and Performance

- 3.3-V I/Os
- Multifunction PCI Express Gen2 x4
- Hard memory controller (DDR3 at 533 MHz)
- 6.375-Gbps and 10.3125-Gbps transceivers
- 3 power rails for simple power network design



Stratix V FPGAs: Highest Bandwidth, Density, and Performance

- High-performance memory controllers for DDR3 at 1,066 MHz, RLDRAII, and QDR II+ SRAM
- 14.1-Gbps and 28.05-Gbps transceivers
- Embedded HardCopy Blocks (PCI Express Gen3 x8)
- Highest precision variable-precision DSP blocks

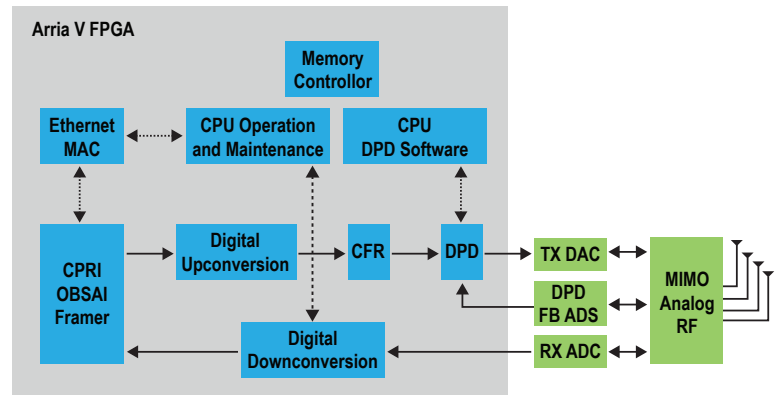
Where You Can Use Our Newest Devices

Here's a sampling of applications where you can take advantage of the capabilities in our newest device families.

Remote Radio Head

For remote radio heads, Arria V FPGAs deliver:

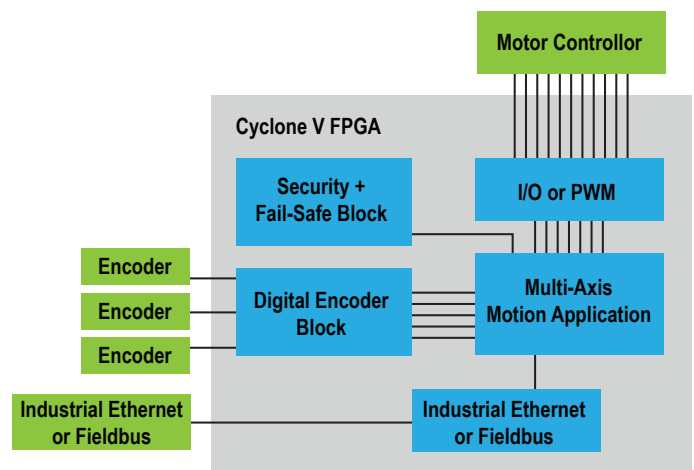
- <10-W power
- Up to 35 transceivers at up to 6.375 Gbps on GX variant; 90 mW per transceiver channel at 6.375 Gbps
- Up to 6 transceivers at up to 10.3125 Gbps on GT variant; 135 mW per transceiver channel at 10.3125 Gbps
- Native support for finite impulse response (FIR) filters in variable-precision DSP blocks
- Hard memory controller with support for DDR3 at 533 MHz
- Efficient resource utilization via two full 18x19 bit paths on each DSP block



Motor Controller

For motor control applications, Cyclone V FPGAs deliver:

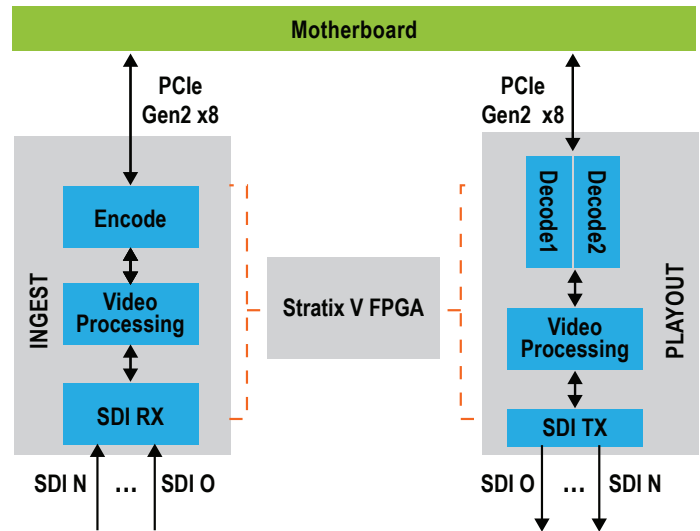
- < 5-W power
- Fewer components for reduced bill of materials (BOM) cost
- Native floating-point support in all DSP blocks
- Ability for you to quickly adapt to evolving Industrial Ethernet protocols
- User-friendly partial reconfiguration, which lets you change core and transceiver functionality on the fly while other portions of your design are running
- >15-year life cycle, supporting long life spans of industrial equipment
- Integrated security to protect your design from cloning and reverse engineering
- Single event upset (SEU) detection and mitigation



Studio Video Server

For studio video servers, Stratix V FPGAs deliver:

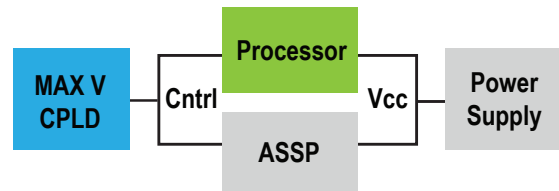
- Support for multiple CODECs through user-friendly partial reconfiguration
- Native 10-bit memory support for faster video buffering of larger and more frames
- Efficient video processing with high ratio of multipliers and memory-to-logic
- Productivity-enhancing solution supported by Video and Image Processing (VIP) Suite of IP cores
- Path to HardCopy V ASICs for lower cost and power volume production



Power Management

MAX V CPLDs are ideal for applications including power management, offering:

- Instant-on capability, so you can power up MAX V CPLDs first and then manage start-up sequences for other devices
- Multi-volt support, so you can select the most convenient I/O voltage for the power management interface (3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V)
- Internal oscillator for periodic monitoring of various power planes, power supplies, and downstream devices
- User flash memory, which captures system information for debug and diagnostic tasks



Common Design Toolset = Better Productivity

Our 28-nm device families are supported by a common, productivity-enhancing design environment. A set of common software tools and design resources equip you to swiftly turn your concepts into revenue-generating applications:

- Quartus® II design software, including its new Qsys system integration tool (available in Subscription Edition v11.0) and PowerPlay power analysis tool
- Embedded processors for efficient implementation of software-oriented features. Our multi-vendor, multi-CPU architecture system-on-a-chip (SoC) platform includes ARM, MIPS, and Nios II processor options.
- Soft IP functions for quick and easy implementation of hardware functions

Innovation You Can Count On

When system performance, power, and cost requirements clash, you've got a solution in our 28-nm device portfolio. Create differentiated products with less time and effort.

Get more details about our 28-nm portfolio by contacting your local Altera® sales representative or FAE or by visiting www.altera.com/28nmportfolio.

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