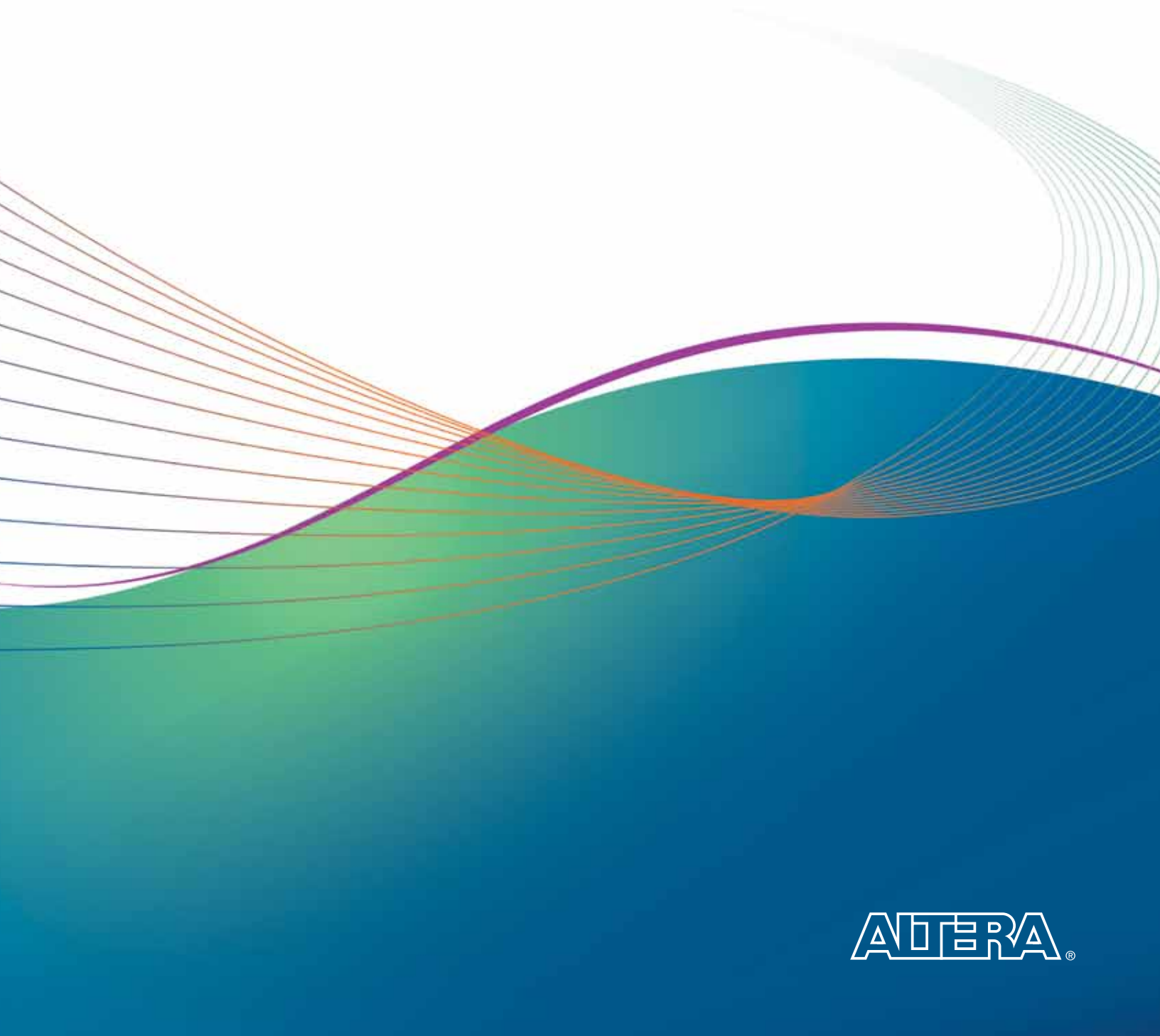


**Stratix V FPGAs: Built for Bandwidth**



## Meeting Bandwidth Demands

Mobile video, audio/video streaming, cloud computing—these are just a few of the many applications driving up bandwidth demands for the underlying communications infrastructure. To be successful, your next-generation products need to meet bandwidth requirements and stay within stringent cost and power budgets.



### That's why, for Altera, simply staying on Moore's Law alone isn't enough.

With our drive to both innovate and to extend our technology leadership, we've created programmable technologies that take you beyond the benefits possible through Moore's Law. Our new 28-nm Stratix® V FPGAs address bandwidth, cost, and power challenges through process improvements *and* unique innovations that dramatically increase the FPGA's capabilities:

- Integrated 12.5-Gbps and 28-Gbps transceivers—get breakthrough bandwidth at lowest bit-error rate (BER) while staying within your cost and power budgets
- Embedded HardCopy® Blocks—integrate more, and get twice the density without a cost and power penalty
- User-friendly fine-grained partial reconfiguration—get ultimate flexibility to easily change core functionality on the fly

For volume production, migrate your Stratix V designs to our new 28-nm HardCopy V ASICs. Also with transceiver variants, HardCopy V ASICs provide pin-, package-, and signal integrity-compatibility with Stratix V FPGAs. The seamless path to HardCopy V ASICs increases performance and lowers design risk, cost, and, by up to 50 percent, power consumption.

## Innovations at 28 nm: Stratix V Variants

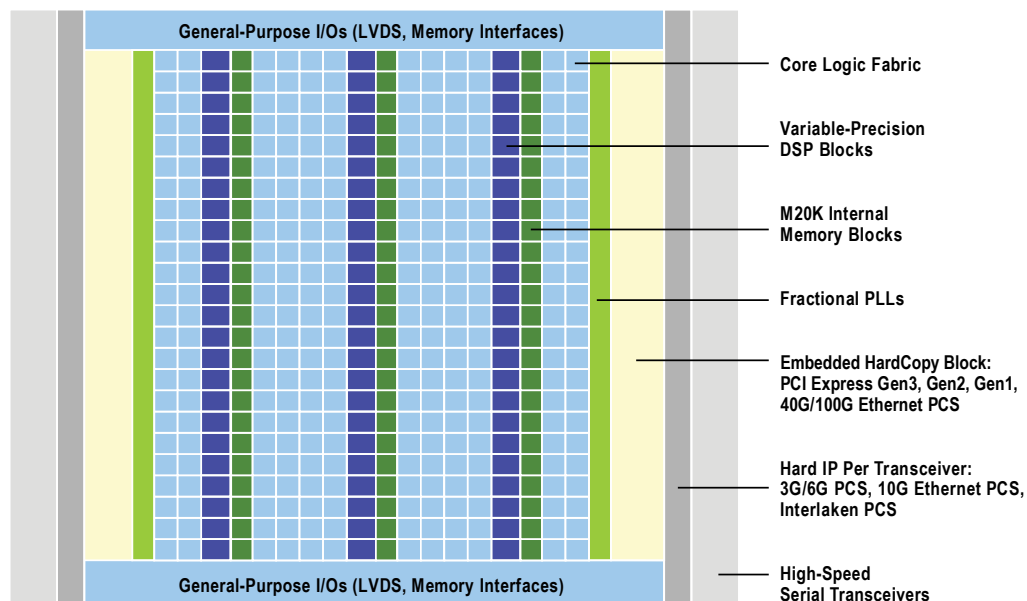
Stratix V FPGAs deliver the highest bandwidth, highest levels of system integration, and ultimate flexibility for a wide variety of applications in areas such as communications, military, broadcast, computer/storage, and test and medical. Choose from a new class of application-targeted FPGAs from within four primary variants:

- Stratix V GT FPGA – Optimized for designs with 28-Gbps transceivers requiring ultra-high bandwidth and performance, such as 40G/100G/400G applications
- Stratix V GX FPGA – Optimized for high-performance, high-bandwidth applications with integrated 12.5-Gbps transceivers supporting backplanes and optical modules
- Stratix V GS FPGA – Optimized for high-performance variable-precision digital signal processing (DSP) applications with integrated 12.5-Gbps transceivers supporting backplanes and optical modules
- Stratix V E FPGA – Optimized for ASIC prototyping with over 1 million logic elements on the industry's highest performance logic fabric

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## Stratix V Floorplan

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## Stratix V Device Highlights

- More than 1 million logic elements (LEs)
- Up to 50 Mb of embedded memory
- Up to 66 identical transceivers with a continuous range of 600 Mbps to 12.5 Gbps
- 28-Gbps transceivers, with a continuous range of 20 Gbps to 28 Gbps
- Up to 6 x72 DDR3 DIMMs at 800 MHz
- 1.4-Gbps LVDS performance
- Up to 3,510 variable-precision DSP blocks
- Embedded HardCopy Blocks

## Highest Bandwidth—Meet Requirements of Data-Intensive Applications

Stratix V FPGAs deliver the highest chip bandwidth through:

- 1.6 Tbps of serial switching capability
- 1,755 GMACS of signal-processing performance
- Up to 6 x72 DDR3 memory interfaces at 800 MHz
- Up to 4 PCI Express Gen3 x8 hard IP blocks

## Lowest Total Power

- Programmable Power Technology
- 28-nm high-K metal gate manufacturing process optimized for low power
- 0.85-V core voltage
- Partial reconfiguration
- Embedded HardCopy Blocks
- Integrated hard intellectual property (IP) per transceiver

## Stratix V Core Architecture

Feature	Why It's Important
Variable-precision DSP block	Provides native support for signal processing of varying precisions—18x18, 27x27, or 18x36—in a sum or independent mode
Adaptive logic module (ALM)	Enhanced ALM with 4 registers per 8-input fracturable look-up table (LUT), enabling higher system performance, easier timing closure, and higher logic capacity
M20K embedded memory block	Maximizes internal memory bits, and simplifies floor planning and routing with hardened error correction code (ECC) capabilities
Enhanced memory logic array block (MLAB)	Provides higher performance for optimal implementation of wide shallow FIFOs (MLAB = 640 bits)
Enhanced routing	Increased logic reach for higher core utilization (> 90 percent) and system performance

## System Integration—Get Increased Functionality in a Smaller FPGA

Providing an unprecedented level of system integration, Stratix V FPGAs give you more functionality in a smaller device, lowering power and cost. Innovations enabling this include:

- Embedded HardCopy Blocks delivering up to 14M ASIC gates or up to 1.12M logic elements to harden standard or logic-intensive applications.
- User-friendly partial reconfiguration, enabling you to reduce the count and size of FPGAs, saving you board space, cost, and power
- Fractional phase-locked loops (fPLLs), providing you with increased clocking flexibility and replacing external voltage-controlled crystal oscillators (VCXOs)
- Integrated electronic dispersion compensation (EDC) capability in transceivers, eliminating the need for external PHYs to interface to optical modules.
- Built-in advanced signal conditioning circuitry enabling transceivers to directly drive 10GBASE-KR backplanes

With Embedded HardCopy Blocks, we've developed application-targeted devices within our primary variants for functions including PCI Express Gen3, Gen2, and Gen1, Interlaken, and 40/100 Gigabit Ethernet (GbE) protocols.

## Ultimate Flexibility—Change Transceiver and Core Functionality On the Fly

With Stratix V FPGAs, you can easily change transceiver and core functionality on the fly while other portions of the design are still running. This flexibility comes from:

- A user friendly method for partial reconfiguration, which requires less development time and effort than competing solutions.
- Dynamically reconfigurable transceivers, which let you easily support multiple protocols, data rates, and physical media attachment (PMA) settings.
- Configuration via PCI Express, which enables you to configure the FPGA using the existing PCI Express link in your application. You'll have a simplified board design by minimizing the number of external configuration devices on your board.

## Industry Applications at 28 nm

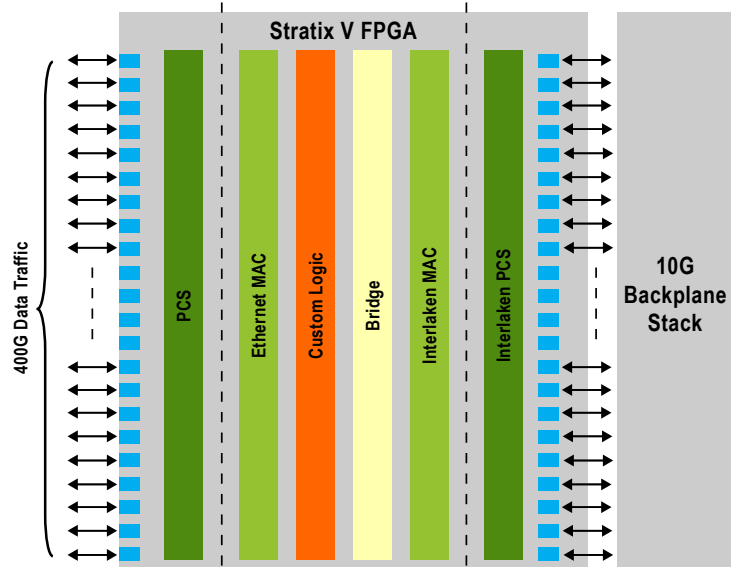
Changing protocol standards, increasing bandwidth and DSP performance demands, cost pressures, product differentiation—these are just a few of the design challenges Stratix V FPGAs meet for a variety of industry applications.

The applications here provide examples of how unique capabilities in our new 28-nm devices can support a wide range of next-generation designs.

### Wireline

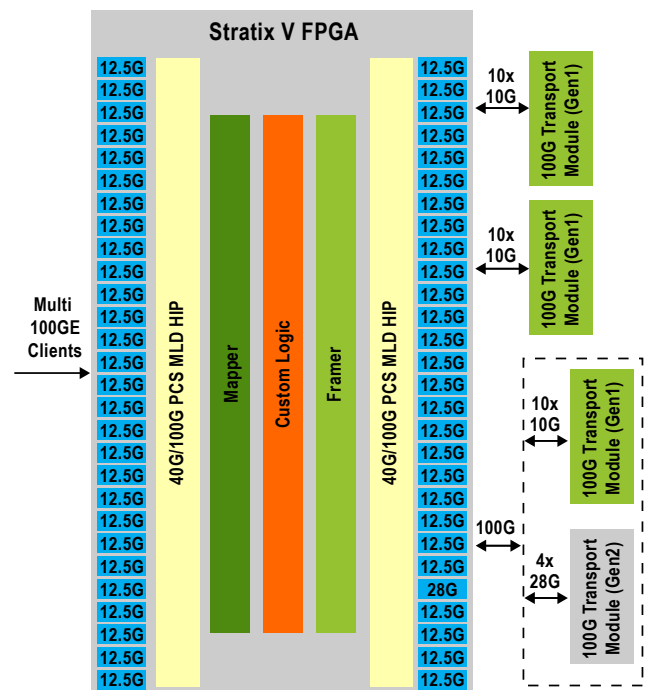
#### 400 GbE Line Card

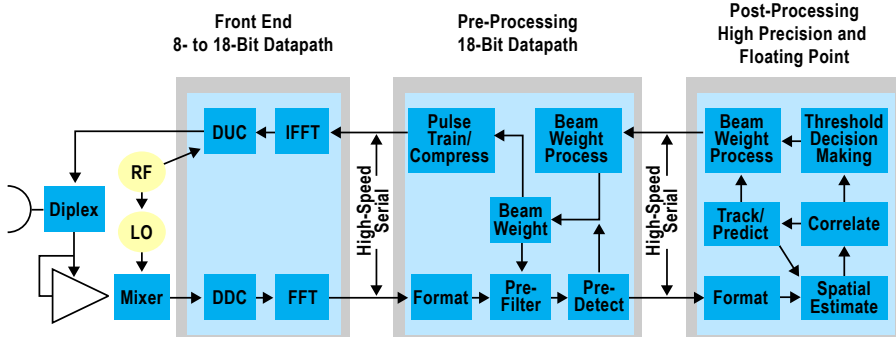
- Highest bandwidth, with 66 backplane-capable transceivers with continuous data rate support from 600 Mbps to 12.5 Gbps
- Integrated multi-protocol support, including hard PCS blocks supporting Interlaken and 40G/100G/400G applications
- Next-generation 400G application support through 28-Gbps transceivers with continuous data rate support from 20 Gbps to 28 Gbps



#### 28-Gbps Optical Transport Network (OTN) Platform

- Single FPGA platform supporting multiple 40G/100G OTN solutions
- Integrated multi-protocol support, including hard MLD/PCS blocks for 40 GbE and 100 GbE
- Direct optical module interface support
- 28-Gbps transceivers with continuous data rate support from 20 Gbps to 28 Gbps for next-generation optical interfaces
- Easy-to-use partial reconfiguration enabling multi-standard client interfaces
- Board space savings with integrated VCXO function inside fPLLs

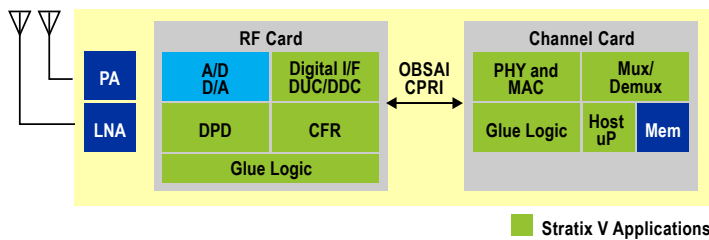




## Military

### Radar Application

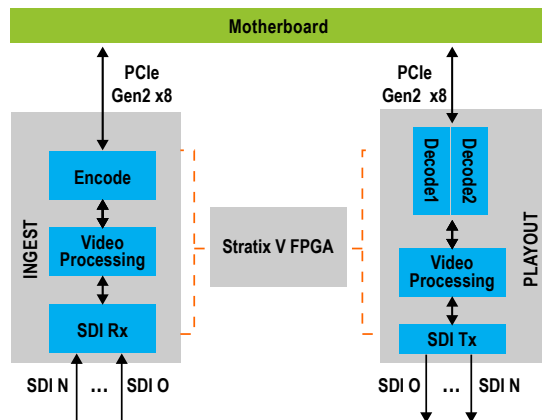
- Efficient floating-point multiplication with up to 1,000 GFLOPS
- Higher signal processing bandwidth with up to 1,755 GMACS
- Automatic single event upset (SEU) detection and correction
- Design security with enhanced Advanced Encryption Standard (AES) algorithm and 256-bit volatile and non-volatile keys
- Productivity-boosting tools in Quartus® II software, including DSP Builder Advanced Blockset and incremental compilation



## Wireless

### RF Card and Channel Card

- Reduced board space, power, and cost via fewer data channels and higher throughput per channel
- Lower system latency and increased system performance and reliability via greater integration
- Design differentiation using highest DSP- and memory-to-logic ratios
- Higher MIMO and bandwidth density compared to competitive offering



## Broadcast

### Studio Video Server

- Best-in-class serial digital interface (SDI) solution
- Support for multiple CODECs through user-friendly partial reconfiguration
- Optimal memory design with native 10-bit support
- Efficient video processing with high ratio of multipliers- and memory-to-logic
- Complete solution via CODECs and 1080p video framework IP core

## Seamless Path to HardCopy V ASICs

When you're ready for volume production, the seamless path from Stratix V FPGAs to package-, pin-, and signal integrity-compatible HardCopy V ASICs lowers risk, cost, and power consumption. Design with Quartus II software, and you can develop one design, using a single set of IP cores and a single set of timing constraints for both the FPGA and ASIC implementations.

The cost advantages of HardCopy V ASICs stem from lower NRE costs based on a reduced number of mask layers vs. standard-cell ASICs. Decreased verification time, and fast and predictable turn-around time—coupled with first-time-right silicon—also lower costs.

HardCopy V ASICs typically generate a 50 percent power reduction, because you're using a smaller die compared to Stratix V FPGAs, have hard-wired routing, and unused elements are removed from the power rail.

## Innovation You Can Count On

To get your concept off the ground and simplify your design process with Stratix V FPGAs, look to our reference designs, design examples, development kits, training classes, and technical support. Learn more by contacting your local Altera® sales representative or FAE, and by visiting [www.altera.com/stratixv](http://www.altera.com/stratixv) for white papers, webcasts, design resources, and more.

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