

**ALTERA**®

# **MAX II**

*The Lowest-Cost CPLD Ever*



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## The Lowest-Cost CPLD Ever

**MAX II** Building on more than 15 years of CPLD leadership and innovation, Altera introduces the MAX<sup>®</sup> II device, the lowest-cost CPLD ever. MAX II devices are based on a groundbreaking new architecture that delivers the lowest cost per I/O pin and the lowest power of any CPLD family. At less than half the price of other CPLDs, this instant-on, non-volatile device family targets general-purpose, low-density logic applications. In addition to delivering the lowest cost for traditional CPLD designs, MAX II devices expand cost and power improvements to higher densities, enabling designers to use MAX II devices in place of higher-cost or higher-power FPGAs, ASSPs, and standard logic devices.

Based on a cost-optimized 0.18- $\mu$ m flash process with six metal layers, MAX II devices operate at approximately one-tenth the power of previous MAX devices. MAX II devices offer densities ranging from 240 to 2,210 logic elements (LEs) and up to 272 user I/O pins. Table 1 describes some of the highlights of MAX II devices, and Table 2 shows the features and available packages.

### Groundbreaking New CPLD Architecture

Based on a groundbreaking new CPLD architecture, MAX II devices redefine the value proposition for CPLDs. Historically, CPLDs have been limited in their ability to deliver a competitive cost structure when compared to small FPGAs. The new MAX II CPLD architecture offers the competitive pricing of low-density FPGAs plus the engineering advantages of being a single-chip, instant-on, non-volatile device.

At higher densities, look-up table (LUT)-based logic array blocks (LABs) and row-and-column routing are more die-size efficient (Figure 1). Because MAX II CPLDs are based on an LUT architecture, they can deliver four times the density, which, combined with instant-on, non-volatility,

make the MAX II device a lower-cost and higher-density CPLD than competing solutions.

Figure 2 illustrates the revolutionary MAX II CPLD architecture, including an array of LUT-based LABs, a bank of non-volatile flash memory, and Joint Test Action Group (JTAG) control circuitry. The MultiTrack<sup>™</sup> interconnect is designed to maximize performance and minimize power by using the most efficient, direct connection from input to logic to output.

Feature	Benefits
Cost-Optimized Architecture	Get 4X the density at half the price with the revolutionary MAX II architecture
Low Power	Reduce power consumption and increase system reliability
High Density	Implement more applications in a single, low-cost device
Non-Volatile & Instant-On Functionality	Reduce cost and board space with a single-chip solution
User Flash Memory	Minimize system costs and chip count by integrating discrete serial or parallel non-volatile storage onto MAX II devices
Real-Time In-System Programmability (ISP)	Reduce maintenance costs by updating while the device is in operation
MultiVolt <sup>™</sup> Core	Operate with a 1.8-, 2.5-, or 3.3-V power supply, minimizing power rails and simplifying board design
MultiVolt I/O Interface	Interface seamlessly to other devices at 1.5-, 1.8-, 2.5-, or 3.3-V logic levels
MultiTrack Interconnect	Optimize performance with general and local routing lines, including a new direct logic cell-to-I/O path called FastIO connection
JTAG Translator	Simplify board management by using MAX II devices to configure external non-JTAG-compliant flash devices

Feature	EPM240	EPM570	EPM1270	EPM2210
LEs	240	570	1,270	2,210
Typical Equivalent Macrocells	192	440	980	1,700
Maximum User I/O Pins	80	160	212	272
User Flash Memory Bits	8,192	8,192	8,192	8,192
Speed Grades	3, 4, 5	3, 4, 5	3, 4, 5	3, 4, 5
Fastest $t_{PD1}$ (corner-to-corner performance)	4.5 ns	5.5 ns	6.0 ns	6.5 ns
Available Packages <sup>1</sup>	100-pin TQFP <sup>2</sup>	100-pin TQFP 144-pin TQFP 256-pin BGA <sup>3</sup>	144-pin TQFP 256-pin BGA <sup>3</sup>	256-pin BGA <sup>3</sup> 324-pin BGA <sup>3</sup>

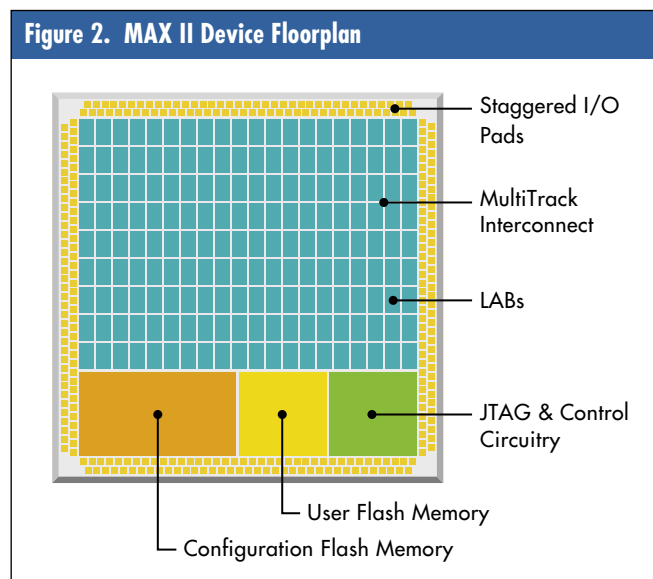
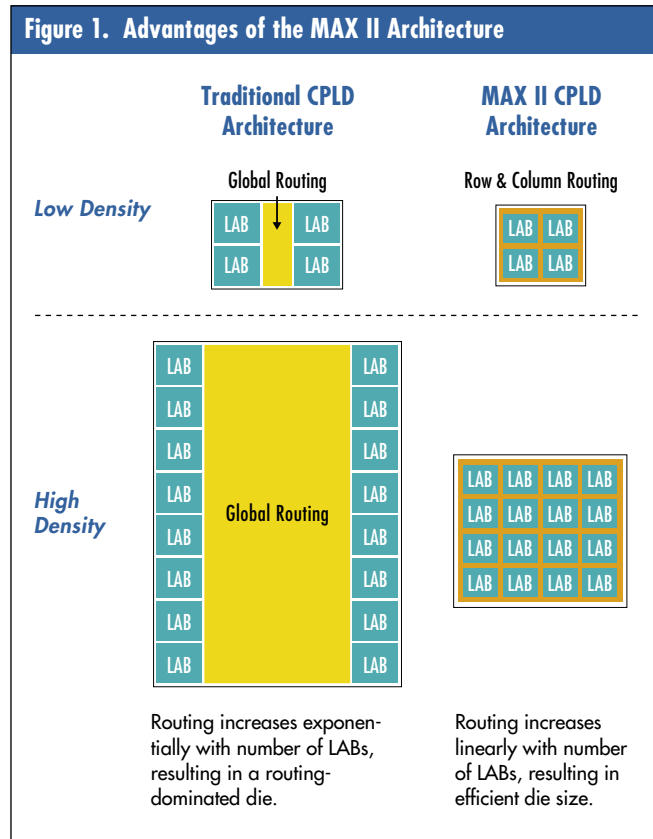
Notes:

<sup>1</sup> All packages support vertical migration across all densities.

<sup>2</sup> TQFP: thin quad flat pack.

<sup>3</sup> FineLine BGA<sup>®</sup> package (1.0-mm pitch).

A minimum die size is achieved by using a pad-limited, staggered I/O pad arrangement, resulting in the lowest cost per I/O pin in the industry. The device is then populated with the maximum number of LEs that fit inside of the I/O ring. The LUT-based architecture delivers the maximum possible logic capability in the smallest I/O-constrained space.



## Board-Management Features

Combined with its low-cost and low-power benefits, the MAX II family incorporates several innovative board-management features such as user flash memory, a JTAG translator, MultiVolt flexibility, and real-time ISP to further reduce the overall system costs.

### User Flash Memory

User flash memory is a user-accessible and programmable non-volatile flash memory block that can save cost and board space by replacing discrete non-volatile memory devices, such as electrically erasable programmable read-only memories (EEPROMs). Typical applications for this feature include storage of board revisions or serial numbers. The user flash memory block can be accessed through the JTAG port or through the core logic.

### JTAG Translator

The JTAG translator allows the user to implement user-specific JTAG commands via the MAX II device core logic, enabling configuration of non-JTAG-compliant devices (such as standard flash memory) on the board. This feature saves board space and simplifies manufacturability.

### MultiVolt Flexibility

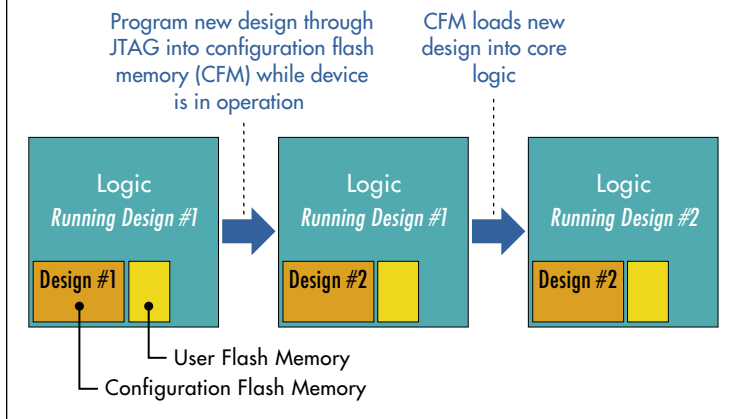
The MAX II architecture supports a MultiVolt core, which allows its operation with a 1.8-, 2.5-, or 3.3-V supply. This feature minimizes the number of power rails and simplifies board-level design.

With the MultiVolt I/O interface, MAX II devices can also seamlessly interface to other devices at 1.5-, 1.8-, 2.5-, or 3.3-V logic levels.

### Real-Time ISP

Real-time ISP helps to reduce maintenance costs by allowing users to change their design while the device is in operation with a previously configured design (see Figure 3 on page 4). This new feature enables quick in-field product updates without requiring the system to be turned off to initiate reconfiguration.

**Figure 3. Real-Time ISP**



### *Ease of Use*

In addition to having new board management features, the MAX II architecture is optimized for ease of use with features such as improved second-time fitting. The MultiTrack interconnect decouples the LABs from the I/O pins, allowing a pin-locked design to have a very high success rate for second-time fitting to accommodate last-minute design changes.

### **Free Design Software**

MAX II devices are supported by Altera's Quartus® II software, the highest-performance and easiest-to-use design software available for CPLD design. Now featuring a built-in MAX+PLUS® II look-and-feel option, MAX+PLUS II users can benefit from the Quartus II software without having to learn a new user interface. The Quartus II software also integrates seamlessly with all of the leading third-party synthesis and simulation tools.

A free version of the software, Quartus II Web Edition, can be downloaded from the Altera web site at [www.altera.com](http://www.altera.com) and is also available on the *Quartus II Software Starter Suite* CD-ROM.

### **Contact Altera Today**

The MAX II CPLD family is the ideal solution for all of your low-cost, low-power logic needs. To learn more about MAX II CPLDs, visit [www.altera.com/max2](http://www.altera.com/max2).



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