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A New Jitter Classification Method Based on Statistical, Physical, and Spectroscopic Mechanisms

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Abstract

This paper introduces a new jitter classification method based on jitter physical mechanisms combined with statistical distribution and spectral properties. The physical jitter properties are first discussed in terms of the source mechanisms, distributions, and spectra. Second, the interrelationship between conventional statistical deterministic jitter (DJ)- and random jitter (RJ)-based jitter separation and classification are studied, and the new physical mechanism-based method is used to establish a mapping relationship that unifies both methods. Third, a new dimension of jitter-component spectroscopy is introduced and combined. Finally, the values and advantages of the new physical and statistical combined jitter classification method, as well as jitter-component spectroscopy are presented.

Author Biography

Dr. Mike Peng Li

As a principle architecture and distinguished engineer at Altera Corporation, Dr. Mike Peng Li is a corporate expert and adviser on jitter, noise, and high-speed link and SERDES architecture. Dr. Li pioneered the jitter separation method (Tailfit); the DJ, RJ, and TJ concept and theory formation; and the jitter transfer function (JTF) concept, theory, and application for high-speed serial link analysis. He is involved in setting and contributing to standards for jitter, noise, and signal integrity for leading serial data communications, including Fibre Channel, Gigabit Ethernet, Serial ATA, PCI Express, and FB DIMM. Currently he is co-chairman for the PCI Express jitter standard committee. Dr. Li has been involved in technical committees for IEEE- and IEC-sponsored technical conferences such as Custom Integrated Circuits Conference (CICC), International Test Conference (ITC), and DesignCon, and is a constant speaker, invited author/speaker, panelist, session, and panel chairs on the subjects of jitter/noise and signal integrity covering both design and test. Prior to joining Altera in 2007, Dr. Li was chief technology officer (CTO) at Wavecrest Corporation, where he developed the technology leadership and vision for the company. He has received many awards, including design paper award from DesignCon/IEC and the contribution award from PCI-SIG. He has been listed in *Who's Who in America* and *Who's Who in the World* since 2006.

Dr. Li has authored or co-authored five books/book chapters on jitter and high-speed I/Os, including the widely distributed and highly ranked book entitled *Jitter, Noise, and Signal Integrity at High-Speed* by Prentice Hall. He has published more than 80 technical papers, holds six patents, and is awaiting approval on eight others. Dr. Li holds a PhD in physics, an MSE in electrical and computer engineering, and an MS in physics, all from the University of Alabama, Huntsville. He also holds a BS in physics from the University of Science and Technology of China. He did his post-doctoral work at University of California, Berkeley, and worked there as a high-energy astrophysicist before joining the industry.

1. Introduction

Before the development of the deterministic jitter (DJ) and random jitter (RJ) concept and theory, jitter was studied and quantified in terms of two common and straightforward statistical numbers, namely peak-to-peak (pk-pk) and standard deviation (SD). However, this parameterization method suffers from two major shortfalls. The first is that in the presence of unbounded jitter such as Gaussian, the pk-pk value of the jitter distribution is a function of its sample size, making the pk-pk a conditional or unstable measure. The second shortfall is that, in the presence of non-Gaussian distribution, multiplying the standard deviation or sigma value to estimate a small probability is inaccurate.

To overcome those shortfalls, the DJ and RJ concept, theory, and separation methods were formed and developed at the end of the 1990s (e.g., [1], [2], [3], [4]). This theory recognizes that there are two fundamentally different components within any jitter distribution, one of which is deterministic with a bounded distribution, the other of which is random with an unbounded or Gaussian distribution. Since DJ is bounded, pk-pk can quantify its distribution with good stability and repeatability. Because RJ is Gaussian, its distribution is characterized by its root-mean-square (RMS) or sigma value, and the Gaussian model extrapolation for smaller probability provides better estimation accuracy and confidence level.

In addition to DJ and RJ components, other jitter components were developed. DJ can include the following subcomponents: data-dependent jitter (DDJ) for lossy medium and data-pattern related jitter, periodic jitter (PJ) for various periodic modulation jitter such as sinusoidal, and bounded-uncorrelated jitter (BUJ) for uncorrelated interferences such as crosstalk and electromagnetic interference (EMI). When the data pattern is a clock, the dominant jitter is called duty-cycle distortion (DCD).

The DJ and RJ concept and theory was later widely adopted by many standards to quantify and specify jitter for high-speed links—including Fibre Channel (FC), Serial ATA (SATA), Gigabit Ethernet (GbE), Optical Internetworking Forum (OIF), PCI Express (PCIe), and Fully Buffered DIMM (FB DIMM)—and has become the de facto method for jitter quantification and analysis in both industry and academia.

The DJ and RJ concept, theory, and separation method carries significant merit in terms of simplicity, better qualification precision, and modeling accuracy at smaller probabilities compared with the statistical parameterization method. However, it is not suited for jitter debug and reduction, as it does not offer necessary and detailed information on the exact physical mechanism and root-causes for the defined jitter components. This is not surprising since the DJ and RJ concept, theory, and separation method first were developed for link-jitter specification and quantification, and not for jitter root-cause identification and reduction. When a high-speed device fails the DJ and RJ testing, the method offers limited help in identifying and reducing the jitter components to make the device pass the test. As the data rate increases to 10 Gbps and beyond, additional jitter reduction and optimization are needed, and advancements of the current DJ and RJ based classification method are in demand.

This paper introduces a new jitter classification method based on jitter physical mechanisms and root causes (e.g., lossy medium, crosstalk, reflection, power-supply noise, phase-locked loop

(PLL)- and oscillator-induced jitter), as well as jitter-component spectroscopy. This new method enhances the DJ- and RJ-based method by including both statistical and physical properties in the classification. After surveying, studying, and quantifying all the fundamental jitter root-causing mechanisms that are critical to high-speed links—including lossy medium-induced jitter, crosstalk-induced jitter, reflection-induced jitter, PLL/VCO jitter, and power-supply noise jitter—each physical jitter is discussed in terms of statistical and spectrum properties. Once the physical jitter properties are understood and quantified, a two-way mapping relationship is established between physical jitter and statistical jitter. Meanwhile, a new dimension of spectroscopy is introduced to the jitter components. Finally, the values and advantages of a unified jitter calcification method that combines both statistical, physical, and spectral properties are discussed.

2. Jitter Root-Cause Mechanisms in a High-Speed Link

The jitter impairments get worse as the data rates increase, because the unit interval (UI) decreases proportionally. The sources of jitter are best illustrated in the context of a serial link, as shown in Figure 1.

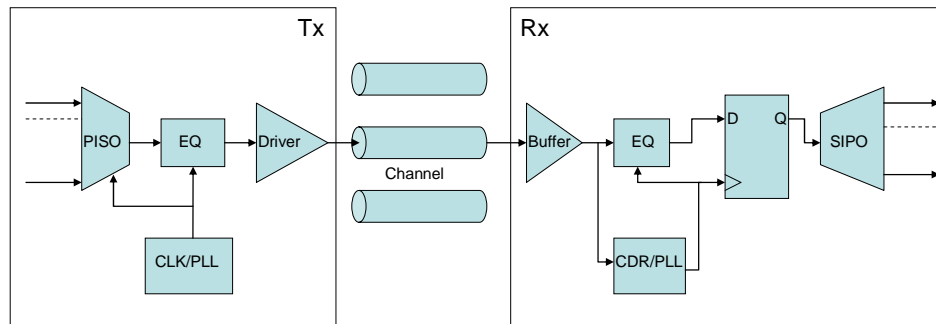


Figure 1. A High-Speed Link System

Within the transmitter (Tx), a parallel-in/serial-out (PISO) or serializer converts multiple parallel lower data-rate lanes to a single higher data-rate lane. An equalization commonly is used to compensate the channel loss. A clock generator, often implemented with PLL circuits, provides the PISO and equalization timing, while a driver provides the necessary voltage level and associated rise and fall times. Tx jitter largely depends on its clock and PLL jitter, especially RJ. The Tx package and parasitic are major sources of DDJ, due to the lossy properties. Reflection-induced jitter between silicon driver and package, and between package and channel can occur if the impedance between them are not perfectly matched. Due to capacitive or inductive coupling, crosstalk can occur on integrated circuits or on the package. For half-rate architecture, both the rising and falling edges of the clock must be used to provide the full data-rate, and the propagation delay between the two edges may cause DCD. Noise on the reference voltage also may cause DCD.

The power supplies needed to operate the PISO, CLK/PLL, EQ, and power-supply noise can be converted to jitter via the coupling. Many different sources contribute to the jitter seen at the output pin of the Tx, so for a given lowest level jitter component (e.g., DCD, intersymbol interference (ISI), PJ, and RJ), there may be multiple root causes possible. For diagnostic and

jitter reduction purposes, it is beneficial if these root causes are well explored and quantified in a systematical manner.

There are at least four different forms of jitter mechanisms for channel-induced jitter. Most electrical-channel materials, such as copper cable, FR-4-based micro-stripe, and stripe-line, are frequency-dependent lossy. Lossy channel and surface roughness are major sources of DDJ at higher data rates. Crosstalk is another source for channel-induced jitter if there is electrical coupling between channels. In addition, the reflections between the channel near-end and far-end with the package of Tx and receiver (Rx) introduce reflection-induced jitter.

Within the Rx, buffer detects the voltage level of the incoming signal. The signal then is sent to clock and data recovery (CDR), which recovers a bit clock from the incoming data signal. In parallel, the signal also is sent to an equalization unit to compensate for the loss due to the channel. The recovered clock uses the clock timing for equalization, data-sampling flip-flop, and as a serial-in/parallel-out (SIPO) or deserializer. CDR commonly is implemented with a PLL, and CDR PLL jitter is a major source for the Rx, particularly for the RJ portion. Reflection-induced jitter arises where there is an impedance mismatch between the channel and the Rx package and integrated circuits. For a multiple-channel transceiver, on-chip electrical coupling at the package or at the integrated circuit causes crosstalk jitter for the Rx. Certainly, the Rx package and parasitic will introduce a certain amount of DDJ. In addition, the power-supply noise for the buffer, CDR, EQ, and SIPO may be coupled to the signal, thus causing power-supply induced jitter.

Each of the following jitter mechanisms for high-speed links has an established mapping relationship with the lowest level jitter components:

- Loss materials (i.e., board level or chip-level interconnects)
- Crosstalk
- Reflection
- PLLs
- Power-supply coupling

(For an overview and basics of jitter and signal integrity in a high-speed link, see [5].)

2.1 Lossy Medium-Induced Jitter

The relationship between the output signal and input signal for a wired transmission medium, such as copper-based circuit board trace or optical fiber, is described by the linear-time invariant (LTI) theory:

$$V_o(t) = V_i(t) * h_m(t) \quad (1)$$

where $V_i(t)$ is the input signal waveform, $h_m(t)$ is the impulse response of the medium, and $V_o(t)$ is the output signal waveform. For an ideal medium (i.e., lossless), $h_m(t)$ is a delta function $\delta(t)$ and the output signal is the same as the input signal, namely $V_o(t) = V_i(t)$, with no signal distortion caused by the lossless medium. When the medium is lossy, its impulse spreads and may cause ripples. A distorted output signal waveform results in ISI, as shown in Figure 2.

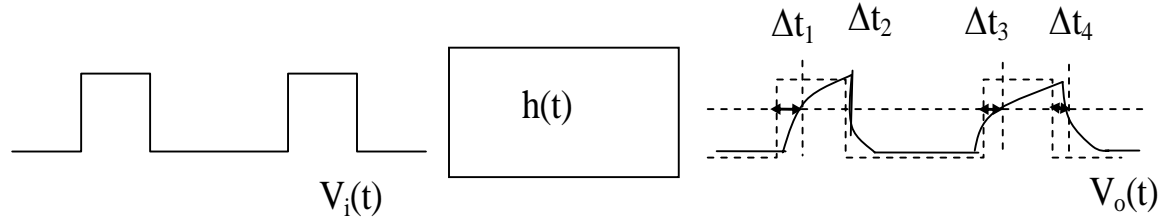


Figure 2. ISI Induced by Lossy Medium

ISI causes both timing jitter (also called DDJ) and amplitude noise. The magnitude of DDJ depends on both the input signal waveform and the medium impulse response. For a digital waveform, the number of the DDJ sample equals the number of edge transitions of a given data pattern. However, the DDJ values may degenerate, as there are several identical edge transition sub-patterns (e.g., 00100) for any given DDJ. Due to the discrete nature, the DDJ probability density function (PDF) may be quantified by the comb function:

$$f_{DDJ}(\Delta t) = \sum_{i=1}^N P_i \delta(\Delta t - DDJ_i) \quad (2)$$

where P_i is the probability for DDJ_i value and DDJ_i is the i th DDJ value. When the data pattern is a clock, the DDJ becomes DCD jitter, because no ISI is associated with the clock pattern by definition.

When the data pattern repeats in a looping mode, the DDJ frequency is the integer multiple of the fundamental pattern frequency, namely $f_{patt} = (1/(2 * L_{patt} * UI))$. Thus, the lowest DDJ frequency is the f_{patt} . For a K28.5 test pattern, $L_{patt} = 20$, and $f_{patt} = f_{Nyquist} / 20$. At a data rate of 10 Gbps, $f_{Nyquist} = 5$ GHz, and $f_{patt} = 250$ MHz for K28.5 pattern, all with high-frequency jitter. For a longer pattern, f_{patt} extends to the low-KHz frequency range. For a clock pattern, the DCD jitter occurs on a per UI basis, namely at $f_{Nyquist}$. Obviously, the DCD frequency is higher than the DDJ minimum frequency f_{patt} . These basic and important properties establish the jitter component spectroscopy concept.

2.2 Crosstalk-Induced Jitter

Crosstalk jitter has been studied intensively in recent years [5]. The most common coupling mechanisms for crosstalk are capacitive and/or inductive coupling. When the aggressor data bits are uncorrelated to the signal data bits, it has been shown that crosstalk jitter PDF follows the central-limiting theorem [6] [7]. That is, when the number of aggressors increases, the PDF follows the Gaussian shape but with a bounded pk-pk. Such a distribution is also called a truncated Gaussian:

$$f_{CJ}(\Delta t_i) = \begin{cases} \frac{P_{CJ}}{\sqrt{2\pi}\sigma_{CJ}} e^{-\frac{\Delta t_i^2}{2\sigma_{CJ}^2}} & \text{for } |\Delta t| \leq CJ_{PK} \\ 0 & \text{for } |\Delta t| > CJ_{PK} \end{cases} \quad (3)$$

where P_{CJ} is a normalization probability coefficient, σ_{CJ} is the sigma value for the truncated Gaussian, and CJ_{pk} is the peak value for crosstalk jitter. Note the discrete nature of the crosstalk jitter PDF (Figure 3): when the number of aggressor increases, the line density and number of distribution lines increase.

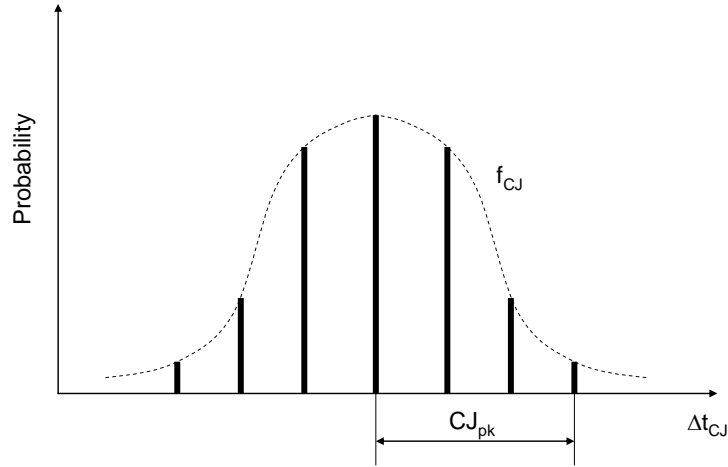


Figure 3. PDF Distribution for Crosstalk With a Large Number of Aggressors

Crosstalk PDF approaches the Gaussian shape when the number of aggressors becomes very large. By analogy, its power spectrum density (PSD) approaches white. The highest frequency is at Nyquist, because crosstalk can occur on an aggressor UI. The low-frequency cutoff depends on the number of aggressors, as the larger the number of aggressors, the lower the crosstalk jitter spectrum will be.

2.3 Reflection-Induced Jitter

Although the physics of reflection has been well established since Maxwell, the jitter PDF and spectral properties due to reflection are still less explored compared to other jitter mechanisms. This may be due to the complexity of reflection in practical high-speed links. Figure 4 illustrates a simple reflection model for a high-speed link.

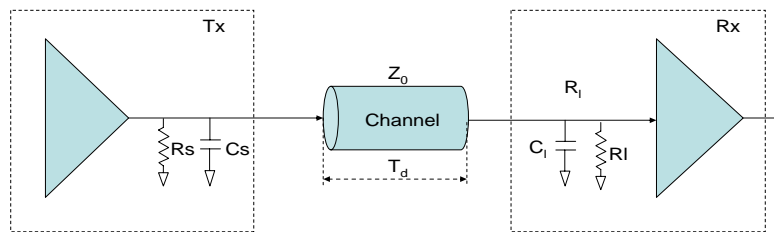


Figure 4. A Model of a Reflection Mechanism for a High-Speed Link

Reflection can occur at the boundary between the source (Tx) termination and the channel input, and between the channel output and the load (Rx) termination. The reflection coefficients at the source and the load are [5]:

$$\rho_s = \frac{Z_0 - Z_s}{Z_0 + Z_s} \quad \text{and} \quad \rho_l = \frac{Z_l - Z_0}{Z_l + Z_0} \quad (4)$$

To illustrate the insights for reflection, the termination resistances for source, load, and channel impedance are assumed to be equal, with equal source and load shunt capacitances:

$$\rho_s = \frac{s\tau}{1+s\tau} \quad \text{and} \quad \rho_l = -\rho_s \quad (5)$$

where $\tau = (Z_0C)/2$. The reflection coefficient in this case has a high-pass property, in that the high-frequency contents of the signal reflect more than low-frequency contents. Since the highest frequency contents correspond to the edge transition, the significant reflection occurs if the rise and fall times are fast.

Assume that a step response $S_0(t)$ is launched to the channel input. At the channel output, the reflected signal is round-trip delayed relative to the original signal. The reflected pulse (or first echo) occurs at $t-2T_d$, the second echo at $t-4T_d$, the n th echo at $t-2nT_d$, and so on, where T_d is the transport delay for the channel (see Figure 4). According to Equation (4), the magnitude of each echo decreases as its number index increases. To illustrate how the reflection induces jitter, Figure 5 illustrates a reflection-induced jitter mechanism under the following assumed conditions: the transport delay of the channel T_d is equal to the pulse width for the clock.

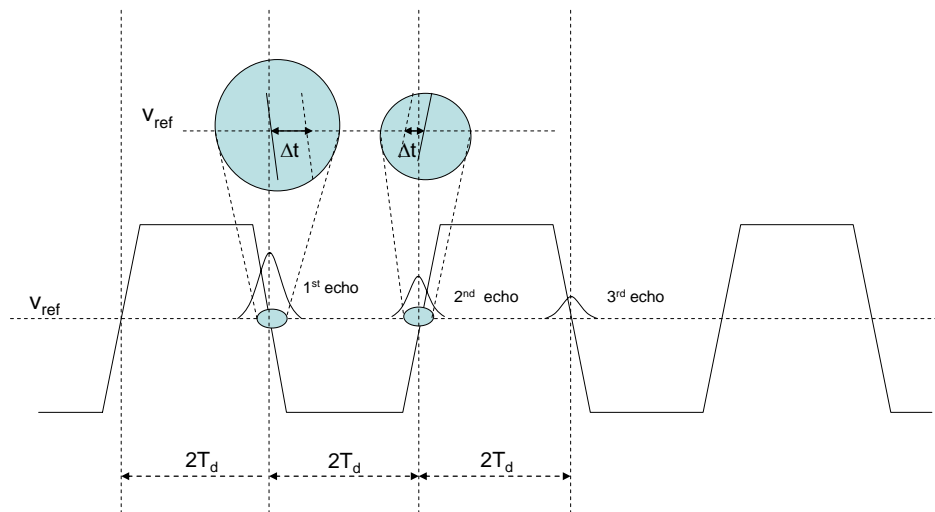


Figure 5. Reflection-Induced Jitter Mechanism

Note that this is an intuitive showing of the reflection jitter mechanism under special conditions. These conditions are relaxed by considering the overall data pattern, the arbitrary relationship between transport delay T_d and UI for the data pattern, all of the edge transition echoes (not just that from the first edge transition), and the termination RC time constant (which affects the echo pulse shape and width). The possibilities for the reflection-induced jitter PDF shape virtually are unbounded, ranging from bimodal (shown in Figure 5) to a close truncated Gaussian due to a central limiting theorem [8],[9].

Reflection-induced jitter should be added to the classical jitter component tree as a new component since its mechanism is different from lossy medium-induced DDJ and crosstalk jitter. Since the acronym RJ has been taken by random jitter, this paper uses the term "echo jitter" (EJ) for reflection-induced jitter.

2.4 PLL Jitter

Since PLLs [10],[11],[5] are used for both Tx clock generation and Rx CDR, PLL jitter plays an important role in determining high-speed transceiver jitter performance. Figure 7 shows the PLL system block diagram and the jitter and noise mechanisms.

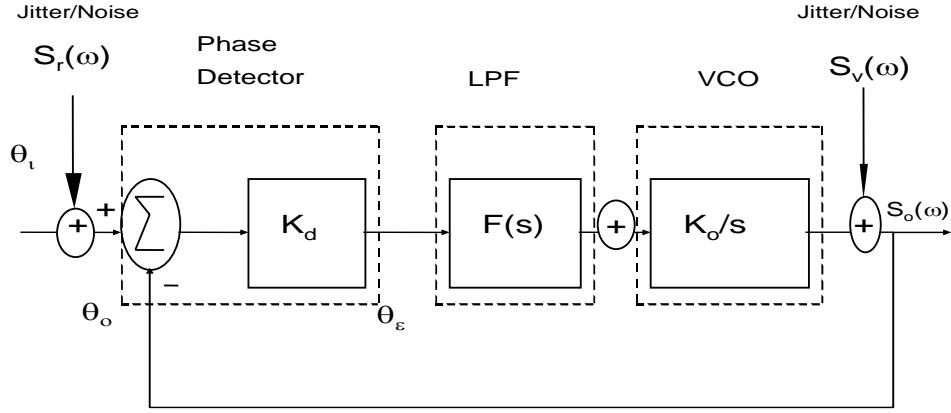


Figure 7. A PLL System and Noise Model

Although PLLs potentially can generate jitter and noise, jitter and noise from the reference clock (quantified by its PSD $S_r(\omega)$) and noise from the VCO (quantified by its PSD $S_v(\omega)$) tend to be more dominant [5]. In this case, PLL output jitter PSD is a function of the reference clock jitter PSD, the VCO noise PSD, and the PLL transfer functions:

$$S_o(\omega) = \left[S_r(\omega) |H_r(s)|^2 + S_v(\omega) |H_v(s)|^2 \right]_{s=j\omega} \quad (6)$$

$$\left[S_r(\omega) \left| \frac{K_d K_o F(s)}{s + K_d K_o F(s)} \right|^2 + S_v(\omega) \left| \frac{s}{s + K_d K_o F(s)} \right|^2 \right]_{s=j\omega}$$

Because $F(s)$ is a low-pass function (LPF), the first term associated with the reference clock is a LPF, and the second term associated with VCO is a high-pass function (HPF). When the reference clock is the dominant jitter source for the PLL and is white, then the PLL output jitter is limited to low-frequency white RJ. In this case, decreasing the PLL bandwidth decreases the PLL jitter. Similarly, when the VCO jitter is the dominant jitter source for the PLL and the reference clock jitter is white, then the PLL output jitter is band-limited high-frequency RJ. Therefore, increasing the PLL bandwidth reduces the PLL output jitter [12].

The PLL jitter spectrum can have both spurious PJ and RJ. In the absence of PJ in the PLL output jitter spectrum, the PLL jitter PDF is Gaussian. If both PJ and RJ are important, then the PDF for the PLL output jitter is a convolution of PJ “U”-shape PDFs with Gaussians.

2.5 Power Supply-Induced Jitter

Power-supply noise for timing-critical devices such as PLLs becomes important at higher data rates. An important mechanism for noise-to-jitter conversion is voltage noise-to-frequency variation conversion via the VCO tuning curve, as shown in Figure 8.

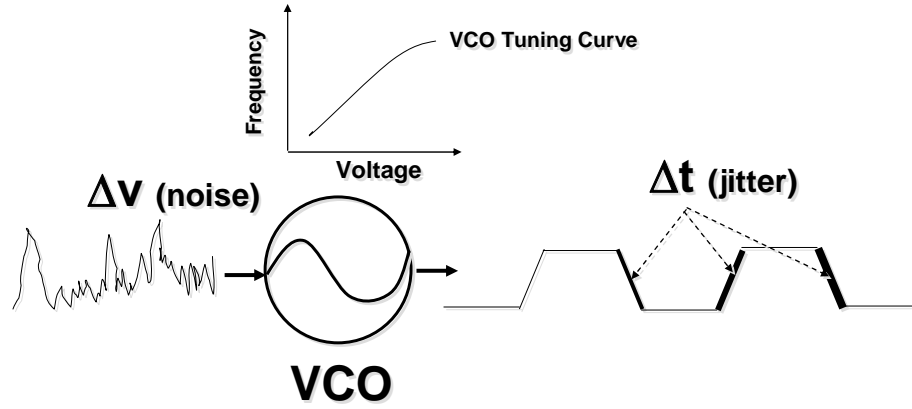


Figure 8. A VCO Jitter Mechanism

Jitter, phase change, and frequency change are interrelated:

$$\Delta t = \frac{\Delta \phi}{2\pi f_0} = \frac{\int_0^t \Delta f(t) dt}{f_0} \quad (7)$$

where Δf is the frequency deviation due to the voltage noise Δv , and

$$\Delta f = \Delta v \cdot \frac{df}{dv} \quad (8)$$

where $\frac{df}{dv}$ is the slope for the VCO tuning curve.

To reduce the power-supply noise, precise and dedicated voltage supplies and regulators are needed for a VCO within a PLL, with a good power-supply rejection ratio (PSRR). The spectrum of the supply induce jitter at the VCO output depends on Equations (7) and (8): If the power-supply noise is white, then the jitter at the VCO output is low-pass filter spectrum due to the integration relationship of Equation (7) [12].

3. New Jitter Classification Scheme

With the knowledge and understanding of the physical jitter properties in terms of statistical distribution and spectrum, a new jitter classification method—combining statistical, physical, and spectral properties—becomes possible.

For Figure 9, note that in addition to the mapping between the physical jitter and statistical jitter, a new DJ component, EJ, is established to overcome the shortfalls discussed in Section 1. (EJ due to reflection is overdue with the statistical jitter classification method, yet it is necessary as EJ becomes severe at high data rates.) In addition, another jitter component, pulse width jitter (PWJ) ([13],[14],[5]), is introduced as a sub-class for DDJ. Finally, DCD is added as a standalone DJ component since it is only good for clock patterns.

With this new statistical and physical unified jitter classification scheme, it is possible to quantify physical jitter, in addition to statistical jitter components, and to match them to achieve solution closure. In other words, for each statistical jitter component, it is possible to pinpoint exactly how much is due to each related physical mechanism. Such information is very critical and important for jitter diagnostic and reduction, which is critical as data rates increase to 10 Gbps and beyond.

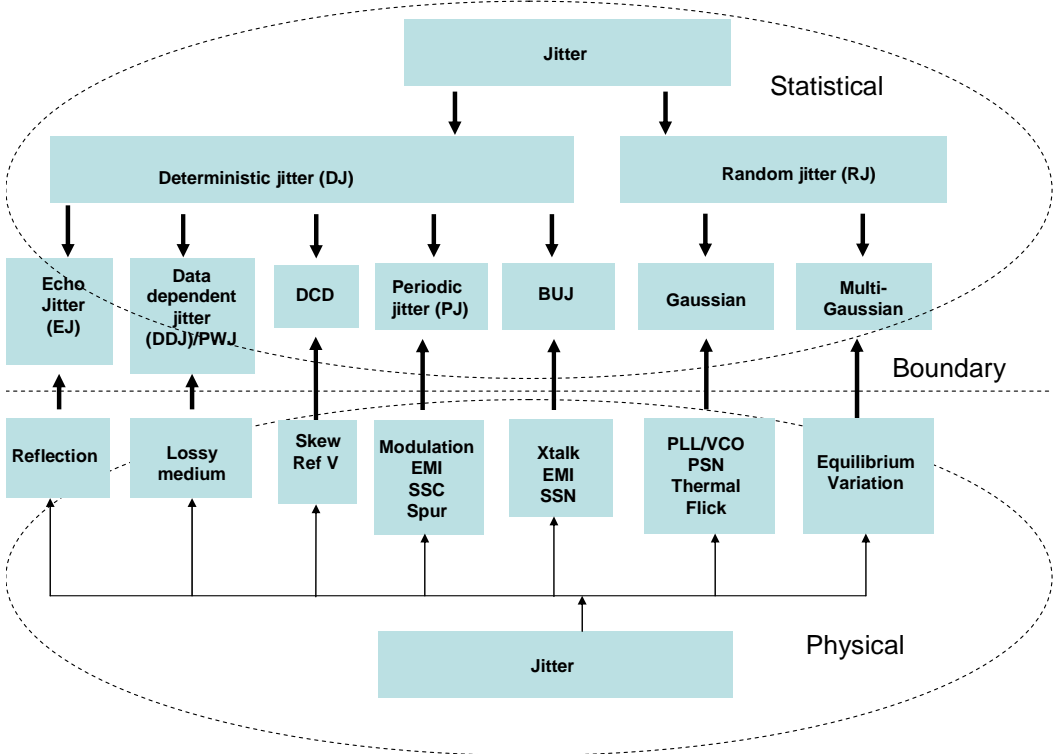


Figure 9. A New Jitter Classification Scheme That Unifies Statistical Jitter With Physical Jitter

Figure 10 illustrates jitter-component spectroscopy by combining each statistical jitter component with its corresponding spectral properties.

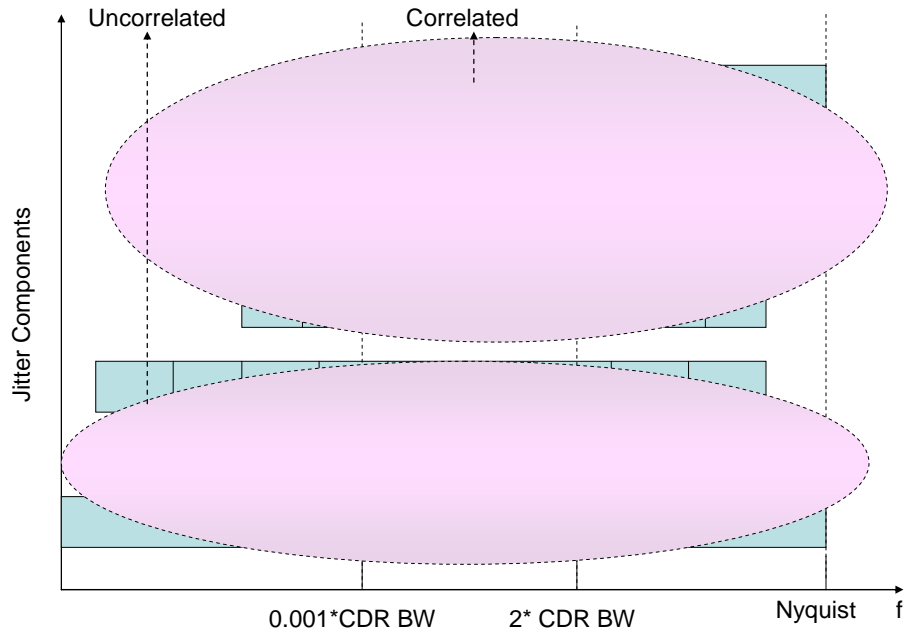


Figure 10. Jitter Component Spectroscopy

In Figure 10, the Nyquist frequency is half the data rate. The CDR bandwidth is commonly set at a frequency equal to the data rate divided by 1667. Most of the 10-Gbps CDRs have their bandwidths at around 1–10 MHz. The low frequency is commonly defined as ~1 KHz, which is in the range of wander frequency. RJ is broadband and continuous from KHz to Nyquist. BUJ caused by both crosstalk and EMI can be discrete and/or continuous. While BUJ frequency can be as high as Nyquist, its low-frequency end may not be as low as that of RJ since it is bounded, suggesting a narrower frequency range. PJ is discrete, and phase or frequency modulation constraints typically limit its higher cutoff to below Nyquist. The highest frequency for DDJ is the data-pattern repeating rate, which is a fraction of Nyquist. EJ can repeat with a pattern, so its frequency can be higher than that of the pattern frequency, and as high as Nyquist. PWJ measures the deviation of a pulse width (i.e., time distance between a rising edge and the consecutive/next falling edge) from ideal. Thus, PWJ can happen from a fraction of Nyquist to Nyquist itself. DCD happens within a clock cycle, either for positive pulse or negative pulse. However, due to the existence of half-rate and quarter-rate clocks in addition to full-rate clocks, DCD can span from a fraction of Nyquist to full Nyquist. Obviously, DCD and PWJ are high-frequency jitter, EJ is can be referred from high frequency to mid-range frequency, DDJ is the mid-frequency jitter, and broadband RJ, BUJ, and PJ span low frequency to high frequency.

PJ, BUJ, and RJ are uncorrelated so that their mid- and lower-band frequency contents can be tracked by clock recovery, leaving only the high-frequency jitter contributing to the system bit error rate (BER). DDJ is correlated and can be corrected to some extent with equalization. EJ is partially correlated to data pattern, but also depends on the resource-channel transport delay and reflection coefficients, so CDR tracking has little effect on EJ. DCD and PWJ are partially correlated and are hard to correct at the receiver side due to their near-Nyquist frequency characteristic. DCD and PWJ must be bounded at the transmitter side to insure their interoperability.

Figures 9 and 10 reveal the inter-relationship between statistical, physical, and spectral properties for the jitter component or mechanism. This new unified and complete jitter classification method offers significant advancements for understanding, quantifying, diagnosing, and reducing jitter-related design, simulation, and validation over the current/old method solely based on jitter statistical properties.

4. Summary

This paper reviewed the physical jitter mechanisms that are critical for a high-speed link, including lossy medium-induced jitter, crosstalk-induced jitter, reflection-induced jitter, PLL/VCO jitter, and power supply-induced jitter. With the statistical and spectrum properties of these physical jitter mechanisms, a new jitter classification method that unifies statistical jitter, physical jitter, and jitter spectroscopy concurrently is established. The new method overcomes the shortfalls of the old/current jitter classification schemes based solely on statistical properties. The new method reveals the fundamentals of jitter statistical, physical, and spectroscopic properties and mechanisms in a simple and unified view, enables a new way to achieve simultaneous jitter quantification and root cause finding, and provides guidance for jitter reduction and optimization for jitter-related design, simulation, and validation.

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