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Analysis of FPGA PDN Noise Propagation by Die & Package 3D Modeling

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Abstract

This paper describes a systematic approach for FPGA die/package PDN model extraction and correlation. A full chip PDN model was developed for analyzing on-chip PDN impedance and noise propagation on power grids. A distributed package model was attached for an integrated modeling to simulate PDN interaction between die and package. Time and frequency domain simulations of die and package PDN noise are performed and compared with lab measurements.

Author Biographies

Zhe Li is a senior engineer at Altera Corporation, focusing on package design and technology development. Currently, he works on modeling and prediction of jitter in FPGAs and die/package PDN noise analysis. His interests include EMC/EMI, system-level measurement techniques and electromagnetic modeling of power distribution networks. He has published over 10 papers and has several patents pending.

Dr. Hong Shi is the Design Engineering Manager of Altera Corporation. He is responsible to engineering design across charters of new and extension product development, new packaging technology implementation, design for performance, and assessment methodology by modeling, simulation and characterization. Dr. Shi has 14 years of industry and research experience in field of optoelectronics, optical fiber communication, microwave circuits and digital circuit packaging. He has published more than 50 technical articles and 10 patents in the related field. Dr. Shi is a frequent speaker in various die-package-system co-design seminar and international technical forums.

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Dr. John Y. Xie has been with Altera for 10 years. He currently serves as a senior package design engineering manager in charge of IC-Packaging interconnection technology solution engineering and design solution engineering. Prior to Altera, he spent 5 years with Prolinx Corporation, an advanced interconnection technology company, as technology development manager. Dr. Xie holds a Ph.D. Degree in Physics. He spent 4 years of Post Doctoral research at Dept. of Physics, University of California at Berkeley. Dr. Xie's expertise and interests include advanced interconnection technology, IC packaging material and process technology, design engineering and signal integrity, IC-Package-PCB co-design engineering and process integration. Dr. Xie holds 23 patents and over 40 publications.

Hui Liu is a leading signal, power, and timing integrity engineer in die-package-PCB co-design responsible for high-speed and high-bandwidth serial and parallel interface designs in Packaging Technology at Altera Corporation. Prior to Altera, Hui worked as a system design engineer on the metro-router platform at Cisco Systems. Hui has more than 10 years of experience in variety of industries and holds multiple patents on signal and power integrity methodologies and designs.

Richard Chen received his B.S. and M.S degree of Electrical Engineering before joining Altera Corp. in 1998. Currently he's a Member of Technical Staff focusing on FPGA characterization. He is responsible for performance characterization of subsystems of FPGA such as memory interface, LVDS, IO, PLL, etc, especially under PDN noise and SSN.

I. Introduction

On-chip power integrity is an area of increasing concern in deep submicron technologies [1, 2]. With increasing clock frequency, lower voltage level and higher logic integration density, accurate modeling and simulation of on-chip power delivery network (PDN) is becoming critical for VLSI circuit designs. The on-chip PDN typically has an power and ground grid structure, commonly referred as power grids.

Traditionally, power grid design is focused on DC IR drop, power and electromigration (EM) analysis. DC IR drop is a static voltage drop that is developed on the power grids with a time-averaged current over several clock periods. PDN noise is dynamic voltage fluctuations. The switching activities in the CMOS devices inject high-frequency currents into the power grids and create large PDN noise. Such noise can cause signal timing variations and degrade circuit performance, especially in noise-sensitive circuits such as phase-locked loops (PLLs) and clock distribution networks [3, 4].

Several approaches can be taken to minimize or eliminate these problems, such as adding on-chip decoupling (OCD) capacitors and allocating more wiring resources to power grids in terms of metal layers, pitch and wire widths. OCD works as an on-chip charge reservoir for load circuits. For immediate charge access, package and PCB do not offer an effective delivery path because of their high loop inductance. OCD sizing and placements within the power grid is extremely important. Without of a proper PDN design, adding OCD may not help reducing the power noise, but becomes a waste of the die area or even causes an IR drop issue as OCD also raises the die leakage currents. This highlights the needs of noise current estimation, on-chip decoupling strategy, power grid modeling and PDN noise analysis.

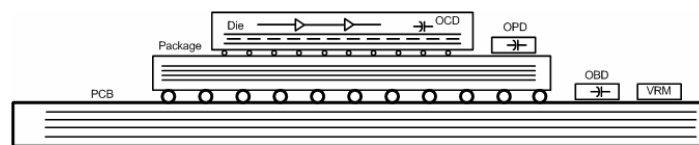


Figure 1. Entire PDN system with all the major components on die, package and PCB. With the flip-chip technology, device substrate is on top of the power grids and connected with package through C4 bumps. Package and PCB power planes are connected vertically through PTHs and BGA balls and vias.

In terms of PDN design and verification, EDA tools lag significantly behind the silicon fabrication process. One of the challenges that designers have to face is the huge size of design and process database. Lumped circuit modeling has been used for system PDN noise analysis with a high-level of abstraction of on-chip circuits and the power grids [5]. This method has been proved to effective for predicting the system parallel resonance with die capacitance and package to PCB inductance. Semiconductor devices keep getting larger and faster and on-chip distributed effects become significant. To ensure proper analysis of the PDN noise, full-chip modeling of the power grid interconnects needs to be developed.

As shown in Figure 1 of the devices with flip-chip technologies, the connection between the chip and the package is more closely related. Package power and ground planes become a direct path for noise propagation through C4 (controlled collapse chip connect) bumps connecting with the on-chip power grids. To truly reflect the noise propagation effects through the die and package, co-simulation of the entire power delivery system must be developed with accurate parasitic representation of the power grids and integrated with the package and PCB modeling.

Another challenge in full chip PDN noise analysis is to construct a distributed noise current model correlated with switching activities of active circuits. Given the size of VLSI designs, full-chip simulation for the switching currents is computationally prohibitive. To circumvent this problem, several methods have been proposed [6], based on standard cell characterization. Full chip simulation is driven with vector or vectorless inputs to identify the switching modes of the active cells. These methods provide a general guideline for estimating an upper bound of the noise currents with the full-chip operations. Simulating for all the mode conditions and vector space in a real design is almost impossible, as it takes too much computation resource.

This paper presents a full-chip PDN noise analysis on a FPGA device. FPGA is made for prototyping and supports a wide range of applications. With FPGA, we can control the design implementations and noise current generation. The rest of this paper is organized as follows. Section II introduces the power grid structure on FPGA devices and power grid modeling. Section III discusses the on-chip capacitance extraction through modeling and measurements. Section IV provides FPGA architecture and its current characterization. Section IV presents the PDN die and package co-simulation and measurement results. Section V concludes the paper with a brief summary.

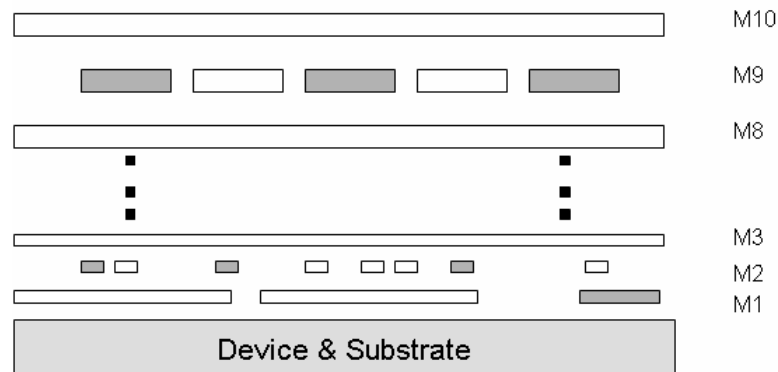


Figure 2. Cross-section view of the FPGA power grids with alternating power (Grey) and ground (blank) wires. Toward lower level metal layers, power and ground wires are more segmented with irregular shapes and non-coupled wires.

II. FPGA Power Grid Modeling

Figure 2 shows a pictorial view of the FPGA power grids that has 10 metal layers on top of a silicon substrate. In each layer, power and ground wires run parallel to each other. The power and ground wires in adjacent layers are connected through vias. The on-chip PDN is connected to the package power and ground planes through C4 bumps. FPGA power grids can be categorized into two level power distributions:

1. Global distribution on top layers that are distributed uniformly over the chip area with wide and alternating power and ground wires (M6 to M10). In these layers, power and ground grids have certain regularities with long horizontal and vertical wires of the same widths. The pitch between two coupled power and ground wires is identical.
2. Local power distribution on lower metal layers with short power and ground wires for power distribution within local logic blocks (from M5 and below). M1 and M2 are used to connect with the transistor power and ground nodes. Toward the lower metal layers, the power and ground wires tend to be more segmented with irregular shapes and non-coupled wires.

Power grid is modeled as a linear passive network consisting of resistance, inductance and capacitance (RLC) elements. Figure 3 shows an equivalent RLC circuit for a regular power and ground grid. Circuit topology is developed from transmission line PI model. Extraction is carried out on via-to-via metal segments including vias from layer to layer connections. Vias are modeled as resistive elements in the equivalent circuit due to their small geometry sizes. Skin effects are not considered as a strong factor in the power grid modeling because the skin depth almost always exceeds the wire thickness and via diameters. Mutual L is included for close coupled wires.

When the power grids get filled with T-junctions, bends and wires with varied width, electrical properties of these structures can be very complicated and its RLC equivalent circuit can only be characterized with a 3D electromagnetic field distribution analysis. Inductance extraction has traditionally been neglected for resistance dominant power supply networks. The significance of power supply noise due to inductance of the on-chip interconnects is shown to increase with technology scaling and larger chip sizes [7].

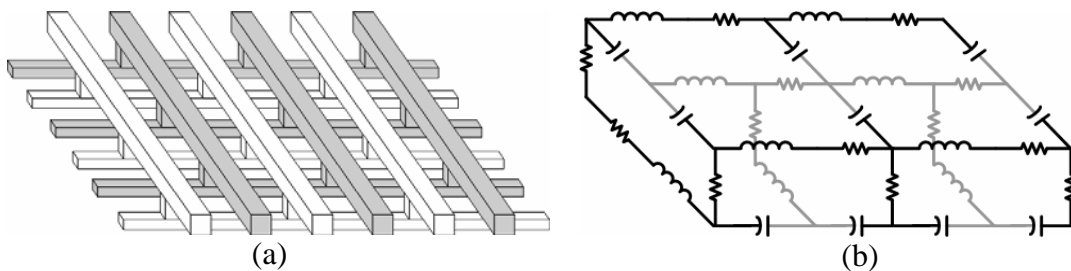


Figure 3. Power grid modeling. (a) Power grid segment. (b) Power grid equivalent circuit. Circuit topology is based on multi-conductor transmission line model. R, L, and C are extracted for each via-to-via wire segment. Via is modeled as a resistive element. Mutual L is also included (not shown in the model).

Extensive research has been devoted to the model extraction of full-chip power-grid interconnects [8]. A number of EDA tools are available for power grid model extractions. EDA developers are trying to provide full-chip solutions with a balance of capabilities and efficiencies. In these EDA tools, we believe that a combination of electromagnetic field solvers and analytical formulae are implemented to extract the power grid parasitics. Extraction is based on reusable power grid segments, building an equivalent circuit library and then progressing in steps to a full-chip model.

We used XcitePI from Sigrity for the power grids modeling on this FPGA device. Figure 4 shows the data flow in the tool including the PDN time and frequency domain simulations. The first step for model extraction is to create the power grid geometry from the layout and process database. An input of GDSII file is processed through the tool, flattening the GDSII hierarchical layout and building the 3D power grid geometry. Combined with a technology file that defines the layer thickness, stack-up, and material properties, the 3D geometry file is processed through the extraction engines, which generate the RLC parasitics for the power grid. The die size of the FPGA device is 18mm x 18 mm, the total GDSII file size is 4.7 gigabytes, the peak memory usage for the power grid extraction is 57 Gbytes, and the CPU run time is about four days on a 64 bit workstation.

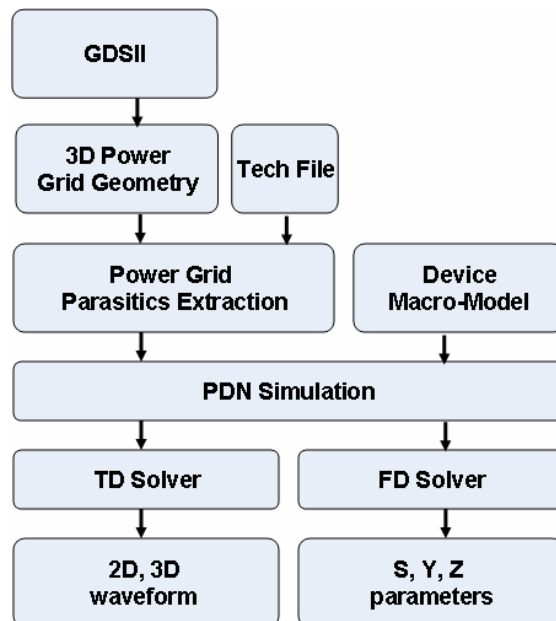


Figure 4. Data flow in PDN noise simulations

III. On-Chip Capacitance Modeling and Measurements

On-chip capacitance serves as an immediate charge access for load circuits. On-chip capacitance includes the power grid parasitic capacitance, and also the capacitance from on-chip devices. There are two portions of the device capacitance, one of which is device intrinsic capacitance from non-switching circuits. Figure 5 shows a typically CMOS inverter circuit with gate-to-source, -drain and -body capacitance (lumped as C_{PG} and C_{NG}), as well as the diffusion capacitance on drain and source (C_{PW} and C_{NW}) through the well resistance (R_{PW} and R_{NW}). The transistor gate capacitance has a resistive path to either power or ground depending on the inverter logic states. Effectively, it can be reduced down to one RC circuit when merging different branches of the entire circuits. The intrinsic capacitance in the device is uniformly distributed across the power grids. Compared to ASIC, FPGA is equipped with much higher intrinsic capacitance as there are considerably more memory, configuration and redundant logics in FPGA to ensure its programming and routing capabilities. The other part of the device capacitance is from on-chip decoupling (OCD) capacitors which are normally planted to protect noise sensitive circuits. The on-chip decoupling capacitors are typically formed with thin-oxide gate capacitance and n-well diffusion capacitance.

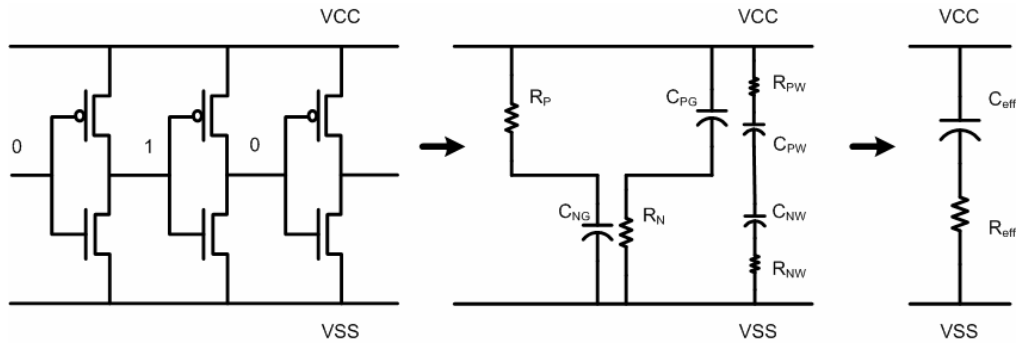


Figure 5. Device intrinsic capacitance within non-switching circuits. Gate capacitance connected to the power supply depends on the circuit logic states.

Device capacitance has a larger impact on the PDN noise as it typically has a much higher value than the power grid wire capacitance. Modeling of the device intrinsic capacitance can be very complicated as the capacitance also involves with the device operations – drawing charges as a load from the power supplies when they switch and providing charges as local decoupling capacitors when they are not switching. The amount of capacitance from switching circuits can be calculated from the average power consumption measurement, $C_{sw} = \frac{P}{V^2 f}$, where f is the switching frequency, P is average power consumption (not including the power consumption from leakage currents), and V is the power supply rail voltage.

Total device capacitance for this study is derived from another measurement. Vector Network Analyzer (VNA) has been used to perform die capacitance characterization [9]. S21 insertion loss in this study was measured on the FPGA power and ground pins in a packaged product. Figure 6 shows the S21 curves under bias and no bias conditions. The

bias voltage is nominal power supply rail voltage, 1.1V. Die capacitance dominates the impedance at lower frequencies. From the S21 results, die capacitance can be extracted.

$$Z_{21} = 25 * \frac{S_{21}}{1 - S_{21}}$$

$$C_{total} = \frac{1}{2\pi f * IM(Z_{21})}$$

As seen from the S21 results, device capacitance on the power supply varies with its bias voltages. When the device is under no bias condition, P and N FET channels are off and the measured capacitance mainly comes from device diffusion capacitance. When the device is fully biased, part of the gate capacitance is connected to the power grids through P FET channels and contributes to the total device capacitance.

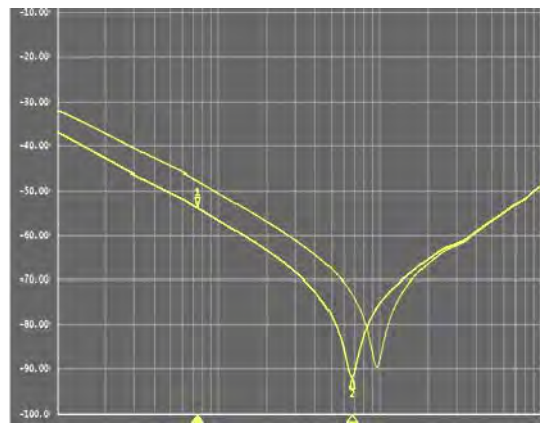


Figure 6. VNA S21 insertion loss measurements on core power supply with bias and no bias voltage on the device. Under bias condition, S21 is lower and more capacitance is measured on the power supply pins.

The VNA measurement is to get the total capacitance on the power grids including the power grid wire capacitance, and the device capacitance from switching and non-switching circuits. The wire capacitance is obtained from power grid RLC extraction based on wire size and spacing between wires. Capacitance from switching circuits is captured from C_{sw} . Subtracting these two from the total device capacitance provides the decoupling capacitance on the device. Resistance of the device capacitance can also be extracted from the real portion of the S21 results. R and C together represent the characteristic of a silicon process. For this FPGA device, R is measured at about 1.5mΩ and C is 351nF. The RC constant for this device is 450ps.

Here we described a general procedure for power grid modeling and device capacitance extraction from measurements. Device capacitance from non-switching circuit is then attached over the chip area onto the power grid for a full-chip PDN noise analysis.

IV. FPGA Switching Currents

4.1 LE Architecture and Current Characterization

Current signature on a FPGA device depends on the logic implementation and the FPGA architecture. The smallest unit of logic in FPGA architecture is a logic element (LE). FPGA consists of rows and columns of LEs with configurable routing that makes connections between them. Figure 7 shows a generic FPGA Logic Element. Each LE contains a Look-Up Table (LUT), an adder, and a wide-functional DFF with associated inputs, clocks, and control signals. To the left is the fabric routing that includes the routing channels and switches connecting signals to the LE inputs. This LE architecture can support a wide variety of functions such as counters and adders with registered or un-registered outputs. As a test case, a typical LE-based test pattern is implemented and the test pattern is repeated on each LE and populated throughout the device.

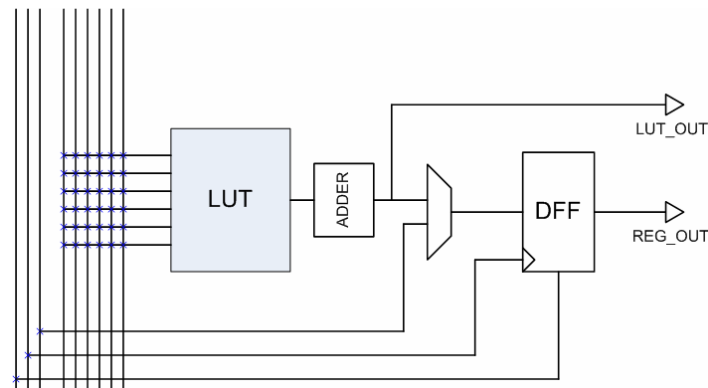


Figure 7. General architecture of a FPGA Logic Element

A key assumption in this analysis is that within each of these LE blocks all distributed effects accounted for by the field solver are negligible. We assume noise currents injected from LE switching transistors can be lumped to one single port in the global power grid. Within the LE block area, the power supply voltage is uniformly distributed and remains constant at each simulation time step. Another assumption is that currents drawn by LEs do not change significantly with power supply noise. Each LE can be modeled as an independent current source.

Switching currents from LE is characterized from SPICE simulations based on LE configurations and its switching activities, as shown in Figure 8. Delay time and signal transition time is also captured in the SPICE simulation. The total LE current waveform is the sum of each sub-block current based on the LE configurations. LE currents also depend on the input data patterns which determine the switching activities of the logic blocks. Following the data path, sub-block currents add up in time from its delay information.

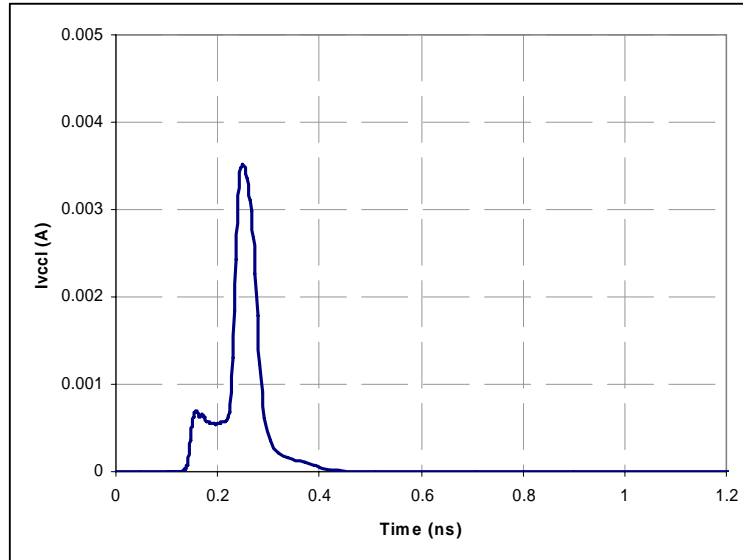


Figure 8. LE switching current profile

4.2 Clock Distribution Networks

FPGA clocks represent a significant portion of the switching currents with their high switching activities and wide spread distributions. This FPGA device has 16 global clock networks and 16 regional clock networks. As shown in Figure 9, each global network can drive through the entire device, and regional clock networks provide clocks within the quadrants down to each logic element. SPICE simulation is carried out to model the switching currents from each type of clock buffers. Timing and clock distribution is modeled and simulated in Quartus® with details of the clock network designs. Follow the clock distribution path, clock currents add up in time based on its delay information in the clock distribution networks.

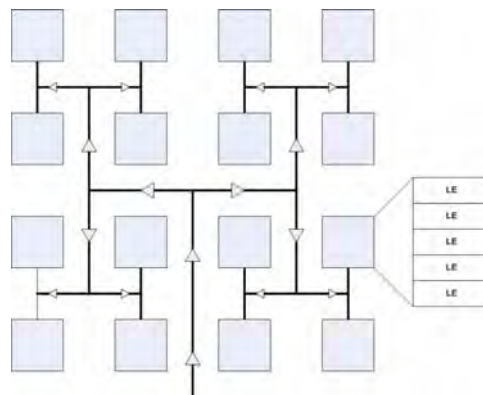


Figure 9. FPGA Clock Distribution

Here we described a general approach for FPGA switching current analysis and model development. Active LEs and clocks as independent current sources are then attached in time and space onto the power grids, from which on-die voltage 2D and 3D waveforms will be developed in the following chapter.

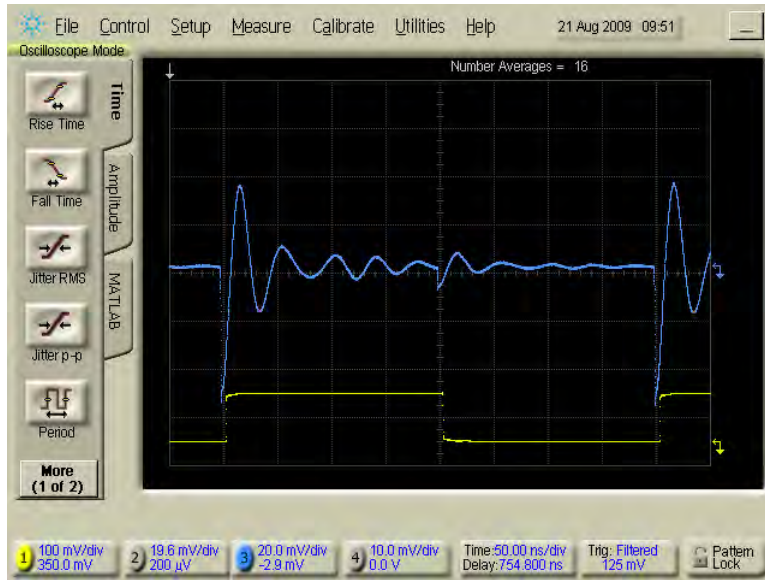
V. Die-Package Co-Simulation and Correlation

4.1 Time Domain Simulation

Three tools are used for time domain die and package co-simulation. On-chip PDN noise is simulated using XcitePI with the distributed current sources, device capacitance and full power grid model. Co-simulation of package is carried out simultaneously in SPEEDXP with Co-Design Studio interfacing between the two solvers. The package used in the FPGA device is a 40mm BGA constructed of 10 metal layers. Die and package simulation is synchronized in each time step with their data passing through Co-Design studio and updated between the two computation domains. Co-simulation of the IC and package includes all of the dependent physical characteristics between the die and the package. It becomes very time consuming if including the complete PCB geometry in the time domain simulation. To save the modeling and simulation efforts, PCB portion of the PDN is simplified with a low frequency equivalent circuit. The primary contribution of PCB to the on-chip PDN noise is the PCB inductance. The PCB components physically and electrically locate far from the on-chip switching circuits and do not impact the high frequency PDN response.

Figure 10 shows the time-domain measurements and simulation results of on-chip PDN noise in a similar setup with the FPGA die, package and PCB. The noise waveform is measured with a DCAJ 50GHZ sampling module and a high frequency Ground-Signal microprobe tapped on a pair of package power/ground sense lines. The power/ground sense lines in this package are designed to monitor the on-chip PDN noise. The FPGA device is loaded with the LE based design as described previously.

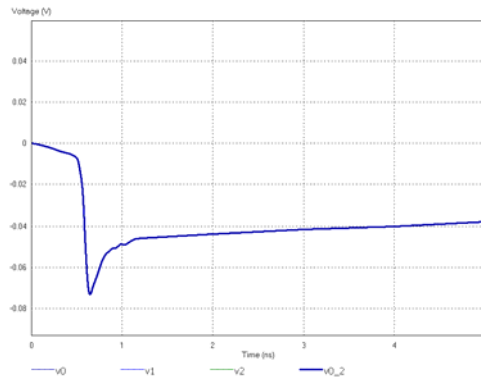
Co-simulation of chip and package correctly capture the full-chip PDN response to the IC operations. At the clock rising edge, the initial voltage drop is caused by the simultaneous switching of LEs and clock distribution networks. Currents are drawn from the on-chip decoupling capacitance for immediate charge access. After the initial voltage drop, currents flow into the chip through the package and PCB inductance with a slow recovery of the on-chip voltage. Simulation predicts about 15% more of the peak voltage drop than the measurements, a mismatch can come from both measurements and simulations. Scopes and probes may not have high enough bandwidth to capture the noise voltage at the peak point. Simulation tends to overestimate the noise as it does not include the transistor drive strength weakening effects in the presence of compressed power supply voltages. A practical consideration is to use simulated PDN noise as an upper bound when considering the PDN noise impacts on signal timing.



(a)



(b)



(c)

Figure 10. PDN noise measurements and simulation comparison. (a) Measured PDN noise on a 50GHz sampling module of DCAJ. On the rising edge of the clock, voltage drops are caused by the switching LEs and clock distribution networks. On the falling edge, LEs are not toggling and the voltage drops are caused only by the clocks. (b) Voltage drop at clock rising edge from the measurements. (c) Voltage drop from chip and package co-simulation.

4.2 PDN impedance

Frequency domain modeling is carried out in two steps. Package model is first extracted in PowerSI with the S-parameter outputs. Then the package S-parameters are brought in XcitePI and attached to the power grid model for the entire PDN simulation. PCB portion of the PDN is included in the first step of package modeling. Figure 11 shows the PDN impedance from on-chip probing ports, Z0 on the device level below the power grids and Z1 on C4 bumps atop the power grids. Both probing ports cover an area of 400um x 400um, and located at the center of the die. Below 100 MHz, the difference between Z0 (on device probe) and Z1 (on C4 probe) is mainly from the power grid resistance. PDN at

C4 bumps has a lower resistance with its parallel path through power grids to die capacitance. For both Z0 and Z1, there are a few peaks at low frequencies that are caused by PCB decaps resonances and the die-package-PCB parallel resonance. At high frequencies, the difference between the two PDN impedances is mainly from the power grid inductance. Above 1 GHz, Z0 shows a slow ramping up as the on-chip PDN sees an inductive path from the local die area through the power grid interconnects to the outside. On the other hand, Z1 at C4 bumps shows a low Q resonance at about 5 GHz, which correlates to the full chip capacitance and the inductance collectively in the power grids and the package planes. Co-simulation of the chip and package can provide an accurate analysis of the chip-package effects at frequency band above the PCB and package resonance.

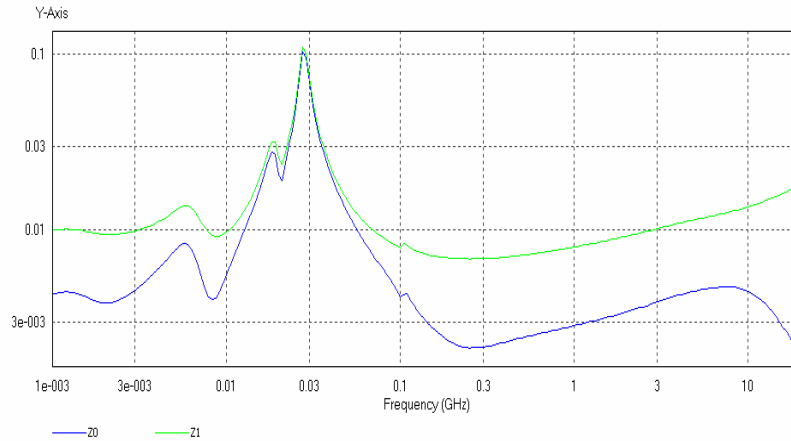


Figure 11. On-chip PDN impedance, Z0 probed on device below the power grids and Z1 probed on C4 bumps on top of the power grids. Port size is 400um x 400um. Ports location is at the center of the die.

4.3 PDN Noise Propagation

A noise current source is placed on the chip to study the noise propagation through the power grids. Figure 12 shows the voltage waveforms at three die locations with the noise excitation. P1 is at the center of the die. P2 and P3 are placed in the diagonal direction outwards to the die corner. As noise waveforms propagate through the PDN, the noise amplitude is significantly attenuated by the on chip decoupling capacitance. The propagation delay for the noise wave front from P1 to P3 is 170ps.

Figure 13 shows snapshots of the voltage distributions on the power grids and the package power planes with the noise excitation at 180ps when voltage drop at P1 reaches its peak. As shown in Figure 13 (a), voltage drop on the power grids is limited around the noise excitation area. On top package power planes, noise localization can still be observed, as shown in Figure 13 (b). Voltage distribution on top package planes, as a shadow of the distribution on power grids, shows close interactions between the two power distribution networks. As shown in Figure 13 (c) of the noise propagated down to bottom package layers, voltage is evenly distributed across the package power and ground planes. Electrically, the power and ground planes at this package level can be lumped to one node with its voltage as a function of time only.

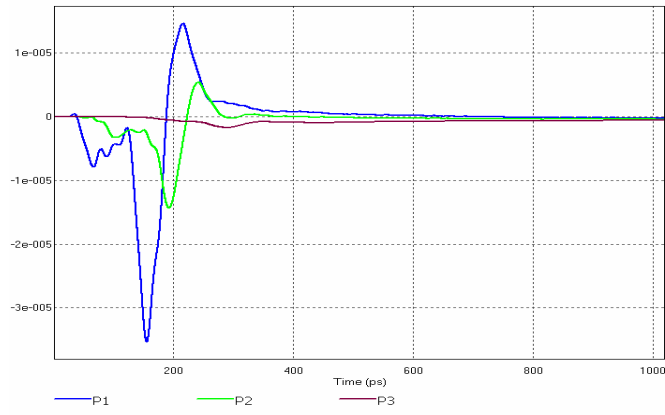
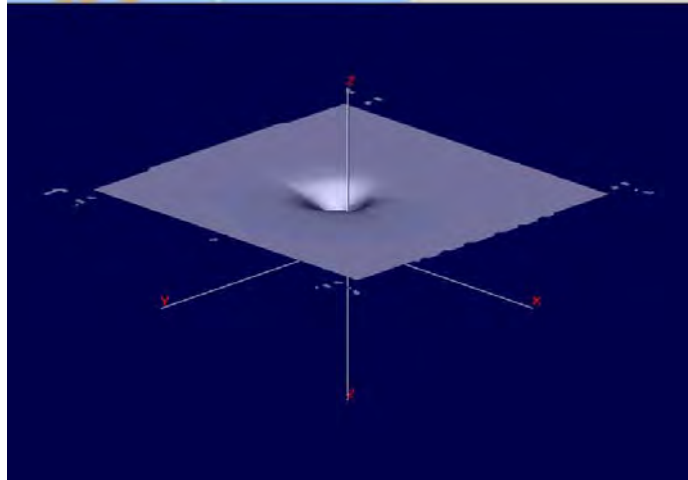
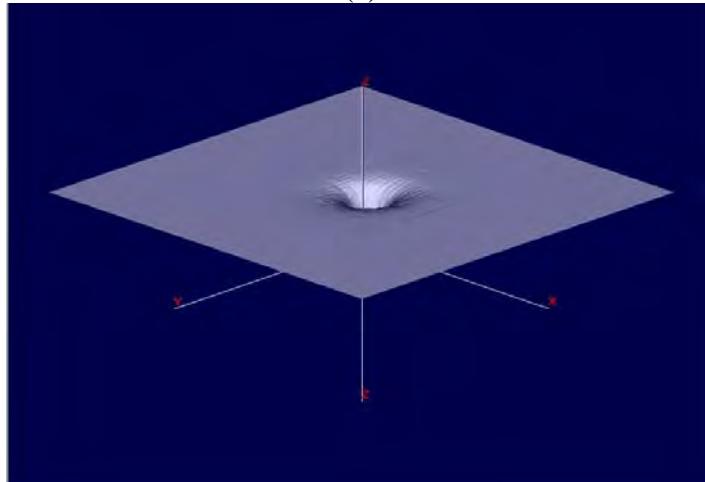


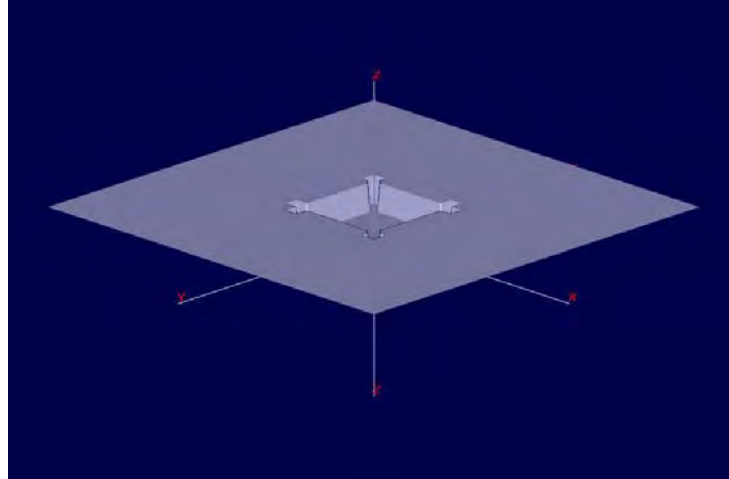
Figure 12 Noise propagation through the power grids. P1 is at the center of the die. P2 and P3 are placed in the diagonal direction outwards to the die corner.



(a)



(b)



(c)

Figure 13. Voltage distribution on power grid and package planes at 180ps (a) Voltage distribution on power grid Metal layer 10. (b) Voltage distribution of package layer 1 and 2 (VSS/VCCL). (c) Voltage distribution of package layer 8 and 9 (VSS/VCCL).

VI. Conclusions

In summary, it has been demonstrated that co-simulation of chip and package PDN is critical for full-chip PDN noise prediction and accurate representation of the noise interaction in the power distribution networks. We have presented a systematic approach for PDN noise analysis with full-chip parasitic of power grids and distributed noise current modeling at their highest level accuracy within computational constraints. The model to hardware correlation shows that we accurately predicted the PDN voltage in response to the IC operations. Co-simulation of the 3D power grids and the package planes shows the on-chip PDN impedance profiles with impacts from power grid resistance and inductance. The characteristics of noise propagation on the power grids, the effectiveness of on-chip decoupling capacitance and the interaction between chip and package have been discussed.

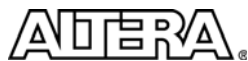
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