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An On-Die Scope Based on a 40-nm Process FPGA Transceiver

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Abstract

In high-speed serial data applications, the characterization of received signal integrity is challenging, since there are no practical methods for external metrology equipment to probe a received internal signal. We present a fully integrated on-die scope based on clock phase interpolation (PI) for data sampling of an FPGA transceiver fabricated with the 40-nm digital CMOS process. This circuit is designed for 1/32 unit interval resolution at data rates up to 11.3 Gbps. We present test methodology, design implementation, and characterization results. We compare improvements of this design over prior implementations. We also present a characterization methodology for calibrating inherent non-linear effects from PI circuit.

Author Biographies

Dr. Weichi Ding received BS and MS degrees in electrical engineering from Fudan University, China, in 1985 and 1988, respectively, and a PhD degree in Systems Engineering from Boston University, Massachusetts, in 1996. From 1988 to 1992, he was an assistant professor of electrical engineering at Fudan University. From 1996 to 2000, he worked at Cirrus Logic, Inc. where he was a manager of analog-mixed signal design. From 2000 to 2006, he was with Cisco Systems, where he worked on transceivers and other analog IPs. Since 2006, he has been with Altera Corporation where he is a senior manager, design engineering. His current interests include broadband data communication circuits, PLLs, A/D and D/A converters, and modeling of systems and architectures.

Mingde Pan received a MSEE from Fudan University in 1982. She was a visiting scholar at the University of Notre Dame from 1988 to 1991. From 1991 to 2007, she worked on PLLs, transceivers for Ethernet and wireless baseband, and A/D D/A converters at Raytheon, Fairchild, LSI, and VIA as a senior staff engineer. She joined Altera in 2007 as a design engineer, senior MTS, and works on signal detectors, phase interpolators, and eye monitors.

Tina Tran is a senior design manager at Altera Corporation, where she works in the design group and is responsible for the development of high-speed transceivers. She has been in the semiconductor industry for more than 15 years, including almost 12 years with Altera. She holds a BSEE from the University of California, Berkeley.

Wilson Wong is a principle design engineer at Altera Corporation. He has more than 19 years of experience in analog circuit design. His current interests include high-speed equalization, adaptive equalization, and clock data recovery circuits. Prior to joining Altera, Mr. Wong worked at Nexgen Microsystems and Tredennick, Inc. He holds a BSEE from the University of California, Berkeley.

Sergey Shumarayev is the director of engineering at Altera Corporation in charge of analog design. He has worked at Altera for over 10 years in the capacities of design engineer, SERDES team engineering senior design manager, and analog group director. He holds a MSEE from Cornell University and a BS in Electrical Engineering Computer Science and Material Science from the University of California, Berkeley. He has over 30 issued patents and has co-authored several papers.

Dr. Mike Peng Li As a principle architecture and distinguished engineer at Altera Corporation, Dr. Mike Peng Li is a corporate expert and adviser on jitter, noise, and high-speed link and SERDES architecture. Dr. Li pioneered a jitter separation method (Tailfit); DJ, RJ, and TJ concept and theory formation; and the jitter transfer function (JTF) concept, theory, and application for high-speed serial link design analysis and validation. He is involved in setting and contributing to standards for jitter, noise, and signal integrity for leading serial data communications, such as Fibre Channel, Gigabit Ethernet, Serial ATA, PCI Express, and FB DIMM. Currently, he is co-chairman of the PCI Express jitter standard committee. Dr. Li has been involved in and led technical committees for IEEE- and IEC-sponsored technical conferences, such as Custom Integrated Circuits Conference (CICC), International Test Conference (ITC), and DesignCon, and is an invited speaker, invited author, panelist, and session and panel chair on the subjects of jitter, noise, and signal integrity covering both design and test.

Prior to joining Altera in 2007, Dr. Li was the chief technology officer (CTO) at Wavecrest Corporation, where he developed the technology leadership and vision for the company. He has received many awards, including design paper awards from DesignCon and IEC and contribution awards from PCI-SIG. He has been listed in *Who's Who in America* and *Who's Who in the World* since 2006. Dr. Li has authored or co-authored five books and book chapters on jitter and high-speed I/O, including the widely distributed and highly ranked book *Jitter, Noise, and Signal Integrity at High-Speed.* He has published more than 80 technical papers, and holds six patents with 12 pending. Dr. Li holds a PhD in physics, an MSE in electrical and computer engineering, and an MS in physics, all from the University of Alabama, Huntsville. He also holds a BS in physics from the University of Science and Technology of China. He did his post-doctoral work at University of California, Berkeley, where he worked as a high-energy astrophysicist before joining the industry.

Dr. Daniel Chow was a senior member of technical staff at Altera Corporation. His responsibilities included defining testing and validation methodologies of high-speed components. Specifically, he was responsible for developing Altera's knowledge base on jitter measurement issues. Dr. Chow received his PhD from the University of California, Davis.

Introduction

High-speed serial transceivers have been widely used for numerous applications such as data communications and telecommunication networks (e.g., GbE, XLAUI/CAUI), optical networks (e.g., SONET, CEI/OIF), computing I/Os (e.g., PCI Express (PCIe), QPI), storage area networks (e.g., SATA, Fibre Channel), wireless networks (e.g., CPRI), and embedded processing (e.g., Serial RapidIO).

Good signal integrity is essential in high-speed applications to ensure low bit-error rate (BER) for compliance with protocol specifications [1]. Signal integrity (including signaling, jitter, and noise) of the transmitted data can be characterized by a wide range of metrology-grade test equipment such as real- and equivalent-time sampling oscilloscopes, BER testers, spectrum analyzers, and time-interval analyzers.

The received data signals are often distorted and/or attenuated by the application-dependent transmission medium (such as chip-to-chip, board-to-board, or system-to-system). Various techniques (e.g., equalization) are available to improve signal integrity prior to clock recovery and sampling for the purpose of reducing the BER of the sampled data.

The most common method for analyzing signal integrity is an eye-diagram measurement. An eye diagram is the superposition of each bit’s waveform over a 1-bit time interval, or unit interval (UI). For transmitted data, an eye diagram is constructed by probing the output signal with an oscilloscope. However, for data received inside the transceiver, there are no practical methods to observe the internal signal’s eye diagram. Thus, the effectiveness of signal-integrity improvement techniques is difficult to quantify. This limits the user’s ability to diagnose, debug, and/or characterize the data transmission link.

We present an on-die scope integrated into the receiver. The eye opening information can be used to monitor received signal integrity after equalization, which cannot be observed with external equipment. The scope has no pattern requirements or limitations, which is beneficial for monitoring and debugging live data traffic. This scope is designed and fabricated in the 40-nm digital CMOS process and embedded into an FPGA transceiver [2]. This scope can be integrated into every transceiver channel of the FPGA, providing simultaneous analysis of link quality across all channels.

We show the architecture of our design, improvements over other designs [3], and characterization data.

On-Die Scope Architecture and Theory

The block diagram for the scope is shown in Figure 1. Incoming data is received (Rx), and signal conditioning (e.g., continuous time linear equalization (CTLE), decision feedback equalization (DFE), etc.) is applied to improve the signal integrity. The data’s embedded clock is extracted by the clock recovery (CR) block. The recovered clock signal determines the sampling time position. A phase interpolator is used to systematically offset the sampling time position relative to the data signal, as shown in Figure 2.

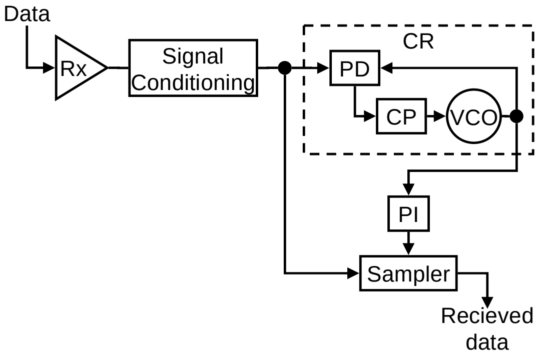


Figure 1. Block diagram for on-die scope

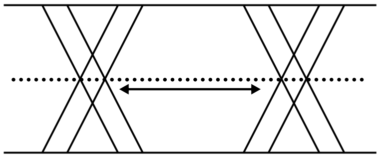


Figure 2. The scope allows systematic shifting of the sampling time position along the dotted line, creating an offset relative to the data signal

By analyzing the received data for varying sampling positions, the on-die scope can effectively probe the width of the eye opening of the received data. Because the phase interpolation (PI) and sampling occurs after clock recovery, the impact of Rx and equalization can be observed by the on-die scope for the purpose of optimizing signal integrity.

The PI's functional mechanism is described by constructing a circle in the *A*-*B* plane (Figure 3), where *A* and *B* are the amplitudes of two orthogonal sinusoidal functions oscillating in time *t* with frequency ω. The PI output *C* is defined as the sum of sinusoidal functions,

$$C = A\sin(\omega t) + B\cos(\omega t). \tag{1}$$

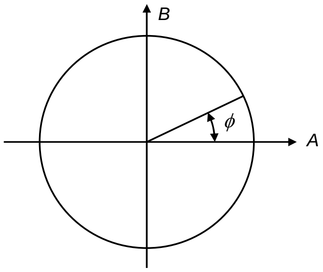


Figure 3. Circle in *A*-*B* plane with phase angle ϕ

By algebraic manipulation and trigonometric identities, it can be shown that

$$\begin{aligned} C &= \sqrt{A^2+B^2}\left(\frac{A\sin(\omega t)+B\cos(\omega t)}{\sqrt{A^2+B^2}}\right) \\ &= \sqrt{A^2+B^2}\left(\cos(\phi)\sin(\omega t)+\sin(\phi)\cos(\omega t)\right), \\ &= D\sin(\omega t+\phi) \end{aligned} \qquad (2)$$

where

$$D = \sqrt{A^2+B^2},\ \phi = \arctan\left(\frac{B}{A}\right). \qquad (3)$$

Therefore, the PI output C is a single sinusoidal function with amplitude D and phase offset ϕ from the base function $\sin(\omega t)$. Any phase offset angle can be obtained by the appropriate choice of the ratio B/A.

Circuit Implementation

The clock signals CLK_0 and CLK_{90} are two differential clock signals constructed from the four-phase clock outputs from the CR and serves as the basis for the orthogonal sinusoidal functions described in equation (1). The four-phase clocks are square waves that require filtering with the appropriate programmable bandwidth to convert them to sinusoidal signals. The clock signals are summed by the load resistor pair, each with a value R. The amplitudes of CLK_0 and CLK_{90} are determined by adjustable current sources I_1 and I_2, respectively. The current sources are controlled by a digital-to-analog converter (DAC). Applying equations (1) and (3) to this circuit, we obtain

$$\frac{V_{Out}}{R} = I_1 \times CLK_0 + I_2 \times CLK_{90}, \qquad (4)$$

where

$$\left|\frac{V_{Out}}{R}\right| = \sqrt{I_1{}^2 + I_2{}^2},\ \phi = \arctan\left(\frac{I_2}{I_1}\right). \qquad (5)$$

Therefore, for constant load resistor R, the output V_{Out} is a simple sinusoidal function with frequency ω and phase offset ϕ from CLK_0 determined by adjusting the ratio of I_2 to I_1.

Since I_1 and I_2 can only take on positive values, the simplified circuit implementation of the PI (Figure 4) can only create phase offsets in the first quadrant (i.e., between 0° and 90° offset from CLK_0). To obtain phase offsets in the remaining three quadrants, the PI must select the appropriate input sinusoidal functions from the four-phase clock outputs of the CR. For simplicity, this is not shown in Figure 4.

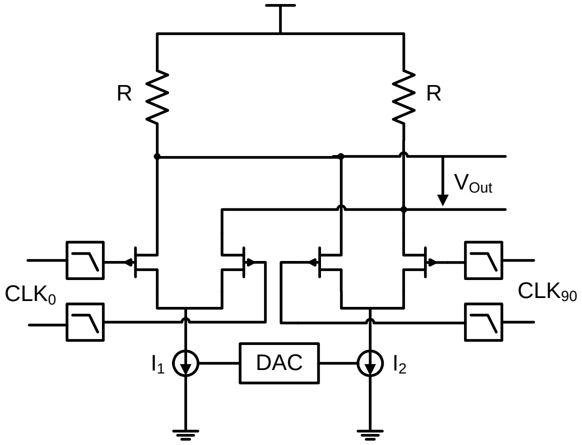


Figure 4. Circuit implementation of the PI

In our implementation, the possible values of the ratio I_2/I_1 are limited by the DAC to four bits of resolution. This limits the phase-offset resolution to 16 values in each quadrant, for a total of 64 values over 360°. Because of the half-rate architecture of the transceiver, one cycle of the recovered clock signal spans two UIs of the received data. Thus, the PI has a timing resolution of 1/32 of a UI of the received data.

The linearity of the phase offsets is limited by the logic controlling the PI. The sum of I_1^2 and I_2^2 must be held constant. Deviations from this constant will introduce non-linearity in the phase offsets. Linearity is dependent on the arctangent function, which is non-linear in nature. The linearity is also dependent on the programmable filter bandwidth for the four-phase clocks. Equation (1) requires the input clocks to be pure sinusoidal functions. Non-ideal filtering on these signals will introduce non-linearity.

Some non-linear effects can be compensated by using a higher resolution DAC at the expense of more complicated circuitry, power consumption, and silicon area. Despite any possible non-linearity in the circuit implementation, the PI will always exhibit monotonicity over its functional range. The accuracy of the PI is limited by CR output clock jitter, duty cycle, and clock phase offsets.

Non-linearity can be compensated by calibration. A simple calibration procedure can be developed by using an external pattern generator capable of injecting known levels of jitter to degrade, or “close,” the received eye diagram in a controlled manner. The received eye width, as determined by the on-die scope, can be compared to the known eye opening due to external jitter.

Other implementations of a phase interpolator require four adjustable current sources in order to span 360° of phase offsets. Our design shown in Figure 4 takes advantage of the available four-phase output clock from the CR to reduce the number of adjustable current sources to two without compromising the 360° range of phase offsets. Our implementation simplifies the controlling logic of the PI, reduces power consumption, decreases loading on the circuit, and can operate at higher speeds. We also take advantage of existing CR and equalization blocks in the transceiver to form a complete signal integrity monitoring solution capable of simultaneous analysis across multiple channels.

Measurement Results

The on-die scope was implemented into Altera's Stratix® IV family of transceiver FPGAs capable of transmitting and receiving data up to 11.3 Gbps.

Figure 5 shows a block diagram for the measurement setup. An Agilent 81141A pattern generator created a 6.5-Gbps pseudo-random bit sequence data stream (PRBS 2^{15}-1) which was transmitted to the Rx of the transceiver. Using the on-die scope, the received data was sampled with varying phase offsets. The sampled data was passed internally from the receiver to the FPGA, where the bits were checked for errors using a soft IP implemented in the FPGA. The number of bits received and the number of bit errors were counted. The BER is the ratio of bit errors to the total number of received bits.

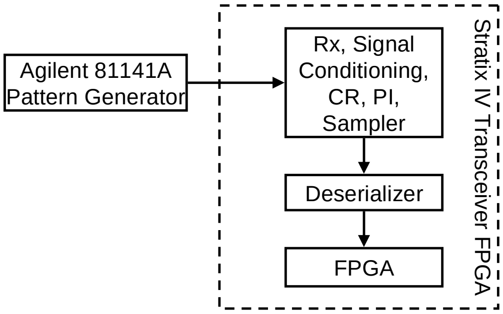


Figure 5. Block diagram for measurement setup

The expectation is that phase offsets close to the center of the eye diagram will have a very low BER. As the phase offsets shift closer to the transition edges, the BER will increase. Figure 6 shows the measured BER for 32 phase offsets over a range of approximately one UI, depending on the linearity of the PI.

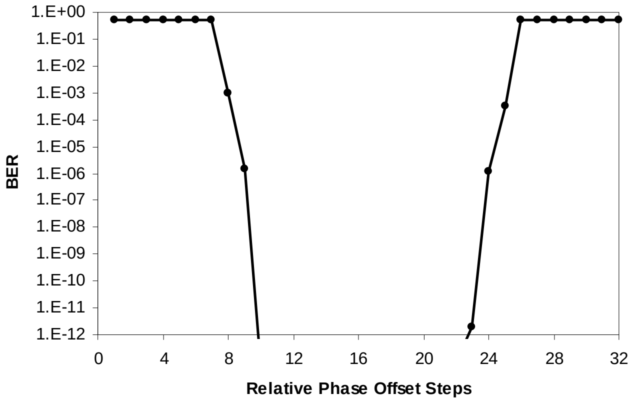


Figure 6. BER for phase offsets over approximately one UI

For relative phase offset steps from 10 to 23, the BER is on the order of 10^{-12} or lower, which is indicative of the sampling point being in the “open,” or error-free, region of the eye diagram.

For relative phase offsets steps from 1 to 7 and 26 to 32, the BER so high that the error-checking IP in the FPGA is unable to synchronize itself to the sampled data, effectively yielding a 50% error because of the transition density of the PRBS pattern. This is indicative of the sampling point being very close to, or in the transition edge region of the eye diagram.

The transitions from high BER to low BER are indications of the receive path’s jitter properties and can be further analyzed to provide jitter decomposition [4].

Based on Figure 6, the effective width of the eye opening at BER = 10^{-12} or lower is 14 phase-offset steps. Neglecting the PI output non-linearity for 6.5 Gbps and 32 phase-offset steps per UI, each phase-offset step corresponds to 4.8 ps. This corresponds to an eye opening of ~67 ps, or a total jitter (TJ) of ~87 ps at BER = 10^{-12}.

To correlate the on-die measurements with an off-chip measurement, we configured the transceiver in a loopback mode so the sampled data is re-timed by the recovered clock and re-transmitted through a transmit buffer (Figure 7). In this configuration, the received data is sampled at the center of the eye. However, due to internal path differences, the loopback performance can only be qualitatively compared with the results from Figure 6.

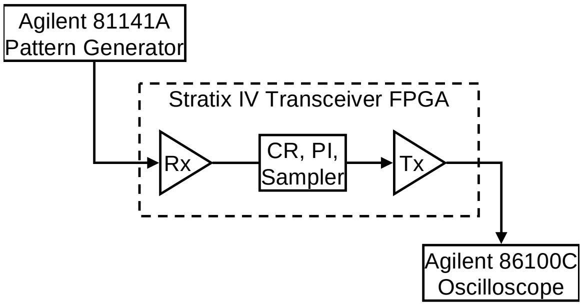
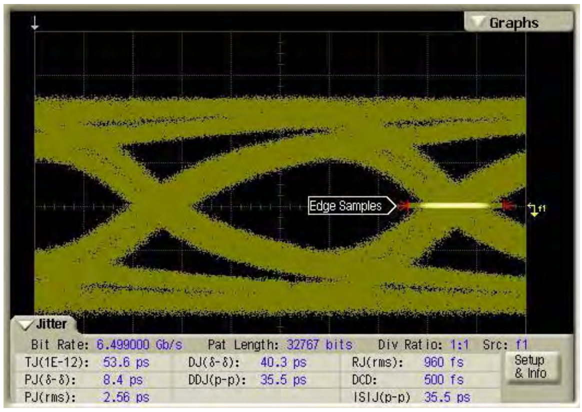


Figure 7. Block diagram for loopback configuration

Figure 8 shows the eye diagram and jitter measurement of the loopbacked data signal (characterized externally with an Agilent 86100C oscilloscope). The TJ is 53.6 ps defined at BER=10^{-12}, which corresponds to an eye opening of ~100 ps. The discrepancy between the eye openings in Figure 6 and Figure 8 is ~33 ps, or ~21% of a UI. This discrepancy is due to internal path differences of the two data signals and non-linearity of the PI.



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Bit Rate: 6.499000 Gb/s    Pat Length: 32767 bits    Div Ratio: 1:1   Src: f1
TJ(1E-12):   53.6 ps     DJ(δ-δ):    40.3 ps     RJ(rms):    960 fs
PJ(δ-δ):     8.4 ps      DDJ(p-p):   35.5 ps     DCD:        500 fs
PJ(rms):     2.56 ps                             ISIJ(p-p)   35.5 ps
```

Figure 8. Measured eye diagram and jitter from loopback path

Conclusions

We presented an on-die scope for monitoring the width of the eye-opening in a received data signal designed for up to 11.3-Gbps operation and fabricated in the 40-nm digital CMOS process. This feature allows evaluation and analysis of equalization effects on received data signals for the purpose of diagnosing signal conditioning and integrity optimization. This solution can be applied to many emerging challenges in verification, characterization, and production testing that cannot be met with external equipment.

References

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