

Cyclone® V Device Family Pin Connection Guidelines

Preliminary PCG-01014-1.1

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The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Cyclone V (transceiver-based device) Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins			
CLK[0:11][p:n]	I/O, Clock	Dedicated positive and negative clock input pins that can also be used for data inputs. OCT Rd is supported on these pins. When you use single-ended I/O standard, only the CLK[0:11]p pins serve as the dedicated input pins to the PLL.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND. Some CLK input pins share dual-purpose functionality with FPLL_[BL,BR,TL,TR]_FB pins. For more information, refer to the specific device pinout file.
FPLL_[BL,BR,TL,TR]_CLKOUT0, FPLL_[BL,BR,TL,TR]_CLKOUTp, FPLL_[BL,BR,TL,TR]_FB	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended clock output pins, one differential clock output pair, or single-ended feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[BL,BR,TL,TR]_CLKOUT1, FPLL_[BL,BR,TL,TR]_CLKOUTn	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Dedicated Configuration/JTAG Pins			
MSEL[0:4]	Input	Configuration input pins that set the FPGA device configuration scheme.	These pins are internally connected through a 5-kΩ resistor to GND. Depending on the configuration scheme used, these pins should be tied directly to VCCPGM or GND. Refer to the "Configuration, Design Security, and Remote System Upgrades in Cyclone V Devices" chapter in the Cyclone V Device Handbook for the configuration scheme options. Tied the MSEL pins to GND if your device is only using JTAG configuration.
AS_DATA0 / ASDO / DATA[0]	Bidirectional	Dedicated configuration pin. When using an EPCS device (x1 mode) this is the ASDO pin and used to send address and control signals between the FPGA and the EPCS/EPCQ. Used as Data[0] for FPP & PS.	When this pin is not used it is recommended to leave the pin unconnected.
AS_DATA[1:3] / DATA[1:3]	Bidirectional	Dedicated configuration data pins. Configuration data is transported on these pins when connected to the EPCQ devices. Used as DATA[1:3] for FPP.	When this pin is not used it is recommended to leave the pin unconnected.
nCSO/ DATA[4]	Output	Output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device. Also, used as DATA[4] in FPP.	When not programming the device in AS mode nCSO is not used. When this pin is not used as an output then it is recommended to leave the pin unconnected.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE should be connected to GND.

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nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	nCONFIG should be connected directly to the configuration controller when the FPGA uses a passive configuration scheme, or through a 10-kΩ resistor tied to VCCPGM when using an active serial configuration scheme. If this pin is not used, it requires a connection directly or through a 10-kΩ resistor to VCCPGM.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistor to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. If this pin is not enabled for use as a configuration pin, it can be used as a user I/O pin.	During multi-device configuration, this pin feeds the nCE pin of a subsequent device. Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. During single device configuration, this pin may be left floating.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistor to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host.
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-kΩ pull-down resistor to GND. This pin has an internal 25-kΩ pull-down.
TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to the VCCPD in the dedicated IO bank which the JTAG pin reside. To disable the JTAG circuitry connect TMS to VCCPD via a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up.
TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD in the dedicated IO bank which the JTAG pin reside. To disable the JTAG circuitry connect TDI to VCCPD via a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up.
TDO	Output	Dedicated JTAG test data output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected. In cases where TDO uses VCCPD = 2.5 V to drive a 3.3 V JTAG interface, there may be leakage current in the TDI input buffer of the interfacing devices. An external pull-up resistor tied to 3.3 V on their TDI pin may be used to eliminate the leakage current if needed.
Optional/Dual-Purpose Configuration			

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DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.	When using the dedicated CRC_ERROR pin configured as an open drain output, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using the dedicated CRC_ERROR configured as open drain, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software. The I/O buffer type is reported in the fitter report.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
DATA[5:15]	I/O, Input	Dual-purpose configuration input data pins. Use DATA [5:7] pins for FPP x8, DATA [5:15] pins for FPP x16. Configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	When the inputs for DATA[5:15] are not used and these pins are not used as an I/O then it is recommended to leave these pins unconnected.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	When using the dedicated INIT_DONE pin configured as an open drain output, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using the dedicated INIT_DONE configured as open drain, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.

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CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to ground.
CvP_CONFDONE	I/O, Output (open-drain)	Configuration via Protocol (CvP) Done pin is driven low during configuration. When CvP is complete, this signal is released and is pulled high by an external pull-up resistor. Status of this pin is only valid if CONF_DONE is high.	When using the dedicated CvP_CONFDONE pin configured as an open drain output, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using the dedicated CvP_CONFDONE configured as open drain, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
nPERST[L0,L1]	I/O, Input	Dedicated Fundamental Reset pin is only available when used in conjunction with PCIe HIP. When low the transceivers are in reset. When high the transceivers are out of reset. When this pin is not used as the fundamental reset, this pin may be used as a user I/O.	Connect this pin as defined in the Quartus II software. This signal is required for CvP configuration scheme. There are two nPERST pins in all Cyclone V devices, even if the device has fewer than two instances of Hard IP for PCIe. The nPERSTL0 pin is located in the bottom left Hard IP and CvP blocks while the nPERSTL1 pin is located in the top left Hard IP. For maximum compatibility, Altera recommends using the bottom left PCIe Hard IP first as this is the only location that supports CvP configuration scheme.
Partial Reconfiguration Pins			
PR_REQUEST	I/O, Input	Partial Reconfiguration Request pin. Drive this pin high to start partial reconfiguration. Drive this pin low to end reconfiguration. This pin can only be used in Partial Reconfiguration using external host mode in FPP x16 configuration scheme.	When the dedicated input PR_REQUEST is not used and this pin is not used as an I/O, then it is recommended to tie this pin to GND.
PR_READY	I/O, Output or Output (open-drain)	The partial reconfiguration ready pin is driven low until the device is ready to begin partial reconfiguration. When the device is ready to start reconfiguration, this signal is released and is pulled high by an external pull-up resistor.	When using the dedicated PR_READY pin configured as an open drain output, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using the dedicated PR_READY configured as open drain, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
PR_ERROR	I/O, Output or Output (open-drain)	The partial reconfiguration error pin is driven low during partial reconfiguration unless the device detects an error. If an error is detected, this signal is released and pulled high by an external pull-up resistor.	When using the dedicated PR_ERROR pin configured as an open drain output, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using the dedicated PR_ERROR configured as open drain, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.

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PR_DONE	I/O, Output or Output (open-drain)	The partial reconfiguration done pin is driven low until the partial reconfiguration is complete. When the reconfiguration is complete, this signal is released and is pulled high by an external pull-up resistor.	When using the dedicated PR_DONE pin configured as an open drain output, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using the dedicated PR_DONE configured as open drain, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
Differential I/O Pins			
DIFFIO_RX_[B,T][#.#]p, DIFFIO_RX_[B,T][#.#]n	I/O, RX channel	These are true LVDS receiver channels on row and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. OCT Rd is supported on all DIFFIO_RX pins.	Connect unused pins as defined in Quartus II software.
DIFFIO_TX_[B,T][#.#]p, DIFFIO_TX_[B,T][#.#]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.
DIFFOUT_[B,T][#.#]p, DIFFOUT_[B,T][#.#]n	I/O, TX channel	These are emulated LVDS output channels. All the user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. External resistor network is needed for emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins	Connect unused pins as defined in Quartus II software.
External Memory Interface Pins			
DQS#[B,R,T]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in Quartus II software.

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DQSn#[B,R,T]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in Quartus II software.
DQ#[B,R,T]	I/O, bidirectional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in Quartus II software.
Hard PHY			
[B,T]_DM_#	I/O, Output	Optional Write Data Mask, edge-aligned to DQ during Write.	Connect unused pins as defined in Quartus II software.
[B,T]_WE#	I/O, Output	Write enable. Write-enable input for DDR2, DDR3 SDRAM and RLD RAM II	Connect unused pins as defined in Quartus II software.
[B,T]_CAS#	I/O, Output	Column Address Strobe for DDR2 & DDR3 SDRAM	Connect unused pins as defined in Quartus II software.
[B,T]_RAS#	I/O, Output	Row Address Strobe for DDR2 & DDR3 SDRAM.	Connect unused pins as defined in Quartus II software.
[B,T]_RESET#	IO, Output	Active low reset signal.	Connect unused pins as defined in Quartus II software.
[B,T]_CK	IO, Output	Output clock for external memory devices.	Connect unused pins as defined in Quartus II software.
[B,T]_CK#	IO, Output	Output clock for external memory devices, inverted CK.	Connect unused pins as defined in Quartus II software.
[B,T]_CKE_#	IO, Output	Active high clock enable.	Connect unused pins as defined in Quartus II software.
[B,T]_BA_#	IO, Output	Bank address input for DDR2, DDR3 SDRAM and RLD RAM II	Connect unused pins as defined in Quartus II software.
[B,T]_A_#	IO, Output	Address input for DDR2, DDR3 SDRAM, and RLD RAM II	Connect unused pins as defined in Quartus II software.
[B,T]_CS#_#	IO, Output	Active low Chip Select.	Connect unused pins as defined in Quartus II software.
[B,T]_CA_#	IO, Output	Command and address input for LPDDR SDRAM	Connect unused pins as defined in Quartus II software.
[B,T]_ODT_#	IO, Output	On-die termination signal enables and disables termination resistance internal to the external memory.	Connect unused pins as defined in Quartus II software.

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Reference Pins			
RZQ_[0,1,2]	I/O, Input	Reference pins for I/O banks. The RZQ pins share the same VCCIO with the I/O bank where they are located. The external precision resistor must be connected to the designated pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to GND. When used for OCT calibration, the RZQ pin is connected to GND through an external 100- or 240- reference resistor depending on the desired OCT impedance. Refer to the Cyclone V device handbook for the OCT impedance options for the desired OCT scheme.
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, ground or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.
Supply Pins (See Notes 4 through 7)			
VCC	Power	VCC supplies power to the core, periphery, HIP and PCS.	Connect all VCC pins to a 1.1V low noise switching regulator. VCCE_GXBL and VCCL_GXBL maybe sourced from the same regulator as VCC with proper isolation filter. Use Cyclone V Early Power Estimator to determine the current requirements for VCC and other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3 and 6.
VCCA_FPLL	Power	PLL Analog power.	Connect these pins to a 2.5V low noise switching power supply through a proper isolation filter. This power rail may be shared with VCC_AUX and VCCH_GXBL. With a proper isolation filter these pins may be sourced from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCC_AUX	Power	Auxiliary supply.	Connect all VCC_AUX pins to a 2.5V low noise switching power supply through a proper isolation filter. This power rail may be shared with VCCH_GXBL and VCCA_FPLL. With a proper isolation filter these pins may be sourced from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCCIO[#]	Power	These are I/O supply voltage pins for I/O banks. Each bank can support a different voltage level from 1.2V to 3.3V. Supported IO standards are LVTTTL/LVCMOS (3.3, 3.0, 2.5, 1.8, 1.5, 1.2V), SSTL(135,125,18,15,2 Class-I/II), HSTL(18,15,12 Class-I/II), HSUL12, LVDS, LVPECL, and PCI/PCI-X.	Connect these pins to 1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V, 3.0V or 3.3V supplies, depending on the I/O standard required by the specified bank. When these pins require 2.5V they may be tied to the same regulator as VCCPD and VCCPGM, but only if each of these supplies require 2.5V sources. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, and 8.
VCCPGM	Power	Configuration pins power supply which support 1.8, 2.5, 3.0 & 3.3V	Connect these pins to either 1.8V, 2.5V, 3.0V or 3.3V power supply. When these pins require 2.5V they may be tied to the same regulator as VCCIO and VCCPD, but only if each of these supplies require 2.5V sources. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VCCPD[#]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 2.5V, 3.0 & 3.3V. For 1.2V, 1.25V, 1.35V, 1.5V, 1.8V or 2.5V I/O standards connect VCCPD to 2.5V and for 3.0V I/O standard connect VCCPD to 3.0V or 3.3V.	The VCCPD pins require 2.5V, 3.0V or 3.3V. When these pins require 2.5V they may be tied to the same regulator as VCCPGM and VCCIO, but only if each of these supplies require 2.5V sources. The voltage on these pins must be equal to or greater than VCCIO of the respective banks. For instance when VCCIO is 3.3V, VCCPD must be 3.3V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3 and 8.

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VCCBAT	Power	Battery back-up power supply for design security volatile key register.	Connect this pin to a Non-volatile battery power source in the range of 1.2V - 3.0V when using design security volatile key. In this case, do not connect this pin to a volatile power source on the board. 3.0V is the typical battery power selected for this supply. When not using the volatile key, tie this to a 1.5V, 2.5V or 3.0V supply. Cyclone V devices will not exit POR if VCCBAT stays at logic low.
GND	Ground	Device ground pins.	All GND pins must be connected to the board ground plane.
VREF[#]N0	I/O, Power	Input reference voltage for each I/O bank. If a bank uses a voltage referenced I/O standard for input operation, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.	If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. When VREF pins are used as I/O, they have higher capacitance than regular I/O pins which will slow the edge rates and affect I/O timing. Decoupling depends on the design decoupling requirements of the specific board. See Note 2 and 8.
Transceiver Pins (See Notes 4 through 10)			
VCCE_GXBL	Power	Analog power, transmitter, specific to the left (L) side of the device.	Connect VCCE_GXBL pins to a 1.1V low noise switching regulator. For Cyclone V GX, these pins may be tied to the same 1.1V regulator as VCC with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 7 and 10. This power rail can be shared with VCCL_GXBL pins.
VCCL_GXBL	Power	Analog power, clock network power, specific to the left (L) side of the device.	Connect VCCL_GXBL pins to a 1.1V low noise switching regulator. These pins may be tied to the same 1.1V plane as VCC with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 7 and 10. This power rail can be shared with VCCE_GXBL pins.
VCCH_GXBL	Power	Analog power, transceiver high voltage power, specific to the left (L) side of the device.	Connect VCCH_GXBL to a 2.5V low noise switching regulator. This power rail may be shared with VCCA_FPLL and VCC_AUX. With a proper isolation filter these pins may be sourced from the same regulator as VCCIO, VCCPD, and VCCPGM when each of these power supplies require 2.5V. Decoupling depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, and 7.
GXB_RX_L[0:11][p,n], GXB_REFCLK_L[0:11][p,n]	Input	High speed positive (p) or negative (n) differential receiver channels. High speed positive (p) or negative (n) differential reference clock specific to the left (L) side of the device.	These pins are AC-coupled when used. Connect all unused pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 9.
GXB_TX_L[0:11][p,n]	Output	High speed positive differential transmitter channels. Specific to the left (L) side of the device.	Leave all unused GXB_TX pins floating.
REFCLK[0:3]_L[p,n]	Input	High speed positive (p) and negative (n) differential reference clock, specific to the left (L) side of the device.	These pins may be AC-coupled or DC-coupled when used. For HCSL I/O standard, it only support DC coupling. Connect all unused pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 9.

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You should create a Quartus® II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Cyclone V (transceiver-based device) Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
RREF_TL	Input	Reference resistor for transceiver, specific to the left (L) side of the device.	If any REFCLK pin or transceiver channel on left side of the device is used, you must connect each RREF pin on that side of the device to its own individual 2.0-kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

- 1) This pin connection guidelines is created based on the Cyclone V GX device family.
- 2) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling.
- 3) Use the Cyclone V Early Power Estimator to determine the current requirements for VCC and other power supplies.
- 4) These supplies may share power planes across multiple Cyclone V devices.
- 5) Example 1 and Figure 1 illustrate power supply sharing guidelines for Cyclone V GX.
- 6) Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
- 7) Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response.
Line Regulation < 0.4%
Load Regulation < 1.2%
- 8) The number of modular I/O banks on Cyclone V devices depends on the device density. For the indexes available for a specific device, please refer to the I/O Bank section in the Cyclone V device handbook.
- 9) For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
- 10) If none of the transceivers are used on one side of the device, then the transceiver power pins on that side may be tied to GND except for the VCCH_GXBL power pin.
- 11) For item [#] Please refer to the device pin table for the pin-out mapping.

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Example 1. Cyclone V GX Power Supply Sharing Guidelines

Example Requiring 2 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes	
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCL_GXBL and VCCE_GXBL with VCC with proper isolation filters.	
VCCL_GXBL					Isolate		
VCCE_GXBL							
VCCIO	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.	
VCCPD							
VCCPGM							
VCC_AUX		2.5			Isolate		VCCH_GXBL and VCCA_FPLL must always be powered up for the PLL operation. May be able to share VCC_AUX, VCCH_GXBL, VCCBAT, and VCCA_FPLL with the same regulator as VCCIO, VCCPD, and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Cyclone V devices. If design security feature is used, VCCBAT should be powered by battery with voltage range as stated in datasheet.
VCCA_FPLL							
VCCH_GXBL							
VCCBAT	Varies						

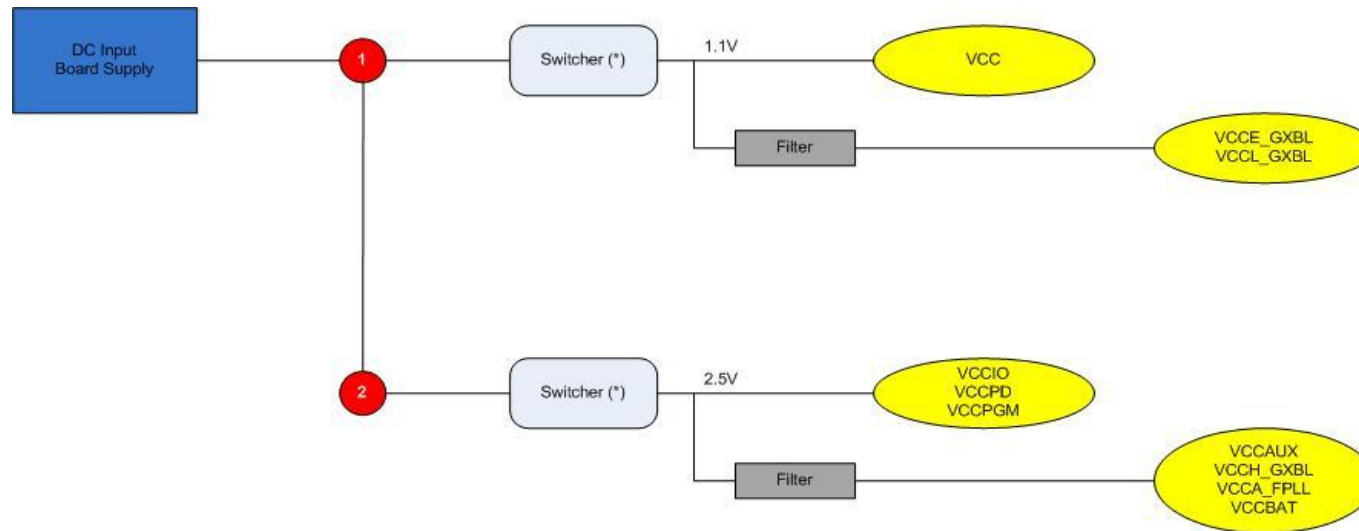
* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Cyclone V GX is provided in Figure 1.

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Figure 1. Example Cyclone V GX Power Supply Block Diagram



* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

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Revision History

Revision	Description of Changes	Date
1.0	Initial Release.	11/25/2011
1.1	Updated VCCA_FPLL and VCCH_GXBL power-up requirements.	3/29/2012