

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

© 2011 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

These pin connection guidelines should only be used as a recommendation, not as a specification.

The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

PLEASE REVIEW THE FOLLOWING TERMS AND CONDITIONS CAREFULLY BEFORE USING THE PIN CONNECTION GUIDELINES ("GUIDELINES") PROVIDED TO YOU. BY USING THESE GUIDELINES, YOU INDICATE YOUR ACCEPTANCE OF SUCH TERMS AND CONDITIONS, WHICH CONSTITUTE THE LICENSE AGREEMENT ("AGREEMENT") BETWEEN YOU AND ALTERA CORPORATION ("ALTERA"). IF YOU DO NOT AGREE WITH ANY OF THESE TERMS AND CONDITIONS, DO NOT DOWNLOAD, COPY, INSTALL, OR USE OF THESE GUIDELINES.

1. Subject to the terms and conditions of this Agreement, Altera grants to you the use of this pin connection guideline to determine the pin connections of an Altera® programmable logic device-based design. You may not use this pin connection guideline for any other purpose.
2. Altera does not guarantee or imply the reliability, or serviceability, of the pin connection guidelines or other items provided as part of these guidelines. The files contained herein are provided 'AS IS'. ALTERA DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.
3. In no event shall the aggregate liability of Altera relating to this Agreement or the subject matter hereof under any legal theory (whether in tort, contract, or otherwise), exceed One US Dollar (US\$1.00). In no event shall Altera be liable for any lost revenue, lost profits, or other consequential, indirect, or special damages caused by your use of these guidelines even if advised of the possibility of such damages.
4. This Agreement shall be governed by the laws of the State of California, without regard to conflict of law or choice of law principles. You agree to submit to the exclusive jurisdiction of the courts in the County of Santa Clara, State of California for the resolution of any dispute or claim arising out of or relating to this Agreement. The parties hereby agree that the party who is not the substantially prevailing party with respect to a dispute, claim, or controversy relating to this Agreement shall pay the costs actually incurred by the substantially prevailing party in relation to such dispute, claim, or controversy, including attorneys' fees.

BY DOWNLOADING OR USING THESE GUIDELINES, YOU ACKNOWLEDGE THAT YOU HAVE READ THIS AGREEMENT, UNDERSTAND IT, AND AGREE TO BE BOUND BY ITS TERMS AND CONDITIONS. YOU AND ALTERA FURTHER AGREE THAT IT IS THE COMPLETE AND EXCLUSIVE STATEMENT OF THE AGREEMENT BETWEEN YOU AND ALTERA, WHICH SUPERSEDES ANY PROPOSAL OR PRIOR AGREEMENT, ORAL OR WRITTEN, AND ANY OTHER COMMUNICATIONS BETWEEN YOU AND ALTERA RELATING TO THE SUBJECT MATTER OF THIS AGREEMENT.

Pin Connection Guidelines Agreement © 2011 Altera Corporation. All rights reserved.

**Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6**

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins				
CLK[1,3,8,10]p	CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins. These pins do not support output functions, OCT Rt, or the programmable weak pull up resistor.	Connect unused pins to GND.
CLK[1,3,8,10]n	CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins. These pins do not support output functions, OCT Rt, or the programmable weak pull up resistor.	Connect unused pins to GND.
CLK[0,2,9,11]p	CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[0,2,9,11]n	CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[4:7,12:15]p	CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[4:7,12:15]n	CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[L1,L4,R1,R4]_CLKp	PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively. OCT Rd is not supported on these pins. These pins do not support output functions, OCT Rt, or the programmable weak pull up resistor.	Connect unused pins to GND.
PLL_[L1,L4,R1,R4]_CLKn	PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively. OCT Rd is not supported on these pins. These pins do not support output functions, OCT Rt, or the programmable weak pull up resistor.	Connect unused pins to GND.

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[L1, L2, L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	PLL_[L1, L2, L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT0p	PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT0n	PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Configuration/JTAG Pins				
nIO_PULLUP	nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5V, 1.8V, 2.5V, or 3.0V) turns off the weak pull-up, while a logic low turns them on.	The nIO-PULLUP can be tied directly to VCCPGM, use a 1 kΩ pull-up resistor or tied directly to GND depending on the use desired for the device. Refer to the description column..
TEMPDIODEp	TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.	If the temperature sensing diode is not connected to an external temperature sense device, then connect this pin to GND.
TEMPDIODEn	TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.	If the temperature sensing diode is not connected to an external temperature sense device, then connect this pin to GND.
MSEL[0:2]	MSEL[0:2]	Input	Configuration input pins that set the FPGA device configuration scheme.	These pins are internally connected through a 5-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used these pins should be tied to VCCPGM or GND. Refer to the "Configuring Stratix IV Devices" chapter in the Stratix IV Handbook. If only JTAG configuration is used, connect these pins to ground.
nCE	nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE should be connected to GND.

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
nCONFIG	nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	nCONFIG should be connected directly to the configuration controller when the FPGA uses a passive configuration scheme, or through a 10-kΩ resistor tied to VCCPGM when using an active serial configuration scheme. If this pin is not used, it requires a connection directly or through a 10-kΩ resistor to VCCPGM.
CONF_DONE	CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.	If internal pull-up resistors on the configuration controller or enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on this pin. Otherwise an external 10-kΩ pull-up resistor to VCCPGM should be used. When using Passive configuration schemes this pin should also be monitored by the configuration controller.
nCEO	nCEO	Output	Output that drives low when device configuration is complete.	During multi-device configuration, this pin feeds the nCE pin of a subsequent device. During single device configuration, this pin is left floating.
nSTATUS	nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.	The OE and nCE pins of the enhanced configuration devices have optional internal programmable pull-up resistors. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up should not be used on these pins. Otherwise, an external 10-kΩ pull-up resistors to VCCPGM should be used. When using Passive configuration schemes this pin should also be monitored by the configuration controller.
PORSEL	PORSEL	Input	Dedicated input which selects between a POR time of 4 -12 ms or 100 - 300 ms. A logic high (1.8V, 2.5V, 3.0V) selects a POR time of 4 -12 ms and a logic low selects POR time of 100 - 300 ms.	The PORSEL pin should be tied directly to VCCPGM or GND.
TCK	TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-kΩ pull-down resistor to GND. See Note 16.
TMS	TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TMS to VCCPD via a 1-kΩ resistor. See Note 16.
TDI	TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TDI to VCCPD via a 1-kΩ resistor. See Note 16.

**Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6**

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
TDO	TDO	Output	Dedicated JTAG test data output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected. See Note 16.
TRST	TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of TRST is optional. When using this pin ensure that TMS is held high or TCK is static when TRST is changed from low to high. If not using TRST, tie this pin to a 1-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry, tie this pin to GND. See Note 16.
nCSO	nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode nCSO is not used. Also, when this pin is not used as an output then it is recommended to leave the pin unconnected.
ASDO	ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.	When not programming the device in AS mode ASDO is not used. Also, when this pin is not used as an output then it is recommended to leave the pin unconnected.
DCLK	DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.	Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. See Note 11.
DEV_CLRn	DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground. See Note 11.
DEV_OE	DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground. See Note 11.
DATA0	DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.	When the dedicated input for DATA[0] is not used and this pin is not used as an I/O then it is recommended to leave this pin unconnected. See Note 11.

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
DATA[1:7]	DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	When the dedicated inputs for DATA[1:7] are not used and these pins are not used as an I/O then it is recommended to leave these pins unconnected. See Note 11.
INIT_DONE	INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. See Note 11.
CLKUSR	CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to ground. See Note 11.
Differential I/O Pins				
DIFFIO_RX[##]p, DIFFIO_RX[##]n	DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on row and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
DIFFOUT_###p, DIFFOUT_###n	DIFFOUT_###p, DIFFOUT_###n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.
<i>External Memory Interface Pins</i>				
DQS[1:38][T,B], DQS[1:34][L,R]	DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in Quartus II software.
DQSn[1:38][T,B], DQSn[1:34][L,R]	DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in Quartus II software.
DQ[1:38][T,B], DQ[1:34][L,R]	DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in Quartus II software.
CQ[1:38][T,B], CQ[1:34][L,R]	CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	Connect unused pins as defined in Quartus II software.
CQn[1:38][T,B], CQn[1:34][L,R]	CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	Connect unused pins as defined in Quartus II software.
<i>Reference Pins</i>				

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
RUP[1:8]A, RUP[3,8]C	RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to the VCCIO of the bank in which the RUP pin resides or GND. When using OCT tie these pins to the required banks VCCIO through either a 25Ω or 50Ω resistor, depending on the desired I/O standard. Refer to the Stratix IV handbook for the desired resistor value for the I/O standard used.
RDN[1:8]A, RDN[3,8]C	RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to GND. When using OCT tie these pins to GND through either a 25Ω or 50Ω resistor depending on the desired I/O standard. Refer to the Stratix IV handbook for the desired resistor value for the I/O standard used.
DNU	DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, ground or any other signal. These pins must be left floating.
NC	NC	No Connect	Do not drive signals into these pins.	When designing for device migration these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.
Supply Pins (See Notes 13 and 14)				
VCC	VCC	Power	VCC supplies power to the core and periphery. Connect to 0.9V.	All VCC pins require a 0.9V supply. Use the Stratix IV Early Power Estimator to determine the current requirements for VCC and other power supplies. These pins may be tied to the same 0.9V plane as VCCHIP. With a proper isolation filter VCCD_PLL may be sourced from the same regulator as VCC. To successfully power-up and exit POR on production devices, fully power VCC before VCCAUX begins to ramp. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 5, 10 and 14.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to 0.9V, even if the PLL is not used.	You are required to connect these pins to 0.9V, even if the PLL is not used. With a proper isolation filter these pins may be sourced from the same regulator as VCC and/or VCCHIP. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 5 and 10.
VCCPT	VCCPT	Power	Power supply for the programmable power technology. Connect to 1.5V.	VCCPT can be connected to a 1.5V linear or low noise switching power supply. When VCCPT is source from a regulator that is shared with other voltage rails, VCCPT must be isolated from the other voltage rails. For data rates ≤ 6.5Gbps where VCCH_GXB requires 1.5V the VCCPT supply may be sourced from the same regulator as VCCH_GXB with the use of a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 5, 10, 12 and 15.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to 2.5V, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.	You are required to connect these pins to 2.5V, even if the PLL is not used. Use an isolated linear or low noise switching power supply. With a proper isolation filter these pins may be sourced from the same regulator as VCCAUX. For data rates ≤ 4.25Gbps where VCCA_[L,R] is 2.5V these pins may also be tied to the same regulator as VCCA_[L,R] with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 5, 10,12, and 15.
VCCAUX	VCCAUX	Power	Auxiliary supply for the programmable power technology. Connect to 2.5V.	VCCAUX can be connected to an isolated 2.5V linear or low noise switching power supply. With a proper isolation filter these pins may be sourced from the same regulator as VCCA_PLL. For data rates ≤ 4.25Gbps where VCCA_[L,R] is 2.5V these pins may also be tied to the same regulator as VCCA_[L,R] with a proper isolation filter. To successfully power-up and exit POR on production devices, fully power VCC before VCCAUX begins to ramp. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 5, 10, 12 and 15.

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	VCCIO[1:8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTTL 3.3V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), 3.0V PCI/PCI-X and LVTTTL 3.3V I/O standards.	Connect these pins to 1.2V, 1.5V, 1.8V, 2.5V or 3.0V supplies, depending on the I/O standard connected to the specified bank. When these pins require 2.5V they may be tied to the same regulator as VCC_CLKIN, VCCPGM and VCCPD, but only if each of these supplies require 2.5V sources. VCC_CLKIN has a set voltage of 2.5V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCPD as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 5 and 10.
VCCPGM	VCCPGM	Power	Configuration pins power supply. Can be connected to 1.8V, 2.5V or 3.0V depending on the particular design.	Connect this pin to either a 1.8V, 2.5V or 3.0V power supply. VCCPGM must ramp-up from 0V to VCCPGM within 100 ms when PORSEL is low or 4 ms when PORSEL is high to ensure successful configuration. When these pins require 2.5V they may be tied to the same regulator as VCC_CLKIN, VCCIO and VCCPD, but only if each of these supplies require 2.5V sources. VCC_CLKIN has a set voltage of 2.5V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPD and/or VCCIO as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 5 and 10.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	VCCPD[1:8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.0V or 2.5V. For 3.3V or 3.0V I/O standard connect VCCPD to 3.0V, and for 1.2V, 1.5V, 1.8V or 2.5V I/O standards connect VCCPD to 2.5V.	The VCCPD pins require a 2.5V or 3.0V power supply. VCCPD must ramp-up from 0V to VCCPD within 100 ms when PORSEL is low or 4 ms when PORSEL is high to ensure successful configuration. When these pins require 2.5V they may be tied to the same regulator as VCC_CLKIN, VCCPGM and VCCIO, but only if each of these supplies require 2.5V sources. VCC_CLKIN has a set voltage of 2.5V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCIO as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 5 and 10.
VCC_CLKIN[3,4,7,8]C	VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks. Connect to 2.5V.	Connect these pins to 2.5V power source. These pins may be tied to the same regulator as VCCIO, VCCPGM and VCCPD, but only if each of these supplies require 2.5V sources. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 5.
VCCBAT	VCCBAT	Power	Battery back-up power supply for design security volatile key register.	Connect this pin to a Non-volatile battery power source in the range of 1.2V - 3.3V when using design security volatile key. 3.0V is the typical power selected for this supply. When not using the volatile key, tie this to a 3.0V supply or GND. Do not share this source with other FPGA power supplies.
GND	GND	Ground	Device ground pins.	All GND pins must be connected to the board ground plane.
VREF[1:8][A,C], VREF[2,3,4,5,7,8]B	VREF[1:8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.	If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 5.
Transceiver Pins (See Notes 13 through 15)				
VCCHIP_[L,R]	NA	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device. Connected to 0.9V.	All VCCHIP_[L,R] pins require a 0.9V supply. When not using HIP these pins may be connected to GND. These pins may be tied to the same 0.9V plane as VCC. With a proper isolation filter these pins may be sourced from the same regulator as VCCD_PLL. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 5 and 10.

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCR_[L,R]	NA	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device. Connect to 1.1 V.	VCCR_[L,R] can be connected to a 1.1V linear or low noise switching regulator. Some Stratix IV devices connect VCCR_L and VCCT_L together, and connect VCCR_R and VCCT_R together. VCCR_L pins must be tied to the same linear regulator as VCCT_L. Also, VCCR_R pins must be tied to the same linear regulator as VCCT_R. For data rates less than 6.5Gbps these pins may be tied to the same 1.1V plane as VCCL_GXB[L,R]. However, for better jitter performance at high data rates this plane should be isolated from all other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 5, 9, 10, 12 and 15.
VCCT_[L,R]	NA	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device. Connect to 1.1 V.	VCCT_[L,R] can be connected to a 1.1V linear or low noise switching regulator. Some Stratix IV devices connect VCCR_L and VCCT_L together, and connect VCCR_R and VCCT_R together. VCCR_L pins must be tied to the same linear regulator as VCCT_L. Also, VCCR_R pins must be tied to the same linear regulator as VCCT_R. For data rates less than 6.5Gbps these pins may be tied to the same 1.1V plane as VCCL_GXB[L,R]. However, for better jitter performance at high data rates this plane should be isolated from all other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 5, 9, 10, 12 and 15.
VCCL_GXB[L,R][0:3]	NA	Power	Analog power, block level clock distribution, Connected to 1.1V.	VCCL_GXB[L,R] can be connected to a 1.1V linear or low noise switching regulator. These pins may be tied to the same 1.1V plane as VCCT_[L,R] and/or VCCR_[L,R]. However, for better jitter performance at high data rates this plane should be isolated from all other power supplies. For the best jitter performance, provide each quad its own power source. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 5, 9, 10, 12 and 15.
VCCH_GXB[L,R][0:3]	NA	Power	Analog power, block level TX buffers. Connect to 1.4 V or 1.5 V.	VCCH_GXB[L,R] can be connected to a 1.4V or 1.5V linear or low noise switching regulator. Connect these pins to 1.4V if the transmitter channel data rate is > 6.5Gbps. Connect these pins to 1.5V if the transmitter channel data rate is ≤ 6.5Gbps. For data rates ≤ 6.5Gbps where VCCH_GXB is 1.5V these pins may be sourced from the same regulator as VCCTPT with a proper isolation filter. For data rates ≤ 6.5Gbps it is possible to use 1.4V from a source that is already utilized on the board as long as VCCH_GXB is properly isolated from the other supply. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 5, 9, 10, 12 and 15.
VCCA_[L,R]	NA	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device. Connect to 2.5V or 3.0 V.	VCCA_[L,R] can be connected to a 2.5V or 3.0V linear or low noise switching regulator. Connect these pins to 3.0V if the TX PLL and/or RX CDR are configured at a base data rate > 4.25Gbps. Connect these pins to 2.5V or 3.0V if the TX PLL and/or RX CDR are configured at a base data rate ≤ 4.25Gbps (See Note 13). For data rates ≤ 4.25Gbps, if VCCA_[L,R] is 2.5V these pins may be sourced from the same linear regulator as VCCAUX and/or VCCA_PLL with a proper isolation filter. Decoupling depends on the design decoupling requirements of the specific board design. See Notes 5, 9, 10, 12 and 15.
GXB_RX_[L,R][0:15]p	NA	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. (Note 6) Connect all unused GXB_RXp pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 2.
GXB_RX_[L,R][0:15]n	NA	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. (Note 6) Connect all unused GXB_RXn pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 2.
GXB_TX_[L,R][0:15]p	NA	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXp pins floating. See Note 2.

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
GXB_TX_[L,R][0:15]n	NA	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXn pins floating. See Note 2.
REFCLK_[L,R][0:7]p, GXB_CMURX_[L,R][0:7]p	NA	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.	These pins may be used for either reference clocks or CMU receiver channels. Switching between the two functions requires reprogramming the entire device. These pins should be AC-coupled when used as reference clocks (see note 7). These pins may be AC-coupled or DC-coupled when used as CMU receiver channels (Note 6). Connect all unused GXB_CMURX_[L,R][p]n pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Notes 3 and 4.
REFCLK_[L,R][0:7]n, GXB_CMURX_[L,R][0:7]n	NA	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.	These pins may be used for either reference clocks or CMU receiver channels. Switching between the two functions requires reprogramming the entire device. These pins should be AC-coupled when used as reference clocks (see note 7). These pins may be AC-coupled or DC-coupled when used as CMU receiver channels (Note 6). Connect all unused GXB_CMURX_[L,R][p]n pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Notes 3 and 4.
GXB_CMUTX_[L,R][0:7]p, GXB_CMUTX_[L,R][0:7]n	NA	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_CMUTX_[L,R][p] and GXB_CMUTX_[L,R][n] floating. See Note 4.
RREF_[L,R][0:1]	NA	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.	If any REFCLK pin or transceiver channel on one side (left or right) of the device is used, you must connect each RREF pin on that side of the device to its own individual 2.00-kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

- This pin connection guideline is created based on the Stratix IV GX and Stratix IV E. Shaded cells indicate pin name differences between the Stratix IV GX and Stratix IV E devices.
- There are up to 16 GXB_RX[L,R] and GXB_TX[L,R] pairs on each side of the device. Transceiver signals GXB_RX[0:15] and GXB_TX[0:15] are device specific.
 - There are 8 channels in 2 transceiver blocks on the right side of the device for a total of 8 channels for the: EP4SGX70DF29, EP4SGX110DF29 and EP4SGX230DF29 devices.
 - There are 8 channels in 2 transceiver blocks on the left and right side of the device for a total of 16 channels for the: EP4SGX290FH29, EP4SGX360FH29, EP4SGX110FF35, EP4SGX230FF35, EP4SGX290FF35, EP4SGX360FF35, EP4SGX230HF35, EP4SGX290HF35, EP4SGX360HF35 and EP4SGX530HF35 devices.
 - There are 12 channels in 3 transceiver blocks on the left and right side of the device for a total of 24 channels for the: EP4SGX230KF40, EP4SGX290KF40, EP4SGX360KF40, EP4SGX530KF40, EP4SGX290KF45 and EP4SGX360KF45 devices.
 - There are 16 channels in 4 transceiver blocks on the left and right side of the device for a total of 32 channels for the EP4SGX530NF45 device.
- Dual purpose CMU receiver channels. Can be used either as reference clock or CMU receiver channels in devices with 5th and 6th transceiver channels.
- Only available in devices with CMU receiver channels. Devices with CMU receiver channels are indicated in the part number by either "H", "K" or "N" in the "Transceiver Count" position in the ordering code.
- Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To assist in decoupling analysis Altera's Power Distribution Network (PDN) design tool serves as an excellent decoupling analysis tool.
[Power Distribution Network Design Tool](#)
- For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapt
- In PCI Express configuration, DC-coupling is allowed on REFCLK if the selected REFCLK I/O standard is HCSL (High-Speed Current Steering Logic)
- The transmitter channel data rate could be equal to the TX PLL base data rate, or half of the TX PLL data rate, or quarter of the TX PLL base data rate depending on the local clock divider setting of 1, 2 or 4. For example, if the TX PLL base data rate is configured to support 6.0Gbps and the local clock divider value of 2 is used, the transmitter channel runs at 3Gbps. In this case, the VCCA_[L,R] pins must be connected to 3.0V as the TX PLL base data rate > 4.25Gbps.
- If one or more transceivers are used on a particular side of the device (left [L] or right [R]) all of the transceiver power pins on that side of the device must be connected to its required power supply, except for VCCHIP which may be connected to GND if not using the HIP. For any unused quad VCC_GXB may be tied to either 1.4V or 1.5V
 In addition, if none of the transceivers are used on one side then the transceiver power pins on that side may be tied to GND.

**Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6**

You should create a Quartus II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

Stratix IV GX Pin Name	Stratix IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
------------------------	-----------------------	---------------------------------------	-----------------	-----------------------

- 10) Use the Stratix IV Early Power Estimator to determine the current requirements for VCC and other power supplies.
- 11) These dual purpose configuration pins can only be used as configuration pins but not regular I/O in F780 of EP4SGX360 and EP4SGX290.
- 12) These supplies may share power planes across multiple Stratix IV devices.
- 13) Examples 1 - 3 and Figures 1 - 3 illustrate power supply sharing guidelines that are data rate dependent. Example 4 and Figure 4 illustrate the power supply sharing guidelines for the Stratix IV E.
 Example 1 and Figure 1, "Power Regs <= 4.25Gbps", show recommendations for designs using the Stratix IV GX that will not exceed 4.25Gbps.
 Example 2 and Figure 2, "Power Regs > 4.25Gbps <= 6.5Gbps", show recommendations for designs using the Stratix IV GX that are between 4.25Gbps and 6.5Gbps.
 Example 3 and Figure 3, "Power Regs > 6.5Gbps", show recommendations for designs using the Stratix IV GX that exceed 6.5Gbps.
 Example 4 and Figure 4, "Power Regs Stratix IV E", show recommendations for designs that use the non-transceiver based Stratix IV E.
- 14) Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
- 15) Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response.
 Line Regulation < 0.4%
 Load Regulation < 1.2%
- 16) The JTAG pins TDI, TDO, TCK, TMS and TRST are powered by VCCPD1A.

Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

Example 1. Stratix IV GX Power Supply Sharing Guidelines for Data Rates <= 4.25Gpbs

Example Requiring 5 Power Regulators

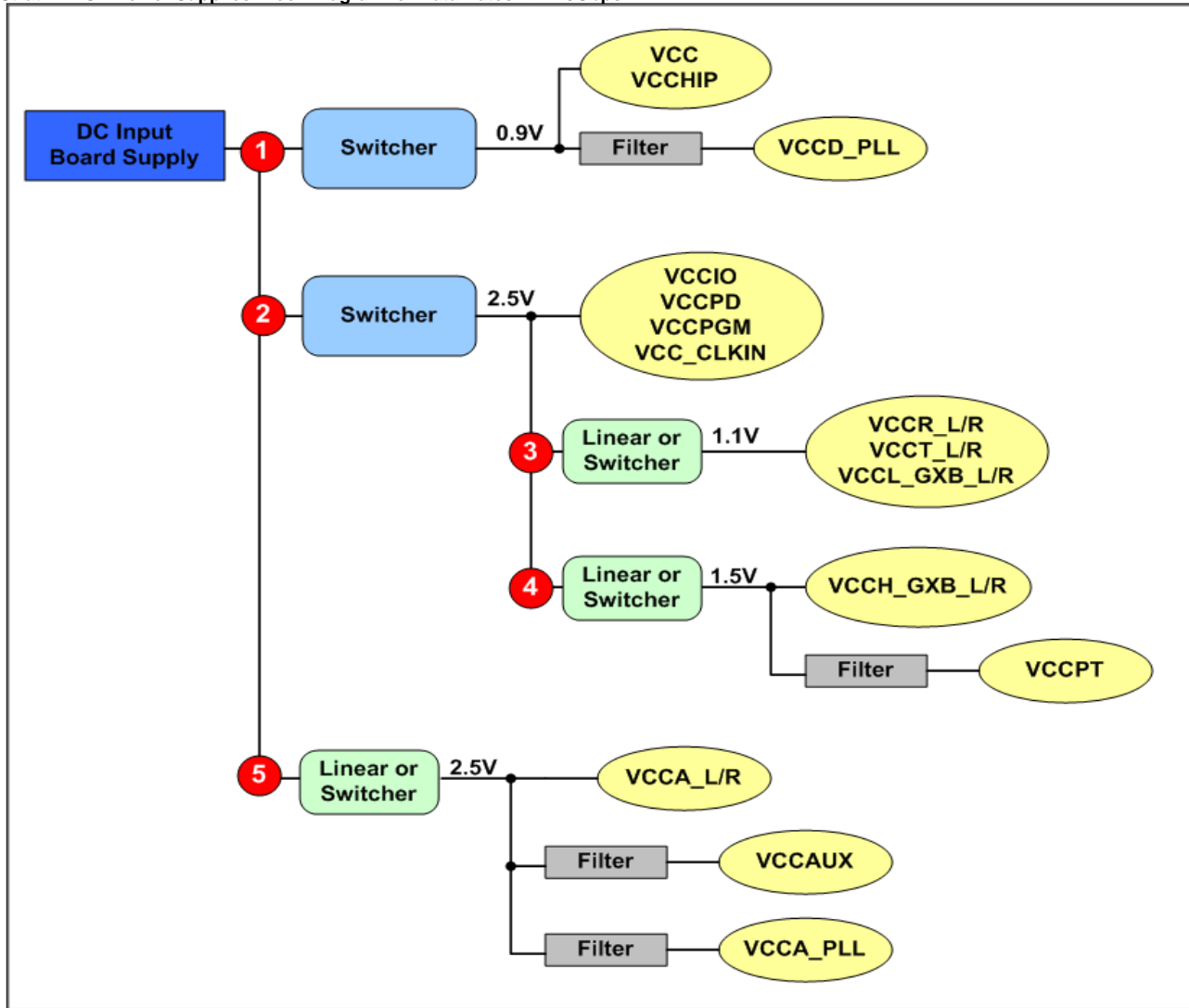
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC (**)	1	0.9	± 30mV	Switcher	Share	VCC and VCCHIP may share regulators. If not using HIP, VCCHIP may be tied to GND
VCCHIP_[L,R]						
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	May be able to share VCCD_PLL with VCC and VCCHIP with a proper isolation filter. If not sharing the regulator with VCC and/or VCCHIP the VCCD_PLL supply should not exceed a tolerance of ± 5%.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	2	Varies	± 5%	Switcher	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B						
VCCPGM						
VCC_CLKIN[3,4,7,8]C						
VCCR_[L,R]	3	1.1	± 5%	Linear or Switcher (*)	Share	Some Stratix IV devices connect VCCR_L and VCCT_L together, and connect VCCR_R and VCCT_R together. For these devices VCCR_L and VCCT_L must be sourced from the same linear or low noise switching regulator and VCCR_R and VCCT_R must be sourced from the same regulator. The left [L] and [R] may share the same regulator. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE (Early Power Estimation) tool within Quartus II to assist in determining the power required for your specific design.
VCCT_[L,R]						
VCCL_GXB[L,R][0:3]						
VCCH_GXB[L,R][0:3]	4	1.5	± 50mV	Linear or Switcher (*)	Share	May be able to share VCCPT with VCCH_GXB with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE tool to assist in determining the power required for your specific design. If not sharing a regulator the VCCH_GXB supply should not exceed a tolerance of ± 5%.
VCCPT						
VCCA_[L,R]	5	2.5	± 5%	Linear or Switcher (*)	Share	May be able to share VCCA_PLL with VCCAUX and VCCA with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCAUX (**)						
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]						

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 15.

** To successfully power-up and exit POR on production devices, fully power VCC before VCCAUX begins to ramp.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix IV GX device for data rates less than or equal to 4.25Gbps is provided in Figure 1.

Figure 1. Example Stratix IV GX Power Supplies Block Diagram for Data Rates <=4.25Gbps



Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

Example 2. Stratix IV GX Power Supply Sharing Guidelines for Data Rates Between 4.25Gbps and 6.5Gbps

Example Requiring 5 Power Regulators

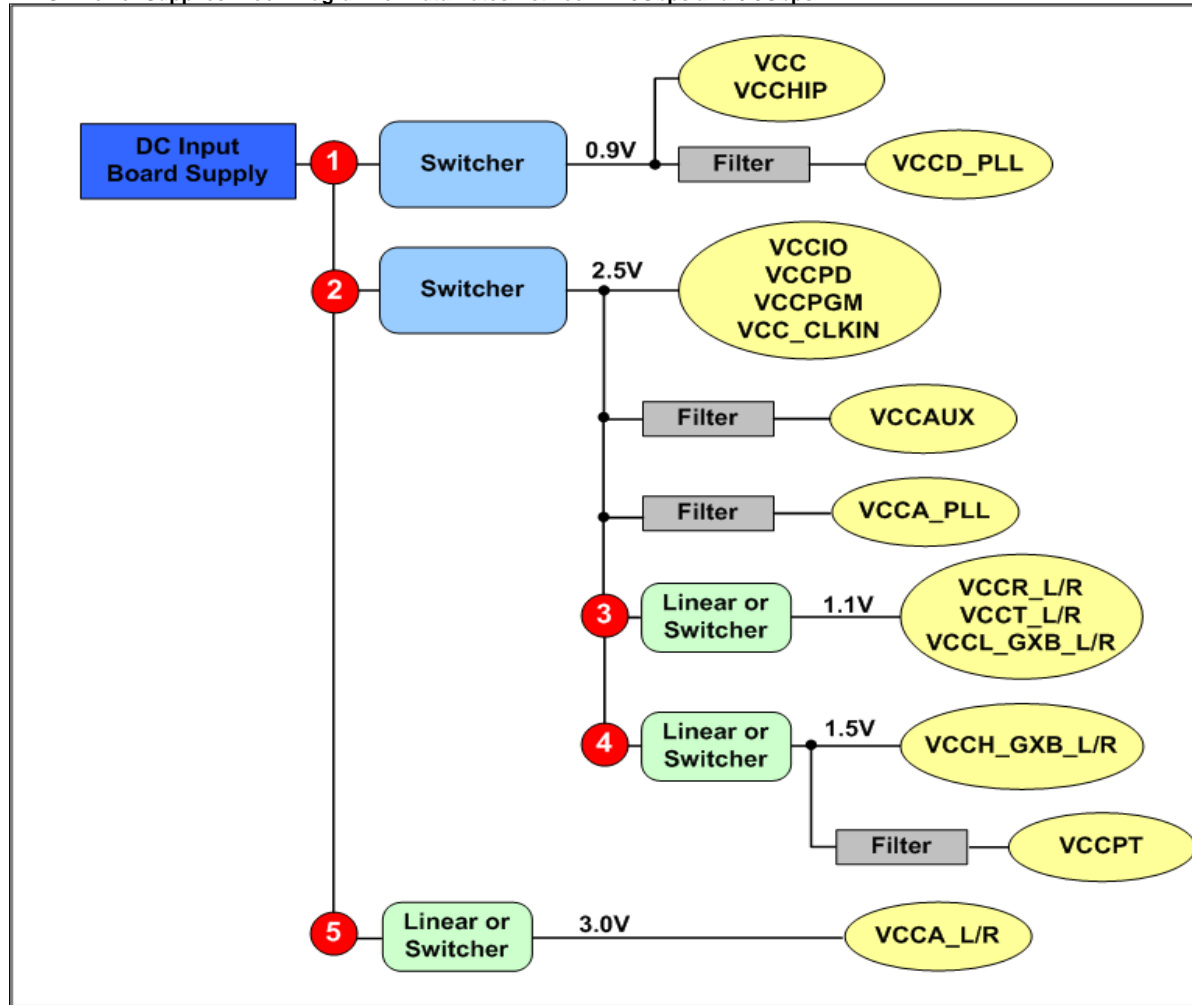
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes					
VCC (**) VCCHIP_[L,R]	1	0.9	± 30mV	Switcher	Share	VCC and VCCHIP may share regulators. If not using HIP, VCCHIP may be tied to GND					
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	May be able to share VCCD_PLL with VCC and VCCHIP with a proper isolation filter. If not sharing the regulator with VCC and/or VCCHIP the VCCD_PLL supply should not exceed a tolerance of ± 5%.					
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B VCCPGM VCC_CLKIN[3,4,7,8]C VCCAUX (**) VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	2	Varies	± 5%	Switcher	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.					
		2.5			Isolate/share	VCCAUX and VCCA_PLL may be able to share a regulator with a proper isolation filter.					
VCCR_[L,R] VCCT_[L,R] VCCL_GXB[L,R][0:3]	3	1.1	± 5%	Linear or Switcher (*)	Share	Some Stratix IV devices connect VCCR_L and VCCT_L together, and connect VCCR_R and VCCT_R together. For these devices VCCR_L and VCCT_L must be sourced from the same linear or low noise switching regulator and VCCR_R and VCCT_R must be sourced from the same regulator. The left [L] and [R] may share the same regulator. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE (Early Power Estimation) tool within Quartus II to assist in determining the power required for your specific design.					
VCCH_GXB[L,R][0:3] VCCPT						4	1.5	± 50mV	Linear or Switcher (*)	Isolate	May be able to share VCCPT with VCCH_GXB with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE tool to assist in determining the power required for your specific design. If not sharing a regulator the VCCH_GXB supply should not exceed a tolerance of ± 5%.
VCCA_[L,R]										5	3.0

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 15.

** To successfully power-up and exit POR on production devices, fully power VCC before VCCAUX begins to ramp.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix IV GX device for data rates between 4.25Gbps and 6.5Gbps is provided in Figure 2.

Figure 2. Example Stratix IV GX Power Supplies Block Diagram for Data Rates Between 4.25Gbps and 6.5Gbps



Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

Example 3. Stratix IV GX Power Supply Sharing Guidelines for Data Rates > 6.5Gbps

Example Requiring 7 Power Regulators

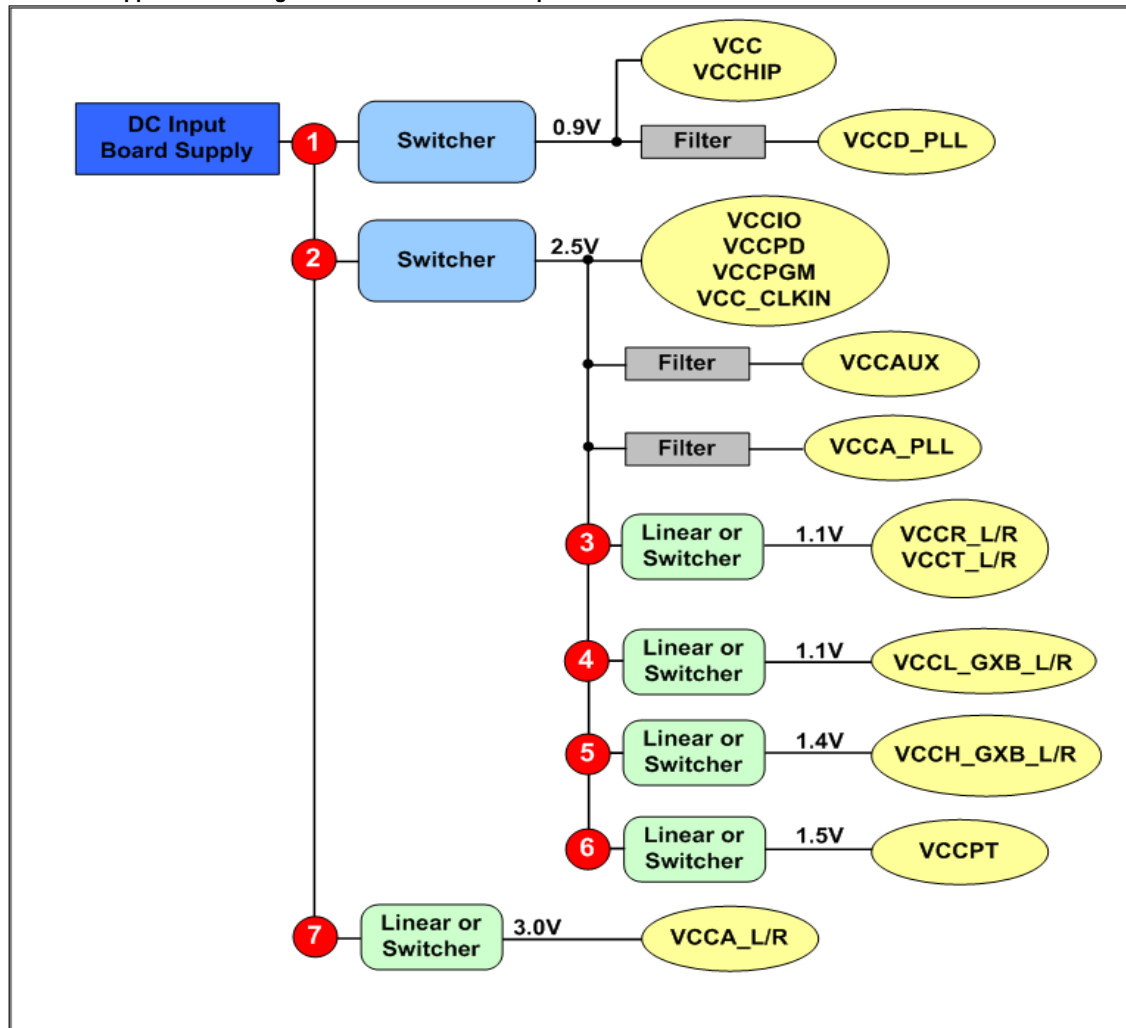
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC (**) VCCHIP_[L,R]	1	0.9	± 30mV	Switcher	Share	VCC and VCCHIP may share regulators. If not using HIP, VCCHIP may be tied to GND
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	May be able to share VCCD_PLL with VCC and VCCHIP with a proper isolation filter. If not sharing the regulator with VCC and/or VCCHIP the VCCD_PLL supply should not exceed a tolerance of ± 5%.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B VCCPGM VCC_CLKIN[3,4,7,8]C	2	Varies	± 5%	Switcher	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCAUX (**) VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]		2.5			Isolate/share	
VCCR_[L,R] VCCT_[L,R]	3	1.1	± 5%	Linear or Switcher (*)	Share	Some Stratix IV devices connect VCCR_L and VCCT_L together, and connect VCCR_R and VCCT_R together. For these devices VCCR_L and VCCT_L must be sourced from the same linear or low noise switching regulator and VCCR_R and VCCT_R must be sourced from the same regulator. The left [L] and [R] may share the same regulator. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE (Early Power Estimation) tool within Quartus II to assist in determining the power required for your specific design.
VCCL_GXB[L,R][0:3]						
VCCH_GXB[L,R][0:3]	5	1.4	± 5%	Linear or Switcher (*)	Isolate	Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCPT	6	1.5	± 50mV	Linear or Switcher (*)	Isolate	Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCA_[L,R]	7	3.0	± 5%	Linear or Switcher (*)	Isolate	Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE tool to assist in determining the power required for your specific design.

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 15.

** To successfully power-up and exit POR on production devices, fully power VCC before VCCAUX begins to ramp.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix IV GX device for data rates greater than 6.5Gbps is provided in Figure 3.

Figure 3. Example Stratix IV GX Power Supplies Block Diagram for Data Rates > 6.5Gbps



Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6

Example 4. Stratix IV E Power Supply Sharing Guidelines (non-transceiver device)

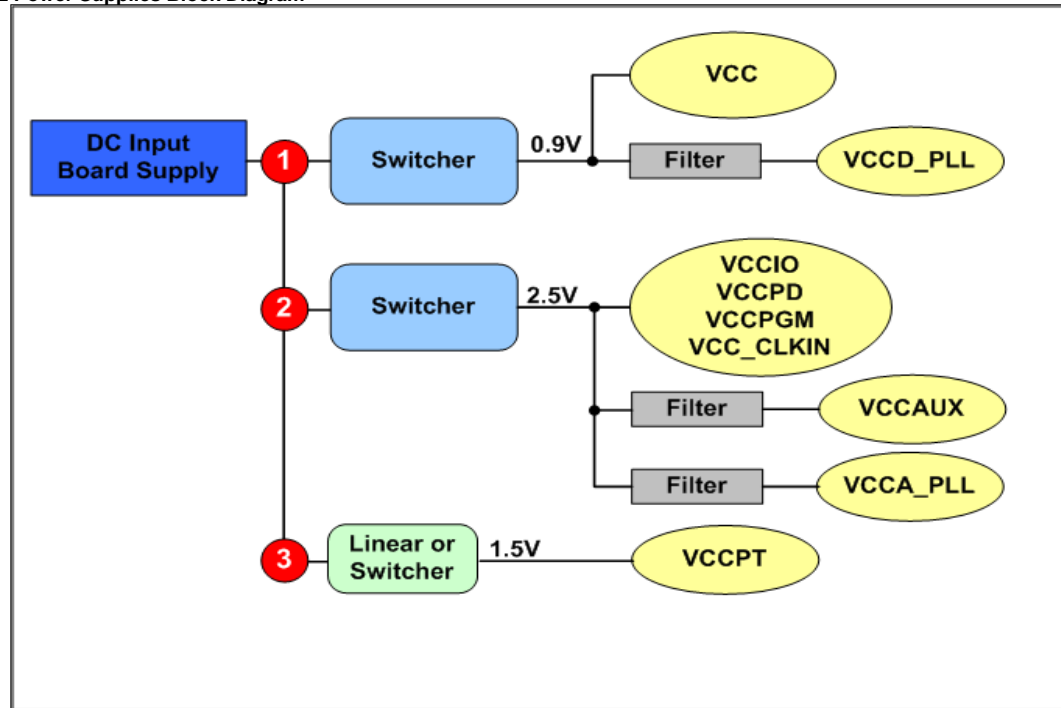
Example Requiring 3 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC (**)	1	0.9	± 30mV	Switcher	Share	May be able to share VCCD_PLL with VCC with a proper isolation filter. If not sharing the regulator with VCC the VCCD_PLL supply should not exceed a tolerance of ± 5%.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	
VCCAUX (**)	2	2.5	± 5%	Switcher	Share	May be able to share VCCA_PLL with VCCAUX with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]		Varies			Share if 2.5V	
VCC_CLKIN[3,4,7,8]C						
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	2	Varies	± 5%	Switcher	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B						
VCCPGM						
VCCPT	3	1.5	± 50mV	Linear or Switcher	Share	Depending on the regulator capabilities this supply may be shared with multiple Stratix IV devices. Use the EPE tool to assist in determining the power required for your specific design.

** To successfully power-up and exit POR on production devices, fully power VCC before VCCAUX begins to ramp.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Stratix IV E device is provided in Figure 4.

Figure 4. Example Stratix IV E Power Supplies Block Diagram



**Stratix® IV GX and Stratix IV E Device Family Pin Connection Guidelines
PCG-01005-1.6**

Revision History

Revision	Description of Changes	Date
1.0	Initial Release.	10/9/2008
1.1	updated figures 1 & 2 diagrams. Corrected GXB_RX unused recommendations, VCCPGM and VCCPD guidelines, Minor edits	11/17/2008
1.2	Add power Reg 4.25 - 6.5Gbps, updated > 6.5G diagram,	5/1/2009
1.3	Add Stratix IV E Power Reg page, Changed Example 2 and Figure 2, Note 13, VCCPT and VCCH_GXB connection guidelines.	6/5/2009
1.4	Changed title of document, updated example and figure titles to indicate GX or E device use. Updated note 13. Added note 15 and VCCR/VCCT/VCCL_GXB/VCCH_GXB/VCCA to include switcher capabilities, Rearranged the tables in examples to match regulator numbers.	8/30/2009
1.5	Added note regarding VCC/VCCAUX power on sequencing. Changed TDI and TMS pull-up to 1k - 10 kΩ. Changed PORSEL description.	1/20/2010
1.6	Removed "Preliminary" status, Added Note 16, Added to CLKIN and PLL[*]CLK descriptions. Updated GND guideline, nCSO and ASDO Pin Type.	6/22/2011