

DSP Development Board Stratix II Edition

Rev 02

Revision History		
Date	Change Description	Rev
10/21/03	Started design	01
2/5/04	Sent out schematic for first design review	01
7/30/04	Started Rev02 changed per document Maine_board_bringup.doc	02

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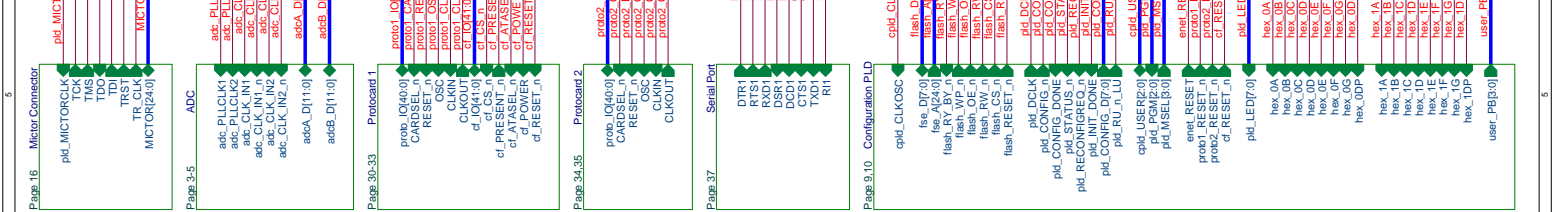
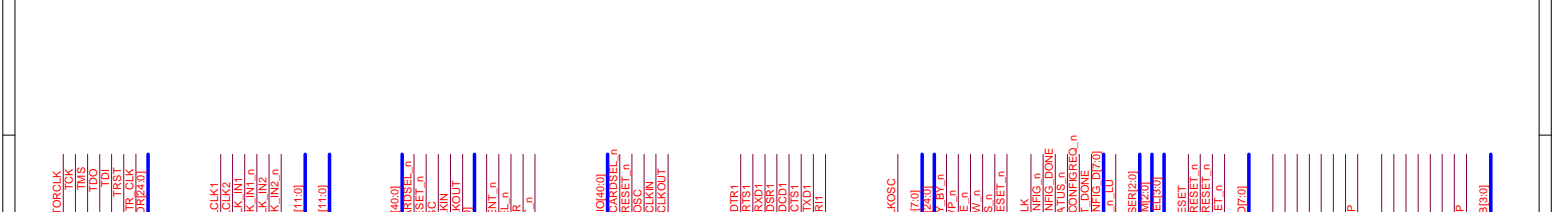
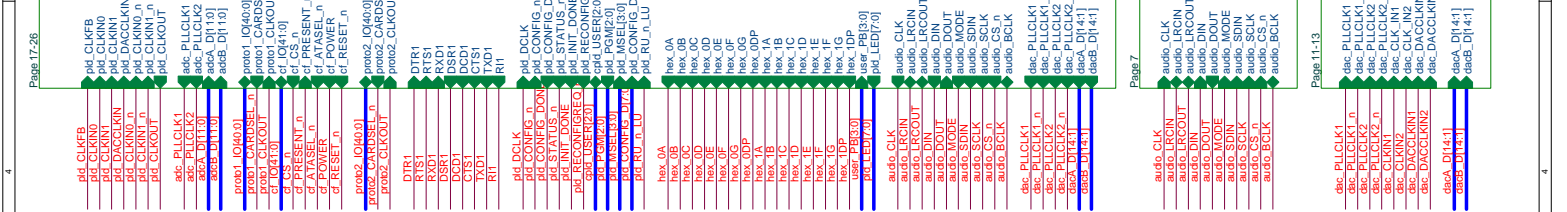
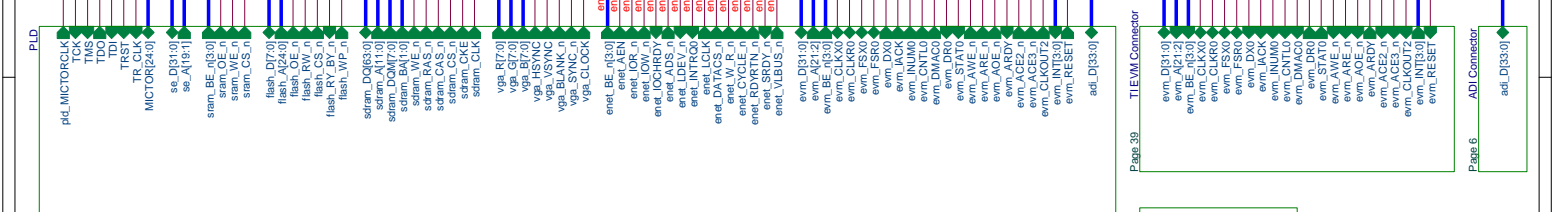
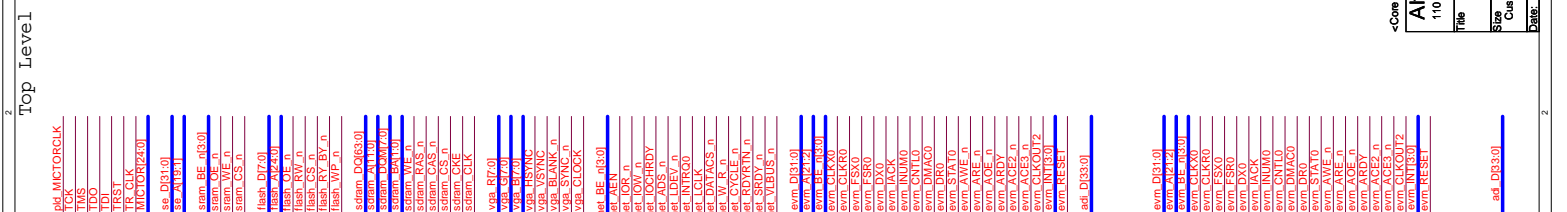
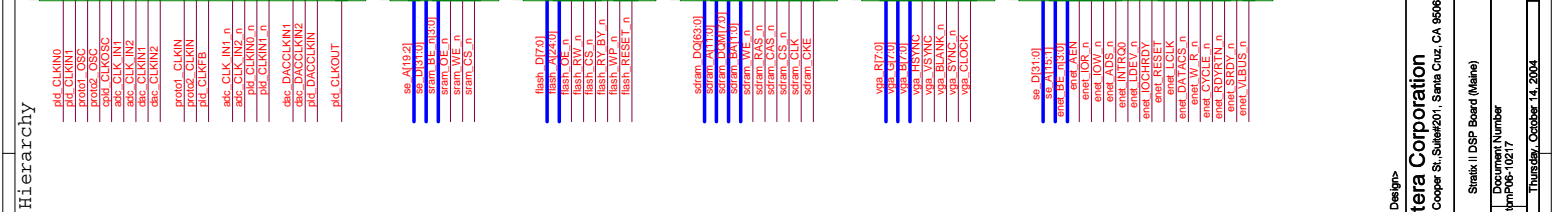
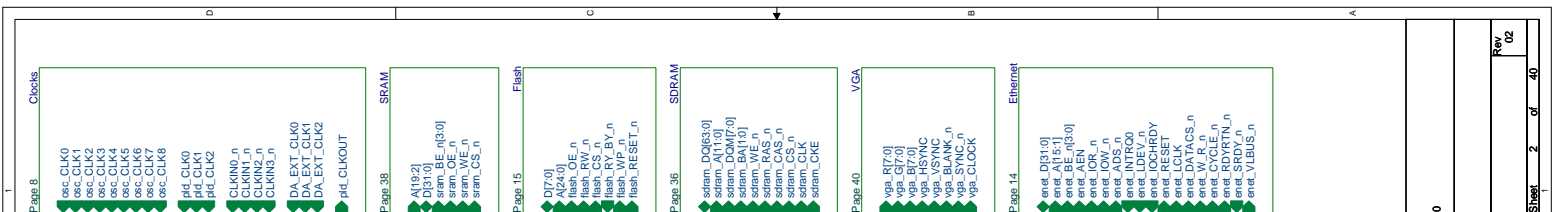
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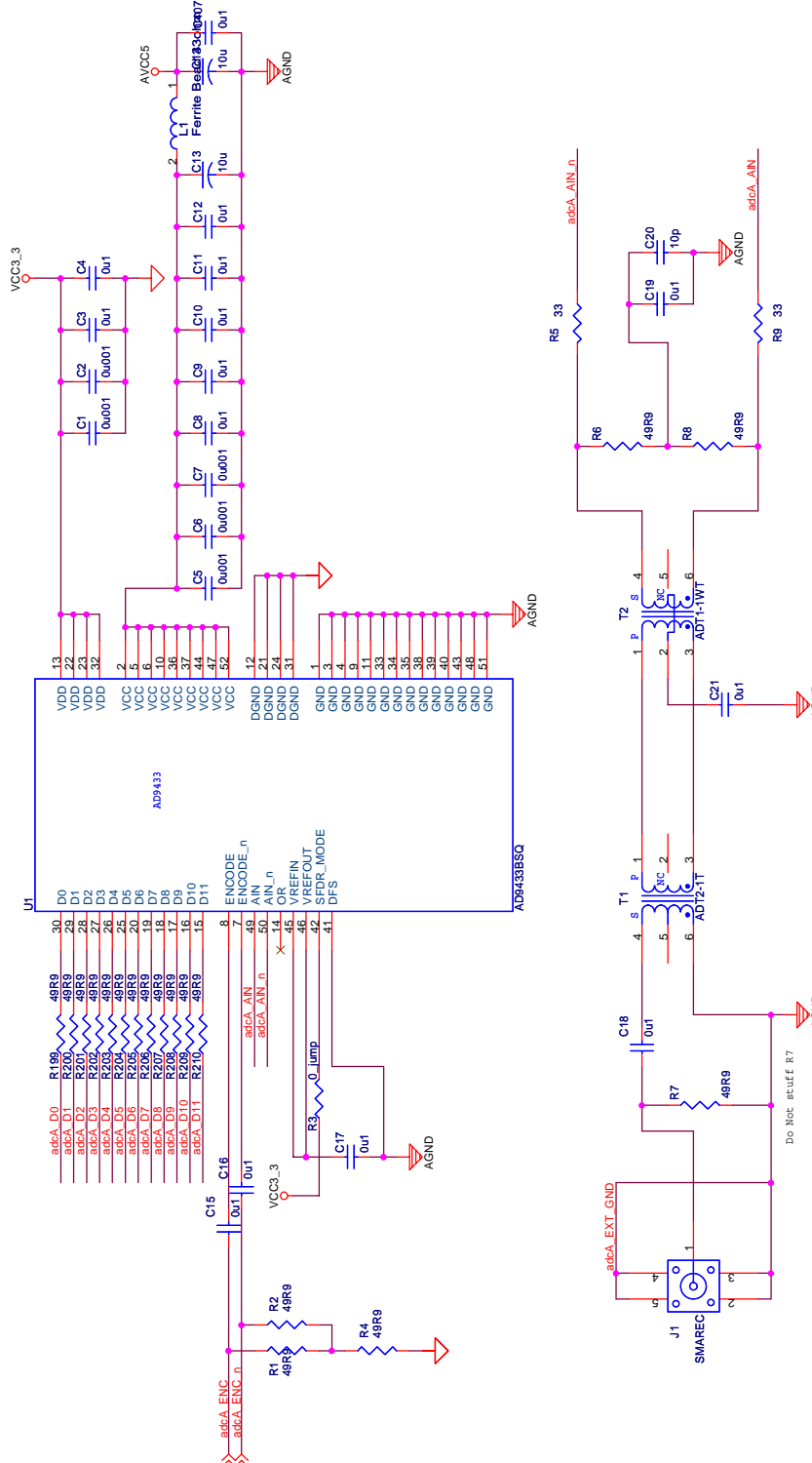
Title Stratix II DSP Board (Maine)

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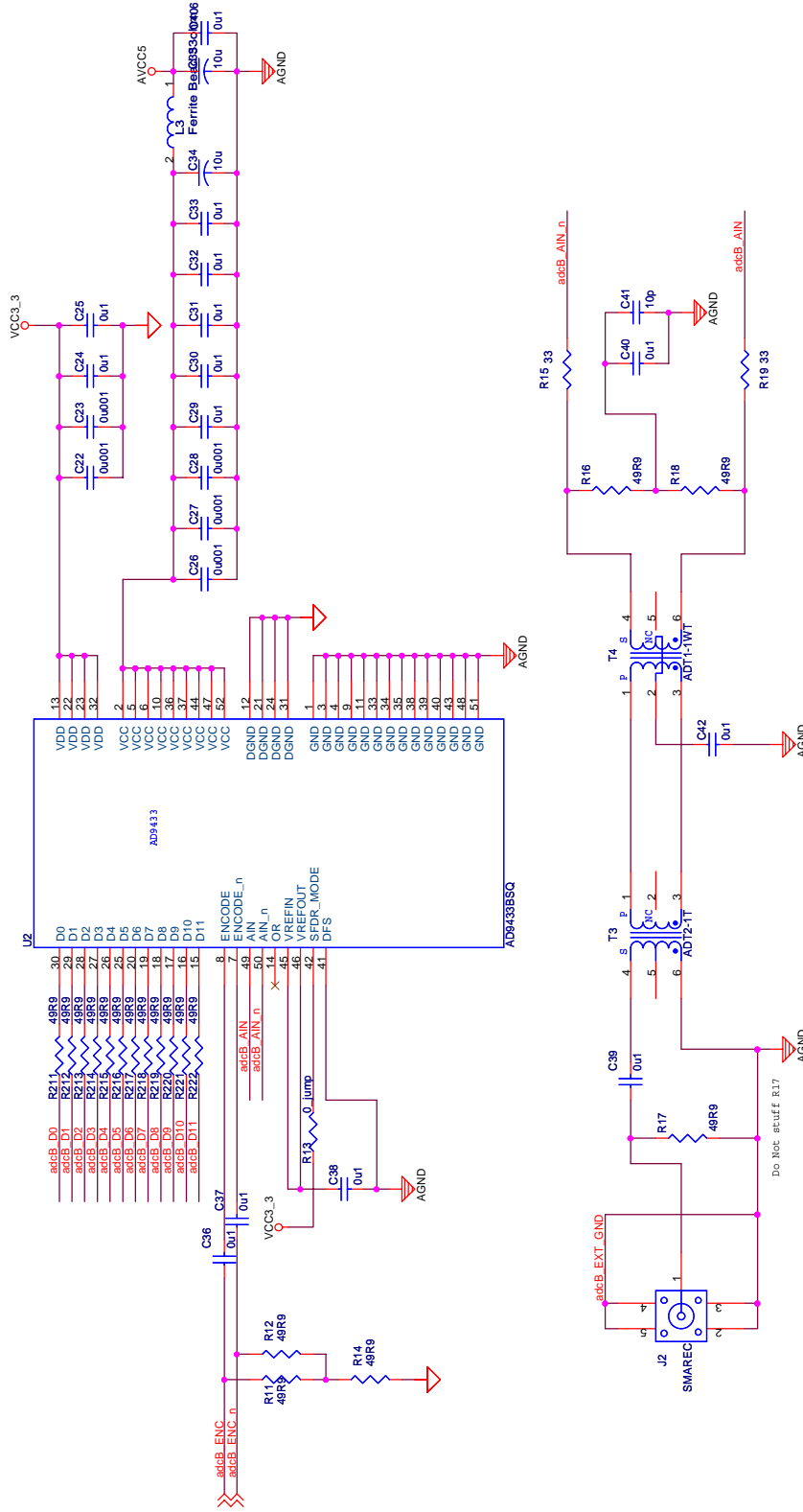


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adcB_D11(0)



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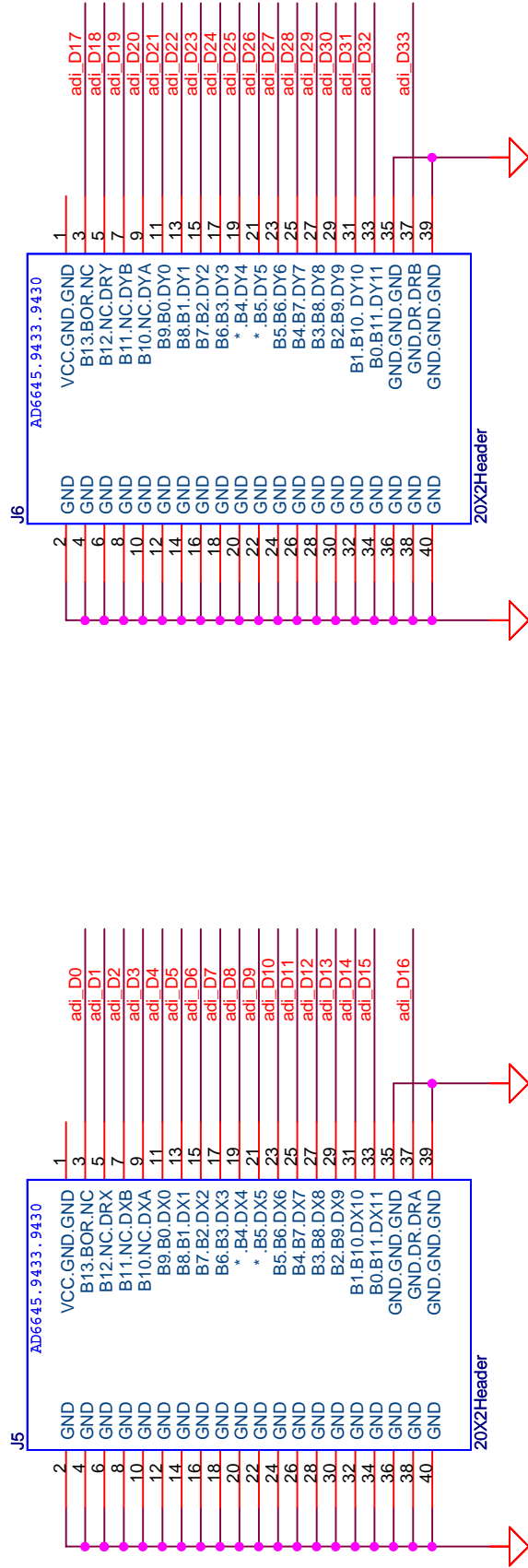
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ADI Connector

adi_D[33:0]



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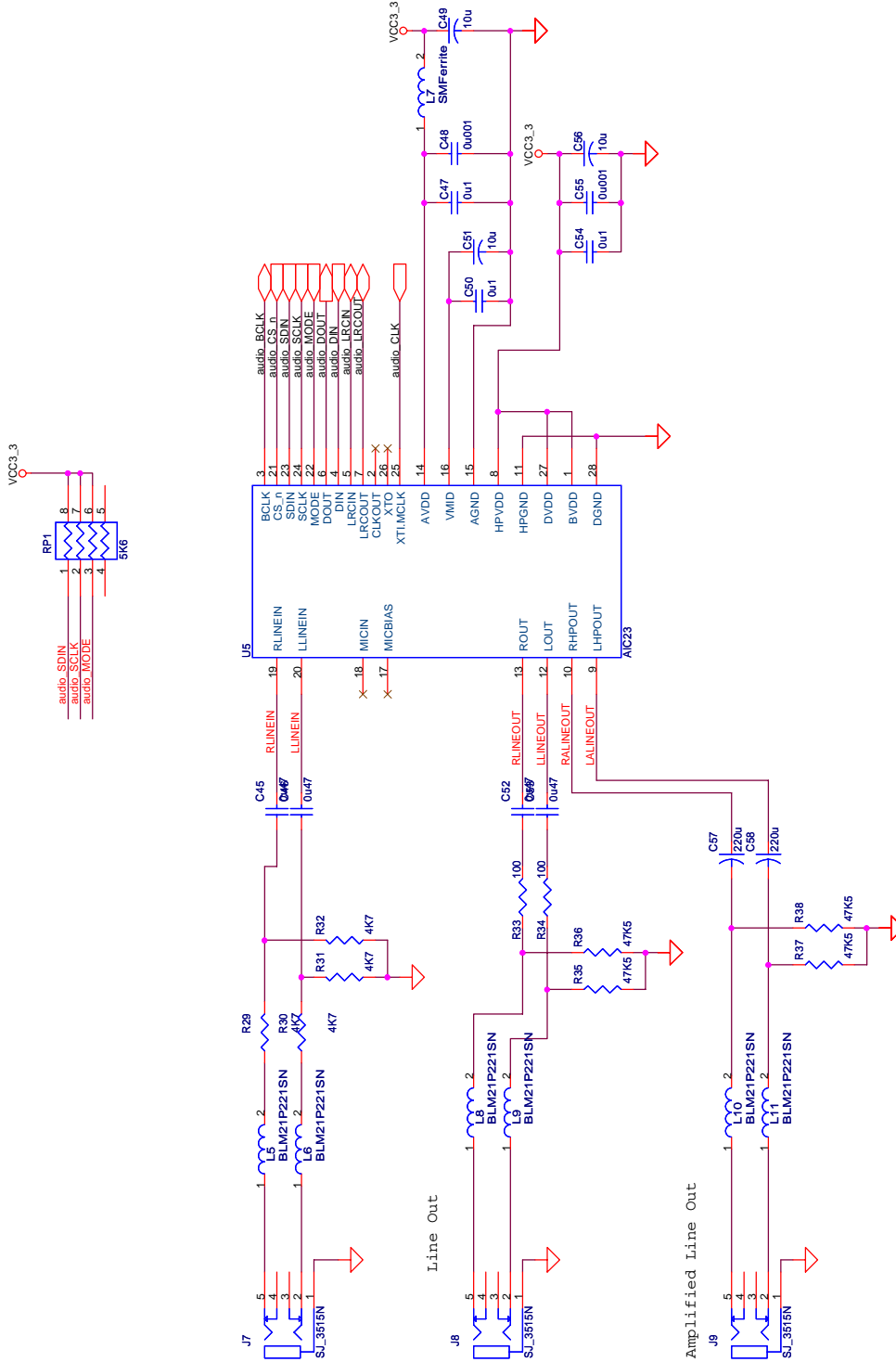
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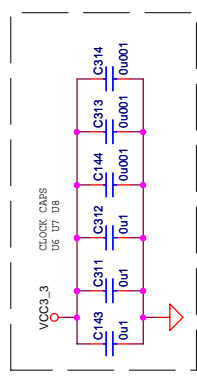
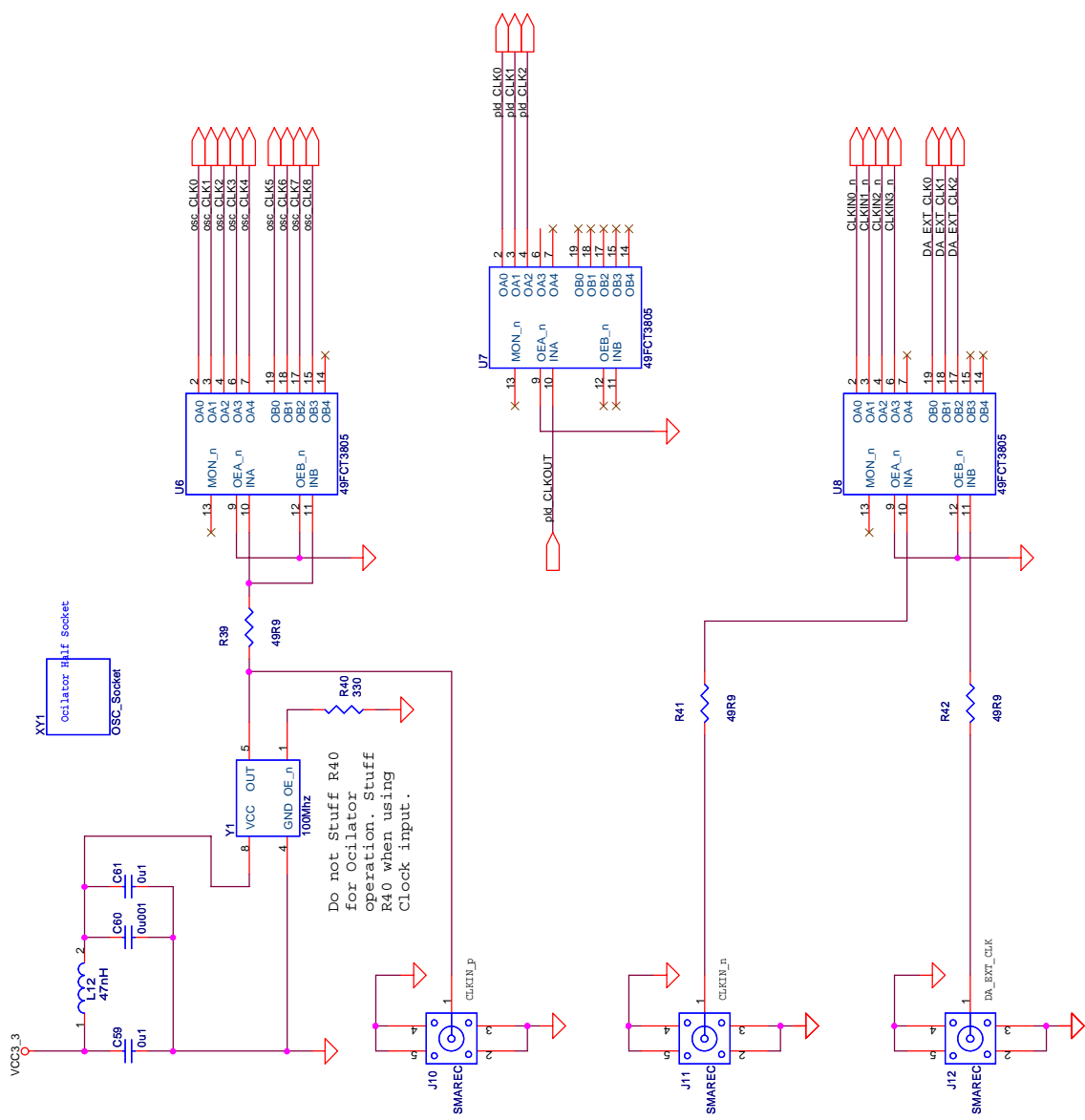
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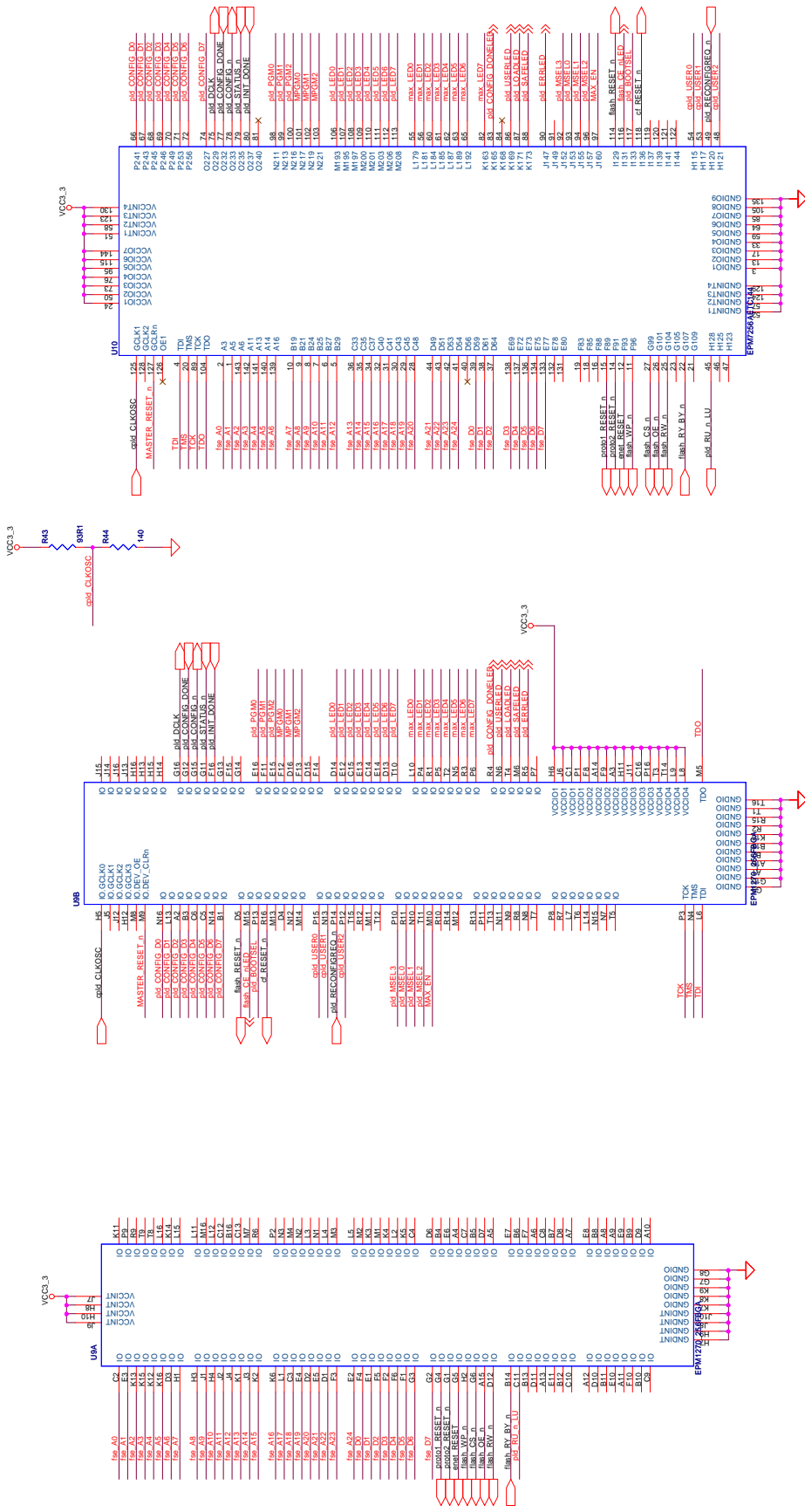
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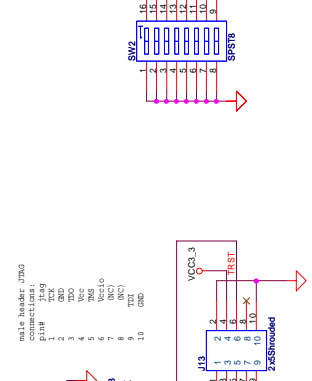
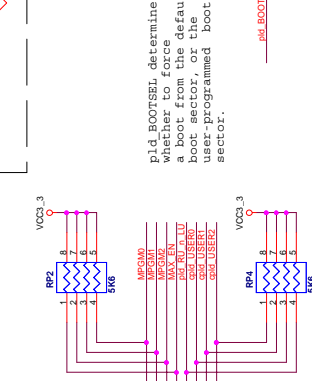
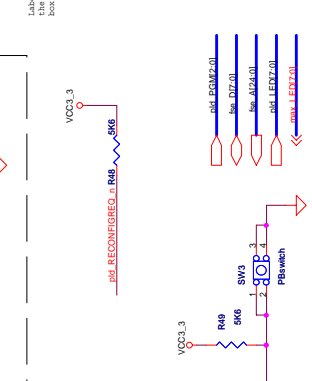
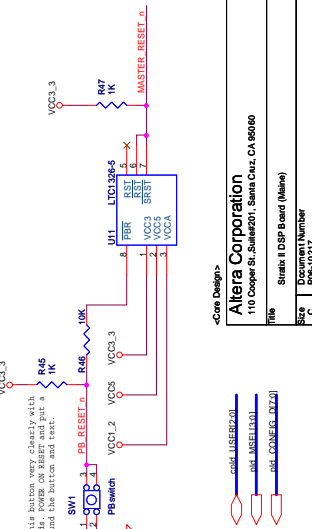
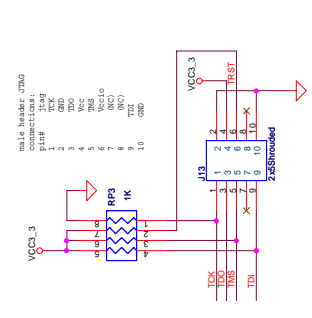


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Configuration PLD



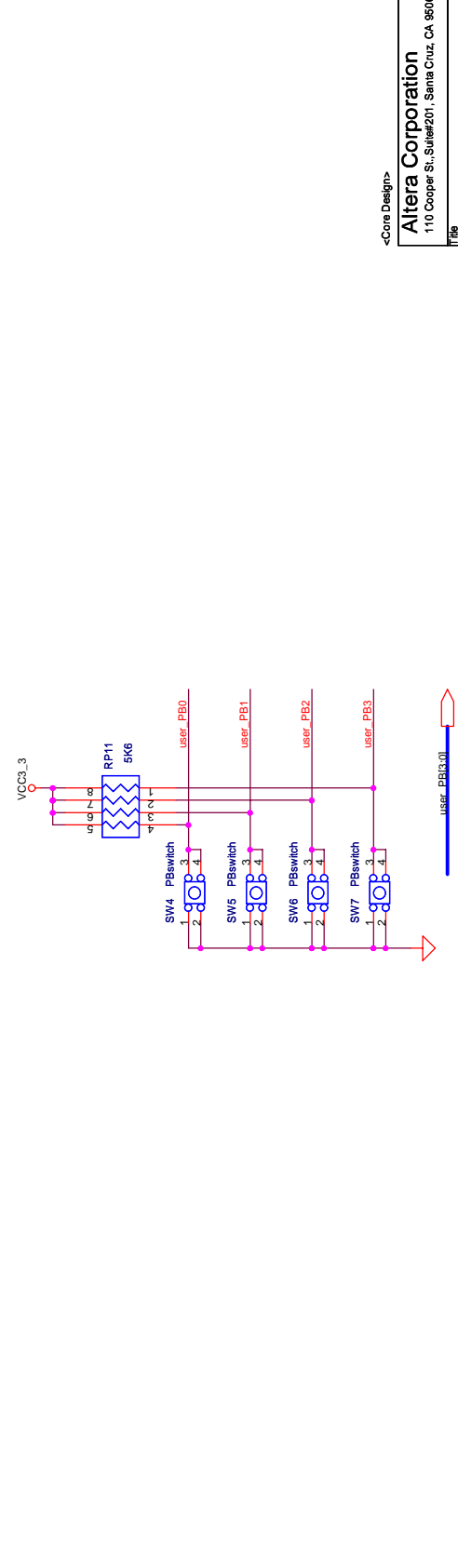
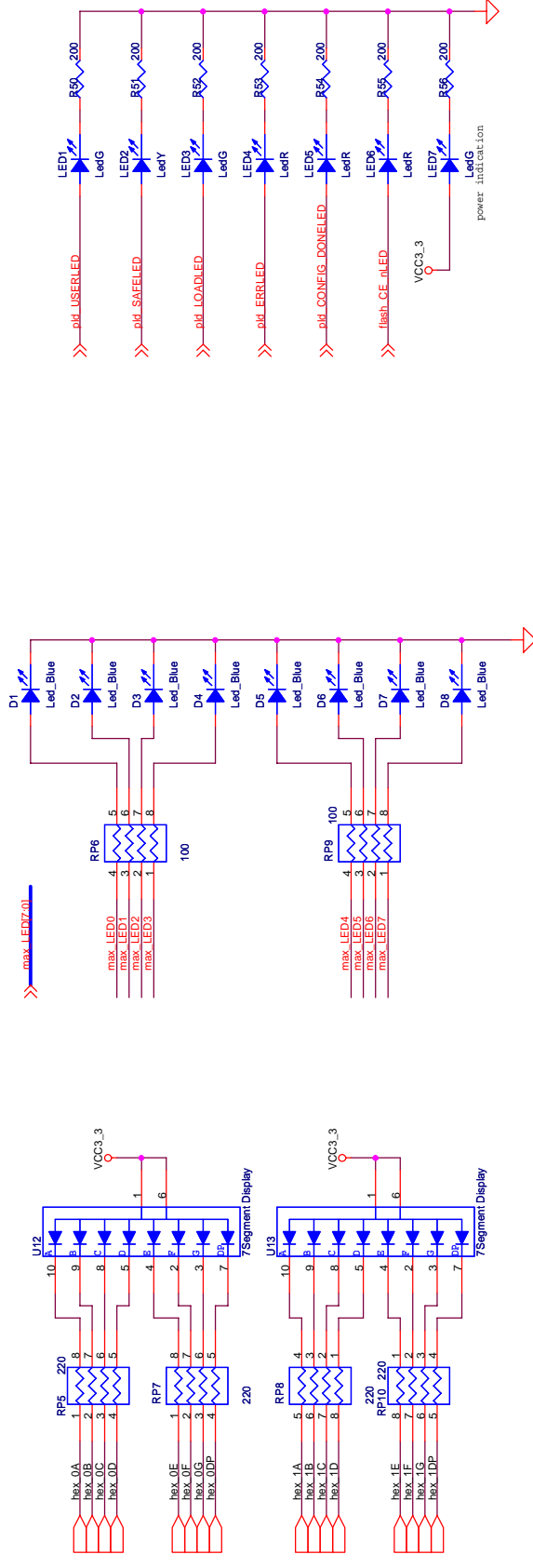
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 Altera FPGAs (Altera)
 Part Number
 Date: 01/11/2004

Label this bottom very clearly with a box around the bottom and text.

PLD BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.

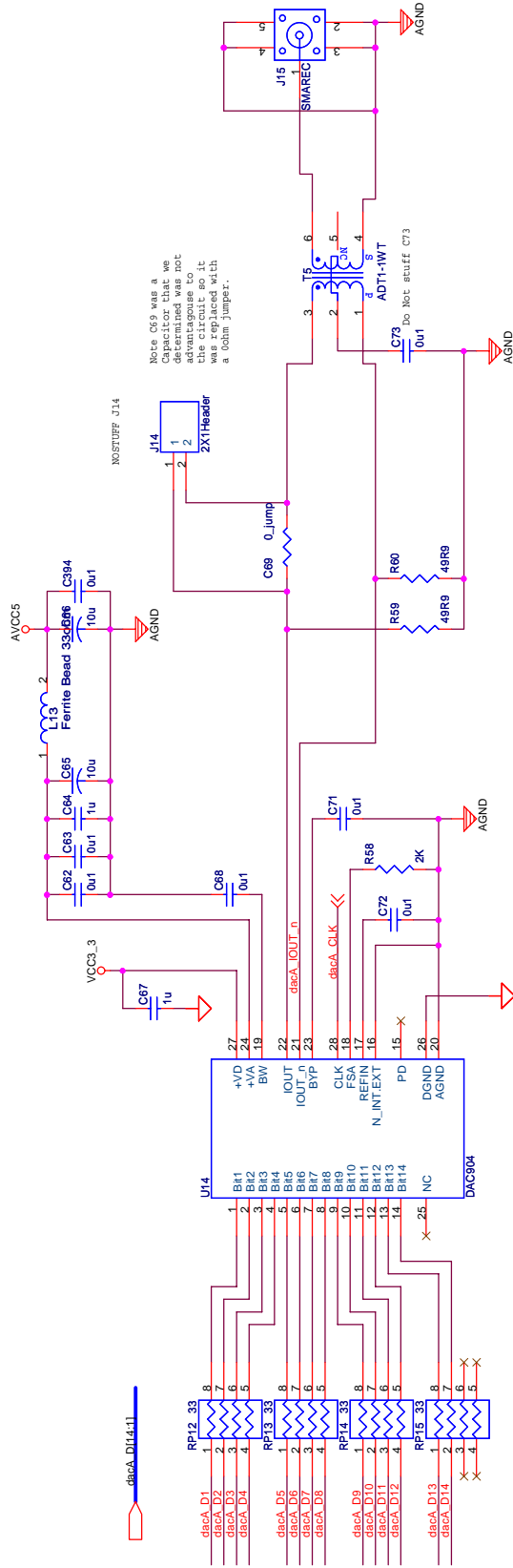
male header JTAG connections:
 1 TCK
 2 TMS
 3 TDI
 4 TDO
 5 NC
 6 NC
 7 NC
 8 NC
 9 TDI
 10 GND

Configuration PLD schematic showing logic elements, pins, and internal connections. It includes sections for logic elements (e.g., U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U51, U52, U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U68, U69, U70, U71, U72, U73, U74, U75, U76, U77, U78, U79, U80, U81, U82, U83, U84, U85, U86, U87, U88, U89, U90, U91, U92, U93, U94, U95, U96, U97, U98, U99, U100), pins (e.g., VCC3_3, GND, USER0, USER1, USER2, USER3, USER4, USER5, USER6, USER7, USER8, USER9, USER10, USER11, USER12, USER13, USER14, USER15, USER16, USER17, USER18, USER19, USER20, USER21, USER22, USER23, USER24, USER25, USER26, USER27, USER28, USER29, USER30, USER31, USER32, USER33, USER34, USER35, USER36, USER37, USER38, USER39, USER40, USER41, USER42, USER43, USER44, USER45, USER46, USER47, USER48, USER49, USER50, USER51, USER52, USER53, USER54, USER55, USER56, USER57, USER58, USER59, USER60, USER61, USER62, USER63, USER64, USER65, USER66, USER67, USER68, USER69, USER70, USER71, USER72, USER73, USER74, USER75, USER76, USER77, USER78, USER79, USER80, USER81, USER82, USER83, USER84, USER85, USER86, USER87, USER88, USER89, USER90, USER91, USER92, USER93, USER94, USER95, USER96, USER97, USER98, USER99, USER100), and internal connections (e.g., USER0, USER1, USER2, USER3, USER4, USER5, USER6, USER7, USER8, USER9, USER10, USER11, USER12, USER13, USER14, USER15, USER16, USER17, USER18, USER19, USER20, USER21, USER22, USER23, USER24, USER25, USER26, USER27, USER28, USER29, USER30, USER31, USER32, USER33, USER34, USER35, USER36, USER37, USER38, USER39, USER40, USER41, USER42, USER43, USER44, USER45, USER46, USER47, USER48, USER49, USER50, USER51, USER52, USER53, USER54, USER55, USER56, USER57, USER58, USER59, USER60, USER61, USER62, USER63, USER64, USER65, USER66, USER67, USER68, USER69, USER70, USER71, USER72, USER73, USER74, USER75, USER76, USER77, USER78, USER79, USER80, USER81, USER82, USER83, USER84, USER85, USER86, USER87, USER88, USER89, USER90, USER91, USER92, USER93, USER94, USER95, USER96, USER97, USER98, USER99, USER100).



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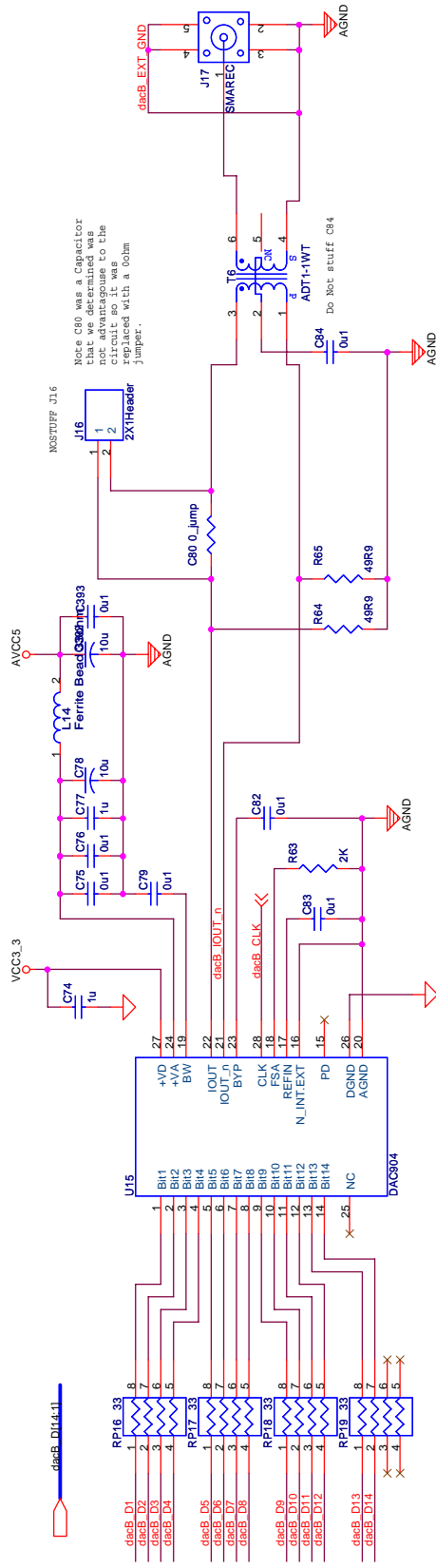
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Note: C90 was a capacitor that we determined was not advantageous to the circuit so it was replaced with a 0ohm jumper.

Do Not stuff C84

TP3 Should be labeled IOUT_n in silk screen

TP3 Test_Header

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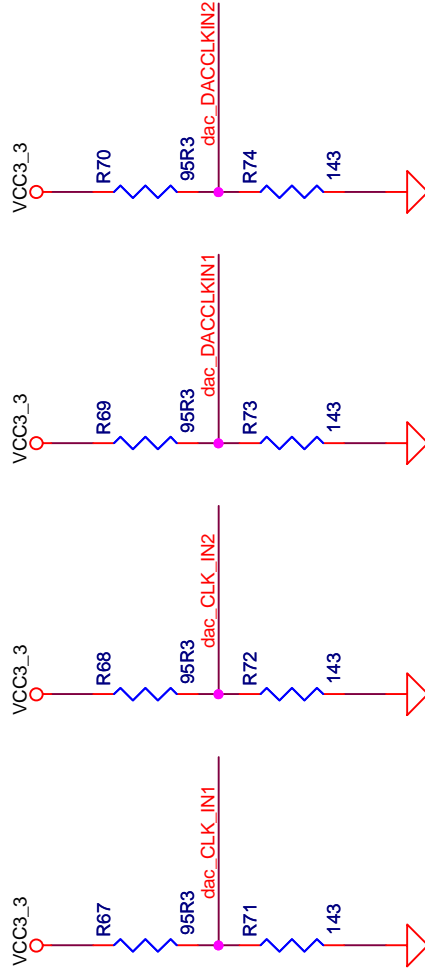
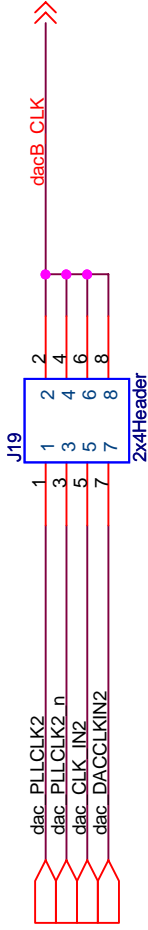
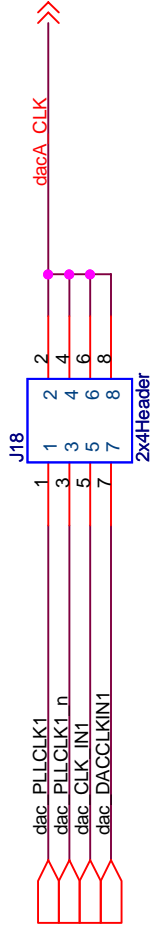
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DAC Clock Jumper

S3 Shunt Jumper



S4 Shunt Jumper



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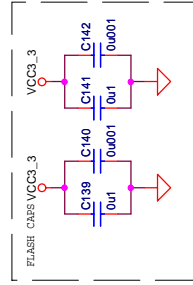
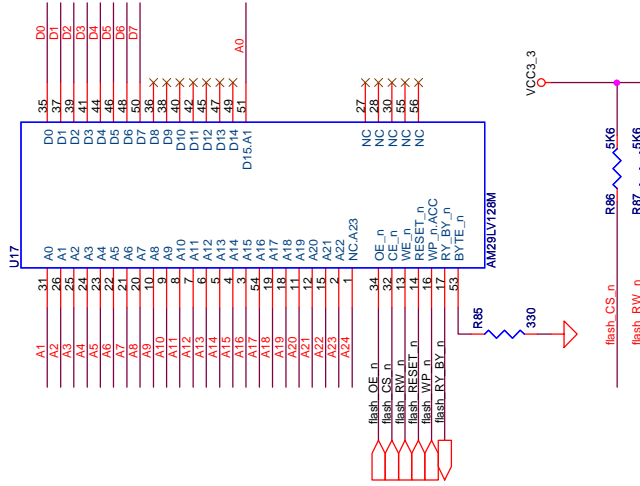
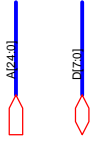
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Flash chip is 16M x 8 for 16Mbytes of flash

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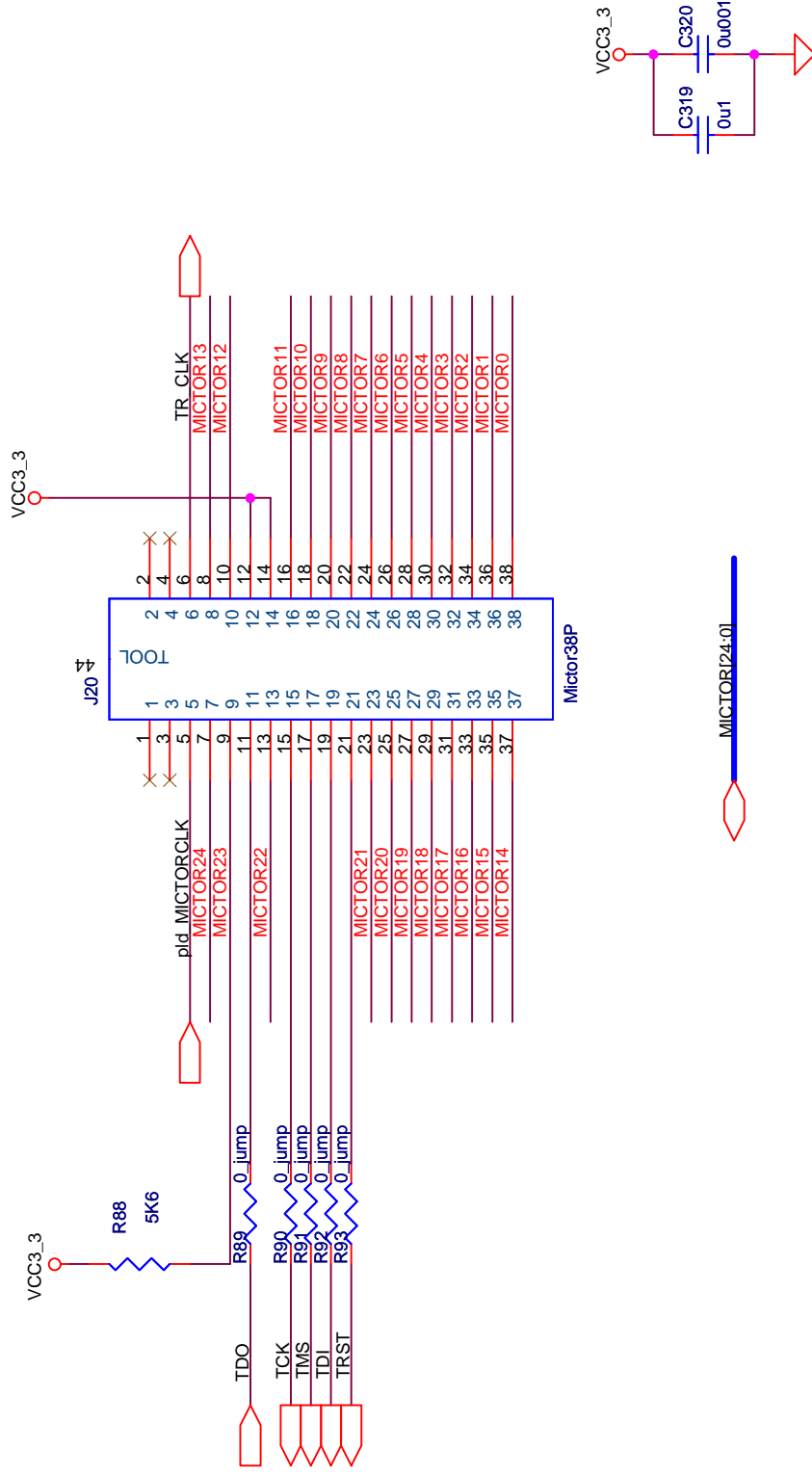
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Size: **Document Number**
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Mictor Connector



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Title

Stratix II DSP Board (Maine)

Size

A

Document Number

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02

Date:

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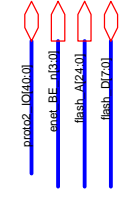
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40

flash_D0	AH30	IO.DIFFIO_RX10p	AE28	enel_CYCLE_n
flash_D1	AH29	IO.DIFFIO_RX11p	AE27	enel_W_R_n
flash_D2	AJ32	IO.DIFFIO_RX12p	AE26	enel_BE_i0
flash_D3	AJ31	IO.DIFFIO_RX20p	AE25	enel_BE_r1
flash_D4	AH31	IO.DIFFIO_RX21p	AE24	enel_BE_r2
flash_D5	AH30	IO.DIFFIO_RX22p	AB24	enel_BE_r3
flash_D6	AH32	IO.DIFFIO_RX30p	AB23	enel_DATAGS_n
flash_D7	AH31	IO.DIFFIO_RX31p	AC25	enel_INTR00
flash_D7	AH31	IO.DIFFIO_RX40p	AC25	enel_AEN
flash_A0	AF30	IO.DIFFIO_RX40p	AB26	enel_T0V_n
flash_A1	AF29	IO.DIFFIO_RX41p	AB25	enel_OCHRDY
flash_A2	AE30	IO.DIFFIO_RX50p	AA25	enel_ADS_n
flash_A3	AE29	IO.DIFFIO_RX51p	AA24	enel_IDEV_n
flash_A4	AG32	IO.DIFFIO_RX60p	AA23	enel_SRD_n
flash_A5	AG31	IO.DIFFIO_RX61p	AA22	enel_VIBUS_n
flash_A6	AF32	IO.DIFFIO_RX80p	AC27	prot02_I00
flash_A7	AF31	IO.DIFFIO_RX81p	AC26	prot02_I01
flash_A8	AE32	IO.DIFFIO_RX90p	AD27	prot02_I02
flash_A9	AE31	IO.DIFFIO_RX91p	AD26	prot02_I03
flash_A10	AD32	IO.DIFFIO_RX100p	Y28	prot02_I04
flash_A11	AD31	IO.DIFFIO_RX101p	Y27	prot02_I05
flash_A12	AB32	IO.DIFFIO_RX110p	Y26	prot02_I06
flash_A13	AB31	IO.DIFFIO_RX111p	Y25	prot02_I07
flash_A14	AC32	IO.DIFFIO_RX120p	AA27	prot02_I08
flash_A15	AC31	IO.DIFFIO_RX121p	AA26	prot02_I09
flash_A16	AE30	IO.DIFFIO_RX130p	Y27	prot02_I010
flash_A17	AE29	IO.DIFFIO_RX131p	Y26	prot02_I011
flash_A18	Y28	IO.DIFFIO_RX140p	W25	prot02_I012
flash_A19	Y27	IO.DIFFIO_RX141p	W24	prot02_I013
flash_A20	AA30	IO.DIFFIO_RX150p	W23	prot02_I014
flash_A21	AA29	IO.DIFFIO_RX151p	W22	prot02_I015
flash_A22	AB32	IO.DIFFIO_RX160p	W29	prot02_I016
flash_A23	AB31	IO.DIFFIO_RX161p	W28	prot02_I017
flash_A24	V31	IO.DIFFIO_RX170p	W27	prot02_I018
flash_WP_n	Y30	IO.DIFFIO_RX171p	W26	prot02_I019
flash_CS_n	AA32	IO.DIFFIO_RX180p	W25	prot02_I020
flash_C1_n	AA31	IO.DIFFIO_RX181p	W24	prot02_I021
flash_RW_n	W32	IO.DIFFIO_RX190p	W23	prot02_I022
flash_RY_BY_n	W31	IO.DIFFIO_RX191p	W22	prot02_I023
enel_LCLK	V31	IO.DIFFIO_RX18n	U28	
enel_LDVRTN_n	V30	IO.DIFFIO_RX16n	U27	
	U32	IO.CLK2pDIFFIO_RX_C1p	U23	prot02_I024
	U31	IO.CLK2pDIFFIO_RX_C1n	U22	prot02_I025
	U30	IO.CLK2pDIFFIO_RX_C1n	AD28	
	U29	CLK3n.INPUT	W30	VCC3_3
	AJ30	VREFB1N.VREFB1M1	AG28	
	AJ29	FPLL8CLKn.INPUT		
		VREFB1N2.VREFB1M2		



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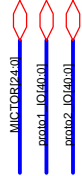
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PLD Bank 2

U18B

pin01_00	R31	I0.DIFFIO_RX21p	T23	MICTOR0
pin01_01	R30	I0.DIFFIO_RX21n	T22	MICTOR1
pin01_02	P32	I0.DIFFIO_RX22p	T28	MICTOR2
pin01_03	P31	I0.DIFFIO_RX22n	T27	MICTOR3
pin01_04	M32	I0.DIFFIO_RX23p	R29	MICTOR4
pin01_05	M31	I0.DIFFIO_RX23n	R28	MICTOR5
pin01_06	N31	I0.DIFFIO_RX24p	R24	MICTOR6
pin01_07	N30	I0.DIFFIO_RX24n	R23	MICTOR7
pin01_08	L32	I0.DIFFIO_RX25p	R23	MICTOR8
pin01_09	L31	I0.DIFFIO_RX25n	R22	MICTOR9
pin01_10	M30	I0.DIFFIO_RX26p	R27	MICTOR10
pin01_11	N29	I0.DIFFIO_RX26n	R26	MICTOR11
pin01_12	N28	I0.DIFFIO_RX28p	P25	MICTOR12
pin01_13	N28	I0.DIFFIO_RX27p	P24	MICTOR13
pin01_14	L30	I0.DIFFIO_RX27n	P27	MICTOR14
pin01_15	L29	I0.DIFFIO_RX28p	P26	MICTOR15
pin01_16	K32	I0.DIFFIO_RX28n	P28	MICTOR16
pin01_17	K31	I0.DIFFIO_RX29p	P28	MICTOR17
pin01_18	K30	I0.DIFFIO_RX29n	N27	MICTOR18
pin01_19	K29	I0.DIFFIO_RX30p	N26	MICTOR19
pin01_20	L32	I0.DIFFIO_RX30n	N25	MICTOR20
pin01_21	H31	I0.DIFFIO_RX31p	M27	MICTOR21
pin01_22	H30	I0.DIFFIO_RX31n	M26	MICTOR22
pin01_23	H31	I0.DIFFIO_RX32p	M27	MICTOR23
pin01_24	G32	I0.DIFFIO_RX32n	M26	MICTOR24
pin01_25	G31	I0.DIFFIO_RX33p	N23	MICTOR25
pin01_26	F32	I0.DIFFIO_RX33n	N22	MICTOR26
pin01_27	F31	I0.DIFFIO_RX34p	M24	TR_CLK_3
pin01_28	E32	I0.DIFFIO_RX34n	M24	R10_VCC1_D30
pin01_29	E31	I0.DIFFIO_RX35p	L26	pin01_CARDSEL_n
pin01_30	H30	I0.DIFFIO_RX35n	L25	pin02_D26
pin01_31	H29	I0.DIFFIO_RX36p	M23	pin02_D27
pin01_32	H29	I0.DIFFIO_RX36n	M22	pin02_D28
pin01_33	G30	I0.DIFFIO_RX37p	K27	pin02_D29
pin01_34	F30	I0.DIFFIO_RX37n	L24	pin02_D30
pin01_35	E30	I0.DIFFIO_RX38p	L23	pin02_D31
pin01_36	D31	I0.DIFFIO_RX38n	J27	pin02_D32
pin01_37	D30	I0.DIFFIO_RX39p	J27	pin02_D33
pin01_38	D29	I0.DIFFIO_RX39n	H28	pin02_D34
pin01_39	D31	I0.DIFFIO_RX40p	H27	pin02_D35
pin01_40	D30	I0.DIFFIO_RX40n	K25	pin02_D37
pin01_CLKOUT	T32	I0.CLK0p/DIFFIO_RX_C0p	K24	pin02_D38
pin02_CLKOUT	T31	I0.CLK0n/DIFFIO_RX_C0n	K24	pin02_D38
	D30	CLK0n.INPUT	F28	VCC3_3
	D29	CLK0p.INPUT	J28	VREFB20.VREFB20
		FFL/CLK0n.INPUT	P30	VREFB22.VREFB22
		FFL/CLK0p.INPUT		



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B P06-10217

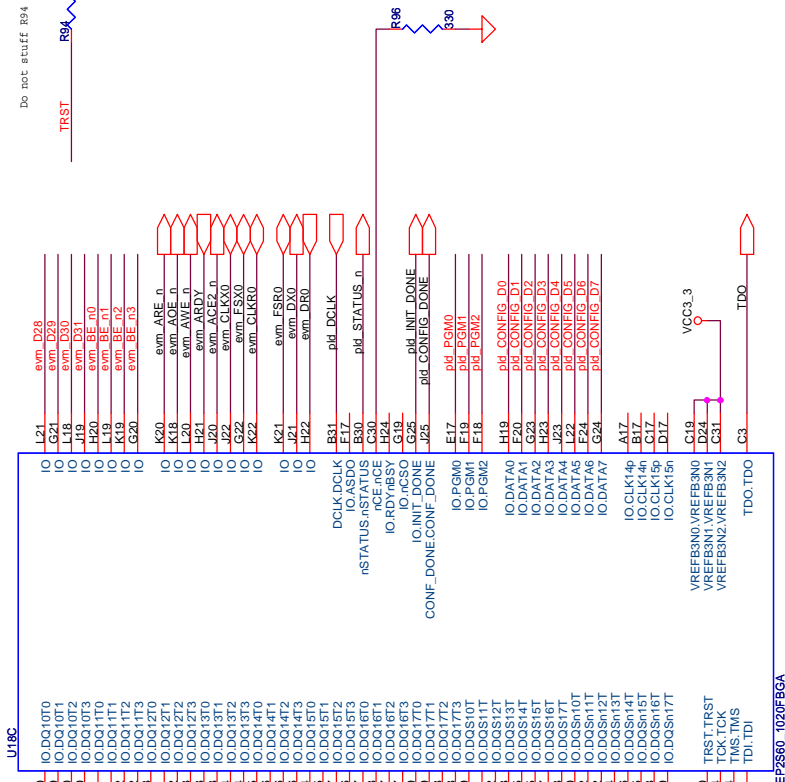
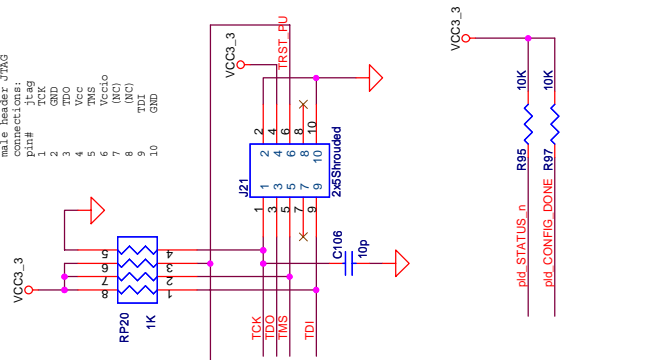
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Rev
02

PLD Bank 3

male header JTM3
connections:
1 TRST
2 TCK
3 GND
4 TDO
5 Vcclo
6 (NC)
7 TDI
8 (NC)
9 TDI
10 GND

Do not stuff R94

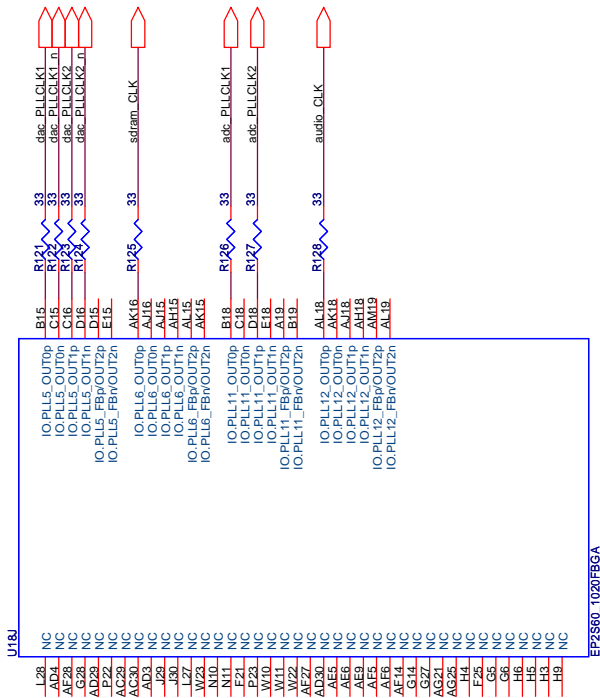


PLD Bank 4

IO.D0070	B4	IO.D0070	K13	DIR1
IO.D0071	D5	IO.D0071	H14	DD1
IO.D0072	E3	IO.D0072	K16	DR1
IO.D0073	A5	IO.D0073	L17	TXD1
IO.D0110	D8	IO.D0110	K15	CTS1
IO.D0112	C6	IO.D0112	L16	RXD1
IO.D0113	A6	IO.D0113	L15	RTS1
IO.D0270	B7	IO.D0270	K12	evm JACK
IO.D0271	E6	IO.D0271	H13	evm INUM0
IO.D0273	A7	IO.D0273	L12	evm CNT10
IO.D0370	C8	IO.D0370	H12	evm STAT0
IO.D0371	C8	IO.D0371	L11	evm DMAC0
IO.D0372	A8	IO.D0372	L11	evm CLKRESET
IO.D0373	A8	IO.D0373	H11	evm INT0
IO.D0470	D8	IO.D0470	L14	evm INT1
IO.D0471	E8	IO.D0471	J14	RT08
IO.D0472	F10	IO.D0472	J14	evm INT2
IO.D0473	F10	IO.D0473	L13	USER PB1
IO.D0570	A10	IO.D0570	L13	USER PB2
IO.D0571	D10	IO.D0571	J13	USER PB3
IO.D0572	D10	IO.D0572	J13	USER PB3
IO.D0573	D11	IO.D0573	J13	USER PB3
IO.D0670	E11	IO.D0670	A16	pd.CLKIN1_n
IO.D0671	G11	IO.D0671	E16	pd.DACCLKIN
IO.D0672	G12	IO.D0672	F16	pd.DACCLKIN
IO.D0673	G12	IO.D0673	F16	pd.DACCLKIN
IO.D0770	A12	IO.D0770	C2	VCC3_3
IO.D0771	A12	IO.D0771	D8	pd.MSEL0
IO.D0772	A12	IO.D0772	C14	pd.MSEL1
IO.D0773	A12	IO.D0773	F8	pd.MSEL2
IO.D0870	E13	IO.D0870	B2	pd.MSEL3
IO.D0871	F13	IO.D0871	F8	pd.MSEL0
IO.D0872	F13	IO.D0872	J10	pd.MSEL1
IO.D0873	F15	IO.D0873	J10	pd.MSEL2
IO.D0874	F15	IO.D0874	H10	pd.MSEL3
IO.D0970	D14	IO.D0970	C2	VCC3_3
IO.D0971	D13	IO.D0971	D8	pd.MSEL0
IO.D0972	D13	IO.D0972	C14	pd.MSEL1
IO.D0973	A14	IO.D0973	F8	pd.MSEL2
IO.D0974	A14	IO.D0974	F8	pd.MSEL3
IO.D0975	A14	IO.D0975	F8	pd.MSEL3
IO.D0976	A14	IO.D0976	F8	pd.MSEL3
IO.D0977	A14	IO.D0977	F8	pd.MSEL3
IO.D0978	A14	IO.D0978	F8	pd.MSEL3
IO.D0979	A14	IO.D0979	F8	pd.MSEL3
IO.D0980	A14	IO.D0980	F8	pd.MSEL3
IO.D0981	A14	IO.D0981	F8	pd.MSEL3
IO.D0982	A14	IO.D0982	F8	pd.MSEL3
IO.D0983	A14	IO.D0983	F8	pd.MSEL3
IO.D0984	A14	IO.D0984	F8	pd.MSEL3
IO.D0985	A14	IO.D0985	F8	pd.MSEL3
IO.D0986	A14	IO.D0986	F8	pd.MSEL3
IO.D0987	A14	IO.D0987	F8	pd.MSEL3
IO.D0988	A14	IO.D0988	F8	pd.MSEL3
IO.D0989	A14	IO.D0989	F8	pd.MSEL3
IO.D0990	A14	IO.D0990	F8	pd.MSEL3
IO.D0991	A14	IO.D0991	F8	pd.MSEL3
IO.D0992	A14	IO.D0992	F8	pd.MSEL3
IO.D0993	A14	IO.D0993	F8	pd.MSEL3
IO.D0994	A14	IO.D0994	F8	pd.MSEL3
IO.D0995	A14	IO.D0995	F8	pd.MSEL3
IO.D0996	A14	IO.D0996	F8	pd.MSEL3
IO.D0997	A14	IO.D0997	F8	pd.MSEL3
IO.D0998	A14	IO.D0998	F8	pd.MSEL3
IO.D0999	A14	IO.D0999	F8	pd.MSEL3
IO.D1000	A14	IO.D1000	F8	pd.MSEL3
IO.D1001	A14	IO.D1001	F8	pd.MSEL3
IO.D1002	A14	IO.D1002	F8	pd.MSEL3
IO.D1003	A14	IO.D1003	F8	pd.MSEL3
IO.D1004	A14	IO.D1004	F8	pd.MSEL3
IO.D1005	A14	IO.D1005	F8	pd.MSEL3
IO.D1006	A14	IO.D1006	F8	pd.MSEL3
IO.D1007	A14	IO.D1007	F8	pd.MSEL3
IO.D1008	A14	IO.D1008	F8	pd.MSEL3
IO.D1009	A14	IO.D1009	F8	pd.MSEL3
IO.D1010	A14	IO.D1010	F8	pd.MSEL3
IO.D1011	A14	IO.D1011	F8	pd.MSEL3
IO.D1012	A14	IO.D1012	F8	pd.MSEL3
IO.D1013	A14	IO.D1013	F8	pd.MSEL3
IO.D1014	A14	IO.D1014	F8	pd.MSEL3
IO.D1015	A14	IO.D1015	F8	pd.MSEL3
IO.D1016	A14	IO.D1016	F8	pd.MSEL3
IO.D1017	A14	IO.D1017	F8	pd.MSEL3
IO.D1018	A14	IO.D1018	F8	pd.MSEL3
IO.D1019	A14	IO.D1019	F8	pd.MSEL3
IO.D1020	A14	IO.D1020	F8	pd.MSEL3
IO.D1021	A14	IO.D1021	F8	pd.MSEL3
IO.D1022	A14	IO.D1022	F8	pd.MSEL3
IO.D1023	A14	IO.D1023	F8	pd.MSEL3
IO.D1024	A14	IO.D1024	F8	pd.MSEL3
IO.D1025	A14	IO.D1025	F8	pd.MSEL3
IO.D1026	A14	IO.D1026	F8	pd.MSEL3
IO.D1027	A14	IO.D1027	F8	pd.MSEL3
IO.D1028	A14	IO.D1028	F8	pd.MSEL3
IO.D1029	A14	IO.D1029	F8	pd.MSEL3
IO.D1030	A14	IO.D1030	F8	pd.MSEL3
IO.D1031	A14	IO.D1031	F8	pd.MSEL3
IO.D1032	A14	IO.D1032	F8	pd.MSEL3
IO.D1033	A14	IO.D1033	F8	pd.MSEL3
IO.D1034	A14	IO.D1034	F8	pd.MSEL3
IO.D1035	A14	IO.D1035	F8	pd.MSEL3
IO.D1036	A14	IO.D1036	F8	pd.MSEL3
IO.D1037	A14	IO.D1037	F8	pd.MSEL3
IO.D1038	A14	IO.D1038	F8	pd.MSEL3
IO.D1039	A14	IO.D1039	F8	pd.MSEL3
IO.D1040	A14	IO.D1040	F8	pd.MSEL3
IO.D1041	A14	IO.D1041	F8	pd.MSEL3
IO.D1042	A14	IO.D1042	F8	pd.MSEL3
IO.D1043	A14	IO.D1043	F8	pd.MSEL3
IO.D1044	A14	IO.D1044	F8	pd.MSEL3
IO.D1045	A14	IO.D1045	F8	pd.MSEL3
IO.D1046	A14	IO.D1046	F8	pd.MSEL3
IO.D1047	A14	IO.D1047	F8	pd.MSEL3
IO.D1048	A14	IO.D1048	F8	pd.MSEL3
IO.D1049	A14	IO.D1049	F8	pd.MSEL3
IO.D1050	A14	IO.D1050	F8	pd.MSEL3
IO.D1051	A14	IO.D1051	F8	pd.MSEL3
IO.D1052	A14	IO.D1052	F8	pd.MSEL3
IO.D1053	A14	IO.D1053	F8	pd.MSEL3
IO.D1054	A14	IO.D1054	F8	pd.MSEL3
IO.D1055	A14	IO.D1055	F8	pd.MSEL3
IO.D1056	A14	IO.D1056	F8	pd.MSEL3
IO.D1057	A14	IO.D1057	F8	pd.MSEL3
IO.D1058	A14	IO.D1058	F8	pd.MSEL3
IO.D1059	A14	IO.D1059	F8	pd.MSEL3
IO.D1060	A14	IO.D1060	F8	pd.MSEL3
IO.D1061	A14	IO.D1061	F8	pd.MSEL3
IO.D1062	A14	IO.D1062	F8	pd.MSEL3
IO.D1063	A14	IO.D1063	F8	pd.MSEL3
IO.D1064	A14	IO.D1064	F8	pd.MSEL3
IO.D1065	A14	IO.D1065	F8	pd.MSEL3
IO.D1066	A14	IO.D1066	F8	pd.MSEL3
IO.D1067	A14	IO.D1067	F8	pd.MSEL3
IO.D1068	A14	IO.D1068	F8	pd.MSEL3
IO.D1069	A14	IO.D1069	F8	pd.MSEL3
IO.D1070	A14	IO.D1070	F8	pd.MSEL3
IO.D1071	A14	IO.D1071	F8	pd.MSEL3
IO.D1072	A14	IO.D1072	F8	pd.MSEL3
IO.D1073	A14	IO.D1073	F8	pd.MSEL3
IO.D1074	A14	IO.D1074	F8	pd.MSEL3
IO.D1075	A14	IO.D1075	F8	pd.MSEL3
IO.D1076	A14	IO.D1076	F8	pd.MSEL3
IO.D1077	A14	IO.D1077	F8	pd.MSEL3
IO.D1078	A14	IO.D1078	F8	pd.MSEL3
IO.D1079	A14	IO.D1079	F8	pd.MSEL3
IO.D1080	A14	IO.D1080	F8	pd.MSEL3
IO.D1081	A14	IO.D1081	F8	pd.MSEL3
IO.D1082	A14	IO.D1082	F8	pd.MSEL3
IO.D1083	A14	IO.D1083	F8	pd.MSEL3
IO.D1084	A14	IO.D1084	F8	pd.MSEL3
IO.D1085	A14	IO.D1085	F8	pd.MSEL3
IO.D1086	A14	IO.D1086	F8	pd.MSEL3
IO.D1087	A14	IO.D1087	F8	pd.MSEL3
IO.D1088	A14	IO.D1088	F8	pd.MSEL3
IO.D1089	A14	IO.D1089	F8	pd.MSEL3
IO.D1090	A14	IO.D1090	F8	pd.MSEL3
IO.D1091	A14	IO.D1091	F8	pd.MSEL3
IO.D1092	A14	IO.D1092	F8	pd.MSEL3
IO.D1093	A14	IO.D1093	F8	pd.MSEL3
IO.D1094	A14	IO.D1094	F8	pd.MSEL3
IO.D1095	A14	IO.D1095	F8	pd.MSEL3
IO.D1096	A14	IO.D1096	F8	pd.MSEL3
IO.D1097	A14	IO.D1097	F8	pd.MSEL3
IO.D1098	A14	IO.D1098	F8	pd.MSEL3
IO.D1099	A14	IO.D1099	F8	pd.MSEL3
IO.D1100	A14	IO.D1100	F8	pd.MSEL3
IO.D1101	A14	IO.D1101	F8	pd.MSEL3
IO.D1102	A14	IO.D1102	F8	pd.MSEL3
IO.D1103	A14	IO.D1103	F8	pd.MSEL3
IO.D1104	A14	IO.D1104	F8	pd.MSEL3
IO.D1105	A14	IO.D1105	F8	pd.MSEL3
IO.D1106	A14	IO.D1106	F8	pd.MSEL3
IO.D1107	A14	IO.D1107	F8	pd.MSEL3
IO.D1108	A14	IO.D1108	F8	pd.MSEL3
IO.D1109	A14	IO.D1109	F8	pd.MSEL3
IO.D1110	A14	IO.D1110	F8	pd.MSEL3
IO.D1111	A14	IO.D1111	F8	pd.MSEL3
IO.D1112	A14	IO.D1112	F8	pd.MSEL3
IO.D1113	A14	IO.D1113	F8	pd.MSEL3
IO.D1114	A14	IO.D1114	F8	pd.MSEL3
IO.D1115	A14	IO.D1115	F8	pd.MSEL3
IO.D1116	A14	IO.D1116	F8	pd.MSEL3
IO.D1117	A14	IO.D1117	F8	pd.MSEL3
IO.D1118	A14	IO.D1118	F8	pd.MSEL3
IO.D1119	A14	IO.D1119	F8	pd.MSEL3
IO.D1120	A14	IO.D1120	F8	pd.MSEL3
IO.D1121	A14	IO.D1121	F8	pd.MSEL3
IO.D1122	A14	IO.D1122	F8	pd.MSEL3
IO.D1123	A14	IO.D1123	F8	pd.MSEL3
IO.D1124	A14	IO.D1124	F8	pd.MSEL3
IO.D1125	A14	IO.D1125	F8	pd.MSEL3
IO.D1126	A14	IO.D1126	F8	pd.MSEL3
IO.D1127	A14	IO.D1127	F8	pd.MSEL3
IO.D1128	A14	IO.D1128	F8	pd.MSEL3
IO.D1129	A14	IO.D1129	F8	pd.MSEL3
IO.D1130	A14	IO.D1130	F8	pd.MSEL3
IO.D1131	A14	IO.D1131	F8	pd.MSEL3
IO.D1132	A14	IO.D1132	F8	pd.MSEL3
IO.D1133	A14	IO.D1133	F8	pd.MSEL3
IO.D1134	A14	IO.D1134	F8	pd.MSEL3
IO.D1135	A14	IO.D1135	F8	pd.MSEL3
IO.D1136	A14	IO.D1136	F8	pd.MSEL3
IO.D1137	A14	IO.D1137	F8	pd.MSEL3
IO.D1138	A14	IO.D1138	F8	pd.MSEL3
IO.D1139	A14	IO.D1139	F8	pd.MSEL3
IO.D1140	A14	IO.D1140	F8	pd.MSEL3
IO.D1141	A14	IO.D1141	F8	pd.MSEL3
IO.D1142	A14	IO.D1142	F8	pd.MSEL3
IO.D1143	A14	IO.D1143	F8	pd.MSEL3
IO.D1144	A14	IO.D1144	F8	pd.MSEL3
IO.D1145	A14	IO.D1145	F8	pd.MSEL3
IO.D1146	A14	IO.D1146	F8	pd.MSEL3
IO.D1147	A14	IO.D1147	F8	pd.MSEL3
IO.D1148	A14	IO.D1148	F8	pd.MSEL3
IO.D1149	A14	IO.D1149	F8	pd.MSEL3
IO.D1150	A14	IO.D1150	F8	pd.MSEL3
IO.D1151	A14	IO.D1151	F8	pd.MSEL3
IO.D1152	A14	IO.D1152	F8	pd.MSEL3
IO.D1153	A14	IO.D1153	F8	pd.MSEL3
IO.D1154	A14	IO.D1154	F8	

PLD Bank 5

Pin	Signal	IO Type	IO Pin
ad4A_D0	D0	IO.DIFFIO_RX43p	J6
ad4A_D1	D1	IO.DIFFIO_RX43n	J7
ad4A_D2	D2	IO.DIFFIO_RX44p	J8
ad4A_D3	D3	IO.DIFFIO_RX44n	J9
ad4A_D4	D4	IO.DIFFIO_RX45p	K3
ad4A_D5	D5	IO.DIFFIO_RX45n	K4
ad4A_D6	D6	IO.DIFFIO_RX46p	L10
ad4A_D7	D7	IO.DIFFIO_RX46n	L11
ad4A_D8	D8	IO.DIFFIO_RX47p	L7
ad4A_D9	D9	IO.DIFFIO_RX47n	L8
ad4A_D10	D10	IO.DIFFIO_RX48p	K8
ad4A_D11	D11	IO.DIFFIO_RX48n	L5
ad4B_D1	D1	IO.DIFFIO_RX49p	L6
ad4B_D2	D2	IO.DIFFIO_RX49n	M10
ad4B_D3	D3	IO.DIFFIO_RX50p	M11
ad4B_D4	D4	IO.DIFFIO_RX50n	M8
ad4B_D5	D5	IO.DIFFIO_RX51p	M8
ad4B_D6	D6	IO.DIFFIO_RX51n	M7
ad4B_D7	D7	IO.DIFFIO_RX52p	N6
ad4B_D8	D8	IO.DIFFIO_RX52n	N7
ad4B_D9	D9	IO.DIFFIO_RX53p	N8
ad4B_D10	D10	IO.DIFFIO_RX53n	N9
ad4B_D11	D11	IO.DIFFIO_RX54p	E8
ad4B_D12	D12	IO.DIFFIO_RX54n	E9
ad4B_D13	D13	IO.DIFFIO_RX55p	E7
ad4B_D14	D14	IO.DIFFIO_RX55n	E4
ad4B_D15	D15	IO.DIFFIO_RX56p	E5
ad4B_D16	D16	IO.DIFFIO_RX56n	P10
ad4B_D17	D17	IO.DIFFIO_RX57p	P11
ad4B_D18	D18	IO.DIFFIO_RX57n	P11
ad4B_D19	D19	IO.DIFFIO_RX58p	S6
ad4B_D20	D20	IO.DIFFIO_RX58n	R7
ad4B_D21	D21	IO.DIFFIO_RX59p	R4
ad4B_D22	D22	IO.DIFFIO_RX59n	R3
ad4B_D23	D23	IO.DIFFIO_RX60p	R10
ad4B_D24	D24	IO.DIFFIO_RX60n	T1
ad4B_D25	D25	IO.DIFFIO_RX61p	T6
ad4B_D26	D26	IO.DIFFIO_RX61n	T5
ad4B_D27	D27	IO.DIFFIO_RX62p	T10
ad4B_D28	D28	IO.DIFFIO_RX62n	T11
ad4B_D29	D29	IO.CLK10p/DIFFIO_RX_C3p	F3
ad4B_D30	D30	IO.CLK10n/DIFFIO_RX_C3n	F5
ad4B_D31	D31	CLK11p.INPUT	F5
ad4B_D32	D32	CLK11n.INPUT	F5
ad4B_D33	D33	FPLL10CLKn.INPUT	F5
ad4B_D34	D34	FPLL10CLKp.INPUT	F5
ad4B_D35	D35	VREFB5N0.VREFB5N0	F5
ad4B_D36	D36	VREFB5N1.VREFB5N1	F5
ad4B_D37	D37	VREFB5N2.VREFB5N2	F5
ad4B_D38	D38	VREFB5N3.VREFB5N3	F5
ad4B_D39	D39	VREFB5N4.VREFB5N4	F5
ad4B_D40	D40	VREFB5N5.VREFB5N5	F5
ad4B_D41	D41	VREFB5N6.VREFB5N6	F5
ad4B_D42	D42	VREFB5N7.VREFB5N7	F5
ad4B_D43	D43	VREFB5N8.VREFB5N8	F5
ad4B_D44	D44	VREFB5N9.VREFB5N9	F5
ad4B_D45	D45	VREFB5N10.VREFB5N10	F5
ad4B_D46	D46	VREFB5N11.VREFB5N11	F5
ad4B_D47	D47	VREFB5N12.VREFB5N12	F5
ad4B_D48	D48	VREFB5N13.VREFB5N13	F5
ad4B_D49	D49	VREFB5N14.VREFB5N14	F5
ad4B_D50	D50	VREFB5N15.VREFB5N15	F5
ad4B_D51	D51	VREFB5N16.VREFB5N16	F5
ad4B_D52	D52	VREFB5N17.VREFB5N17	F5
ad4B_D53	D53	VREFB5N18.VREFB5N18	F5
ad4B_D54	D54	VREFB5N19.VREFB5N19	F5
ad4B_D55	D55	VREFB5N20.VREFB5N20	F5
ad4B_D56	D56	VREFB5N21.VREFB5N21	F5
ad4B_D57	D57	VREFB5N22.VREFB5N22	F5
ad4B_D58	D58	VREFB5N23.VREFB5N23	F5
ad4B_D59	D59	VREFB5N24.VREFB5N24	F5
ad4B_D60	D60	VREFB5N25.VREFB5N25	F5
ad4B_D61	D61	VREFB5N26.VREFB5N26	F5
ad4B_D62	D62	VREFB5N27.VREFB5N27	F5
ad4B_D63	D63	VREFB5N28.VREFB5N28	F5
ad4B_D64	D64	VREFB5N29.VREFB5N29	F5
ad4B_D65	D65	VREFB5N30.VREFB5N30	F5
ad4B_D66	D66	VREFB5N31.VREFB5N31	F5
ad4B_D67	D67	VREFB5N32.VREFB5N32	F5
ad4B_D68	D68	VREFB5N33.VREFB5N33	F5
ad4B_D69	D69	VREFB5N34.VREFB5N34	F5
ad4B_D70	D70	VREFB5N35.VREFB5N35	F5
ad4B_D71	D71	VREFB5N36.VREFB5N36	F5
ad4B_D72	D72	VREFB5N37.VREFB5N37	F5
ad4B_D73	D73	VREFB5N38.VREFB5N38	F5
ad4B_D74	D74	VREFB5N39.VREFB5N39	F5
ad4B_D75	D75	VREFB5N40.VREFB5N40	F5
ad4B_D76	D76	VREFB5N41.VREFB5N41	F5
ad4B_D77	D77	VREFB5N42.VREFB5N42	F5
ad4B_D78	D78	VREFB5N43.VREFB5N43	F5
ad4B_D79	D79	VREFB5N44.VREFB5N44	F5
ad4B_D80	D80	VREFB5N45.VREFB5N45	F5
ad4B_D81	D81	VREFB5N46.VREFB5N46	F5
ad4B_D82	D82	VREFB5N47.VREFB5N47	F5
ad4B_D83	D83	VREFB5N48.VREFB5N48	F5
ad4B_D84	D84	VREFB5N49.VREFB5N49	F5
ad4B_D85	D85	VREFB5N50.VREFB5N50	F5
ad4B_D86	D86	VREFB5N51.VREFB5N51	F5
ad4B_D87	D87	VREFB5N52.VREFB5N52	F5
ad4B_D88	D88	VREFB5N53.VREFB5N53	F5
ad4B_D89	D89	VREFB5N54.VREFB5N54	F5
ad4B_D90	D90	VREFB5N55.VREFB5N55	F5
ad4B_D91	D91	VREFB5N56.VREFB5N56	F5
ad4B_D92	D92	VREFB5N57.VREFB5N57	F5
ad4B_D93	D93	VREFB5N58.VREFB5N58	F5
ad4B_D94	D94	VREFB5N59.VREFB5N59	F5
ad4B_D95	D95	VREFB5N60.VREFB5N60	F5
ad4B_D96	D96	VREFB5N61.VREFB5N61	F5
ad4B_D97	D97	VREFB5N62.VREFB5N62	F5
ad4B_D98	D98	VREFB5N63.VREFB5N63	F5
ad4B_D99	D99	VREFB5N64.VREFB5N64	F5
ad4B_D100	D100	VREFB5N65.VREFB5N65	F5
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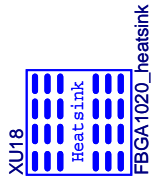
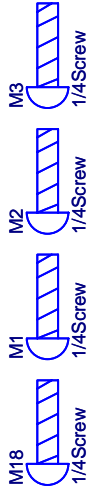
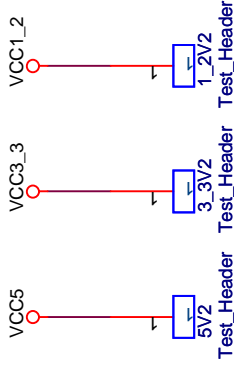
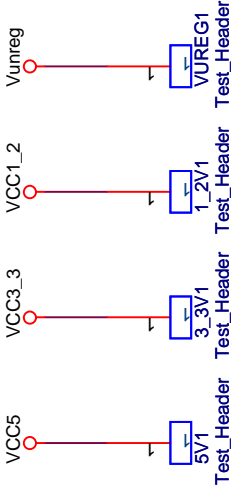
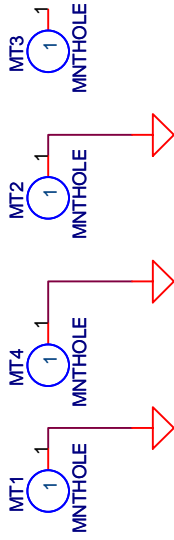
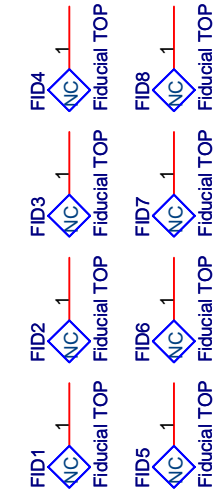
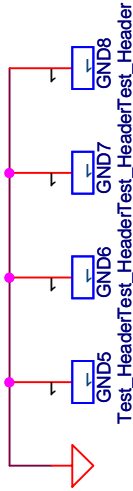
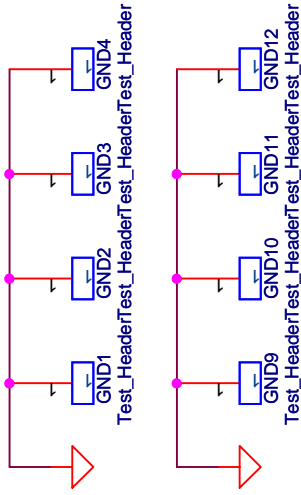
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Reset and Test headers



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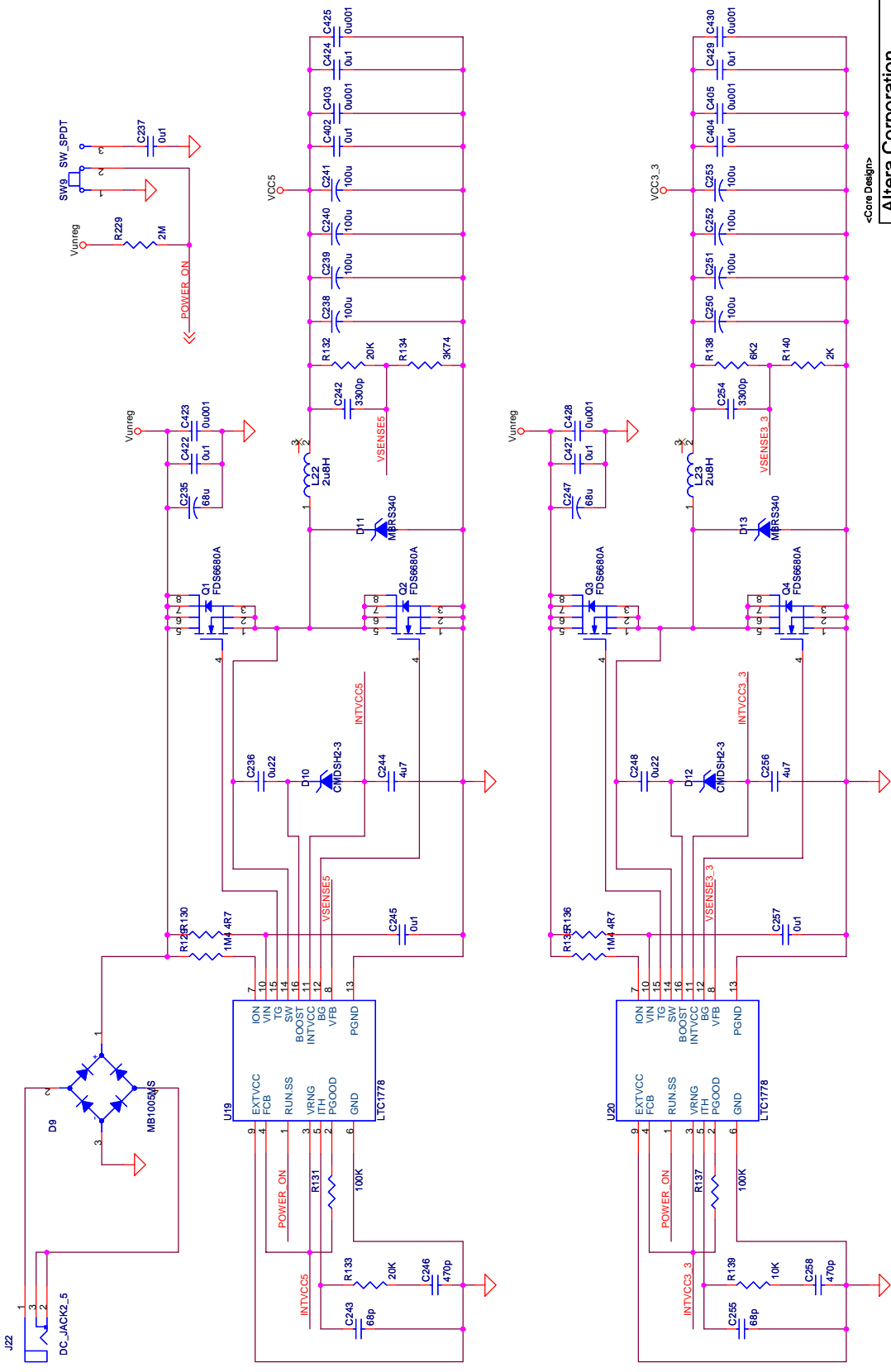
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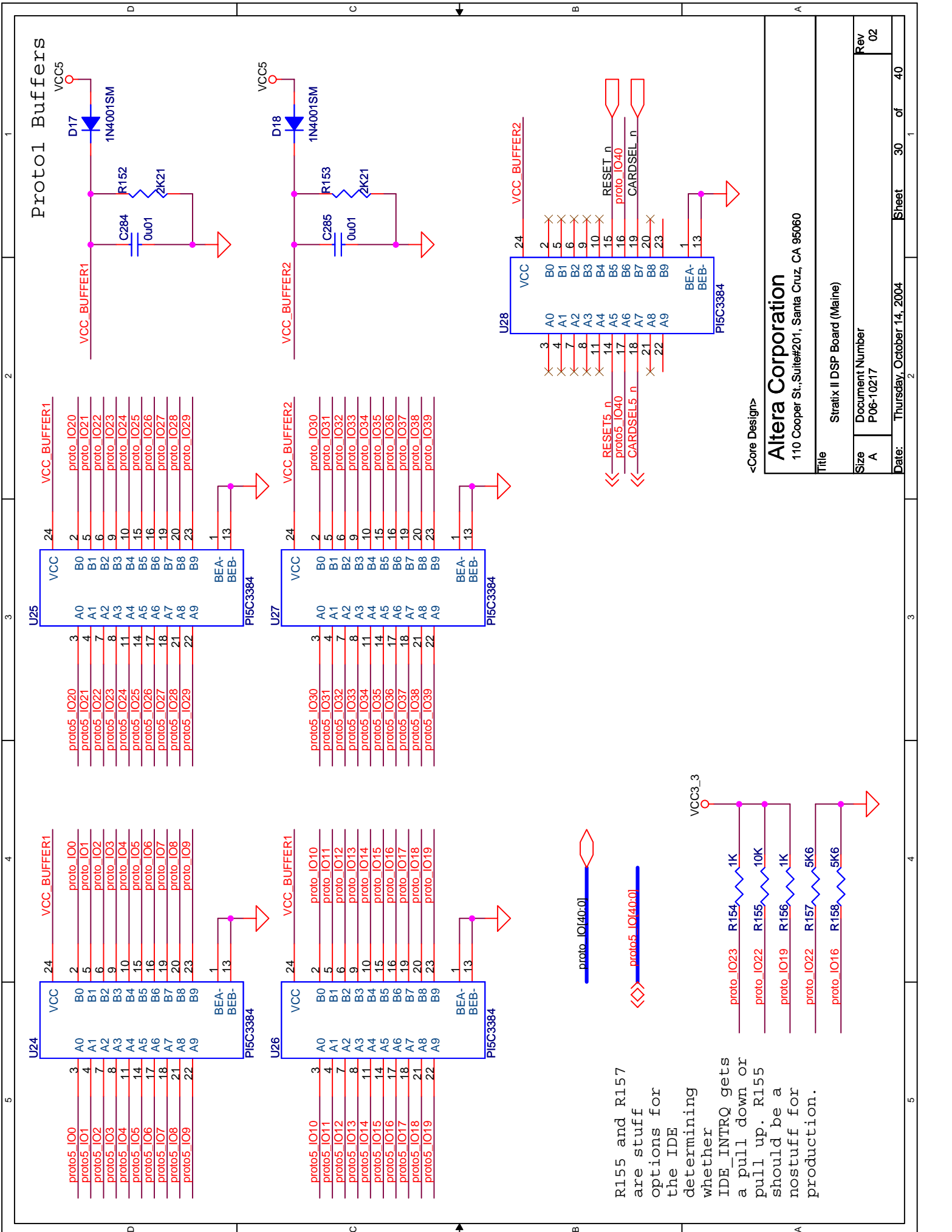
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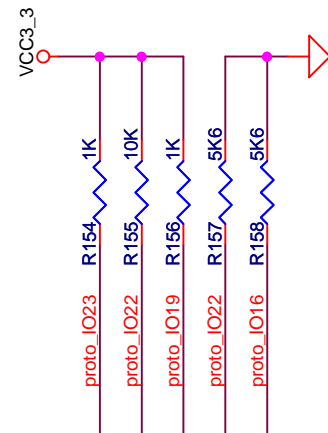
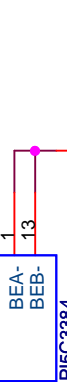


Proto1 Buffers

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5	proto5_IO2	5	
6	proto5_IO3	B0	
7	proto5_IO4	B1	
8	proto5_IO5	B2	
9	proto5_IO6	B3	
10	proto5_IO7	B4	
11	proto5_IO8	B5	
12	proto5_IO9	B6	
13		B7	
14		B8	
15		B9	
16		BEA-	
17		BEB-	
18		1	
19		13	
20			
21			
22			



3	proto5_IO10	24	VCC_BUFFER1
4	proto5_IO11	2	
5	proto5_IO12	5	
6	proto5_IO13	B0	
7	proto5_IO14	B1	
8	proto5_IO15	B2	
9	proto5_IO16	B3	
10	proto5_IO17	B4	
11	proto5_IO18	B5	
12	proto5_IO19	B6	
13		B7	
14		B8	
15		B9	
16		BEA-	
17		BEB-	
18		1	
19		13	
20			
21			
22			



R155 and R157 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R155 should be a nostuff for production.

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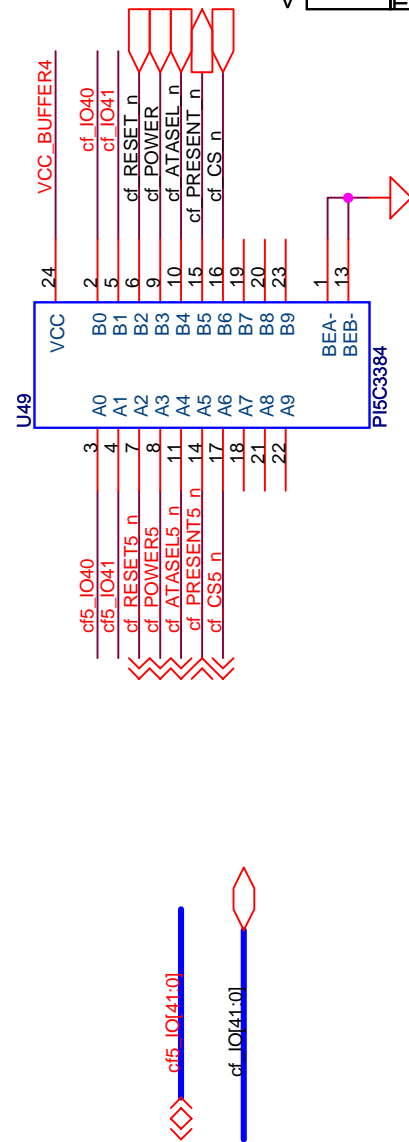
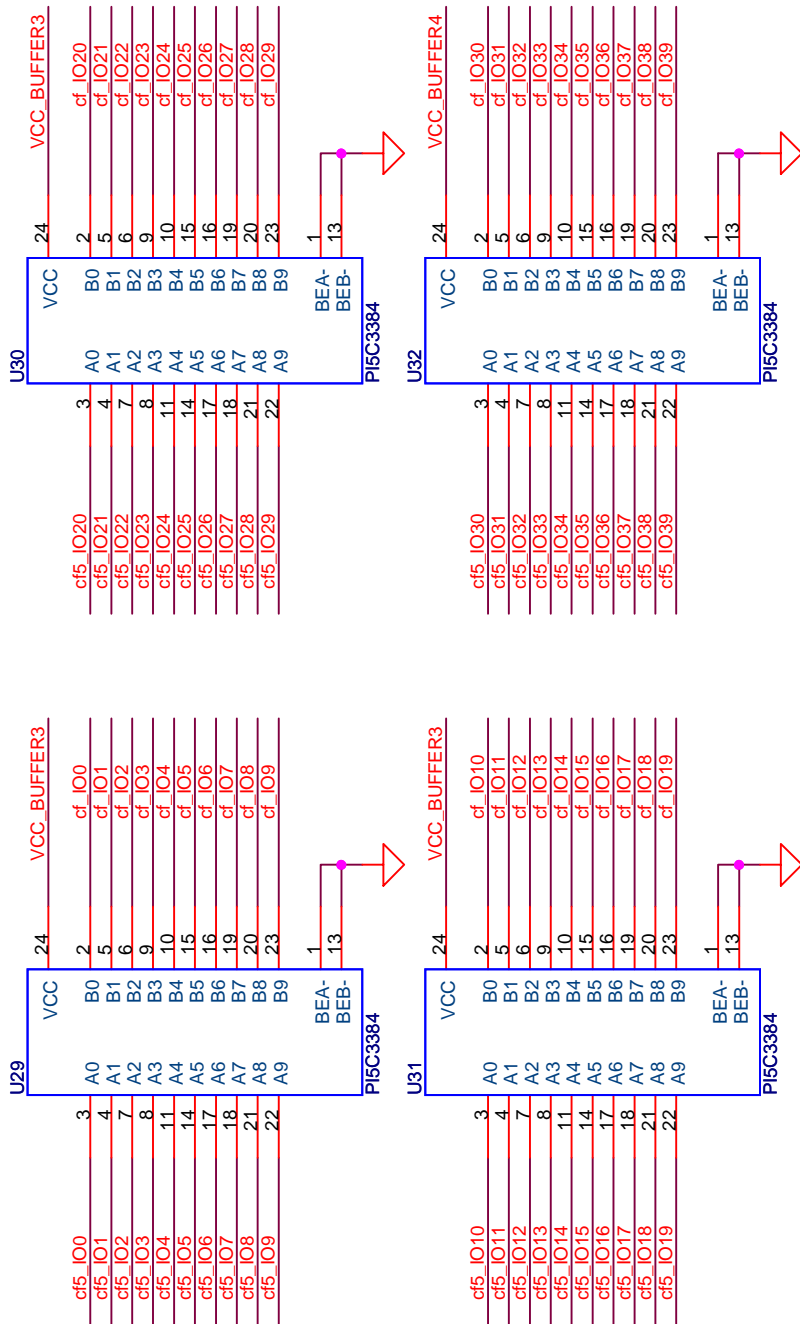
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Proto1 Buffers



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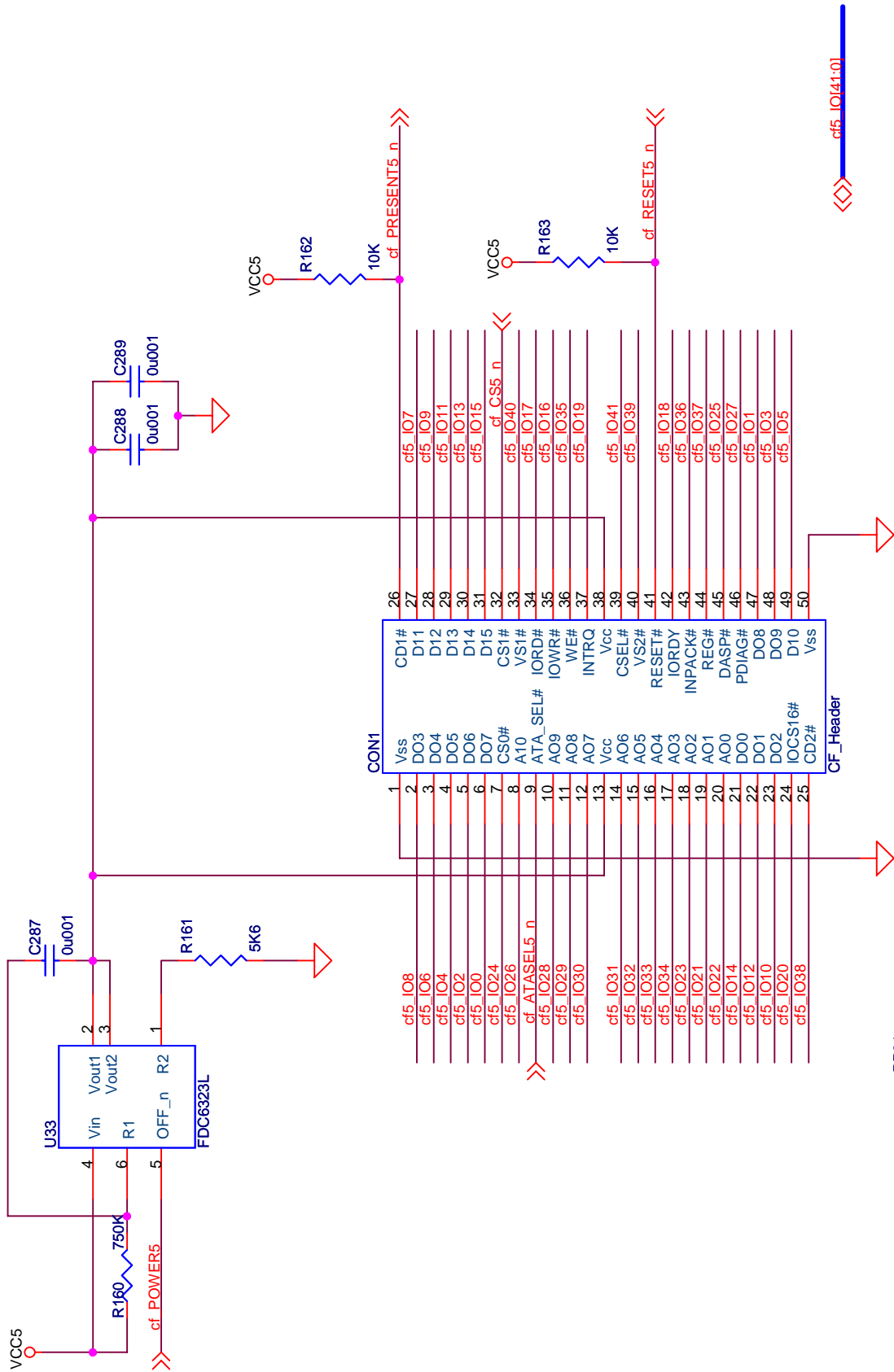
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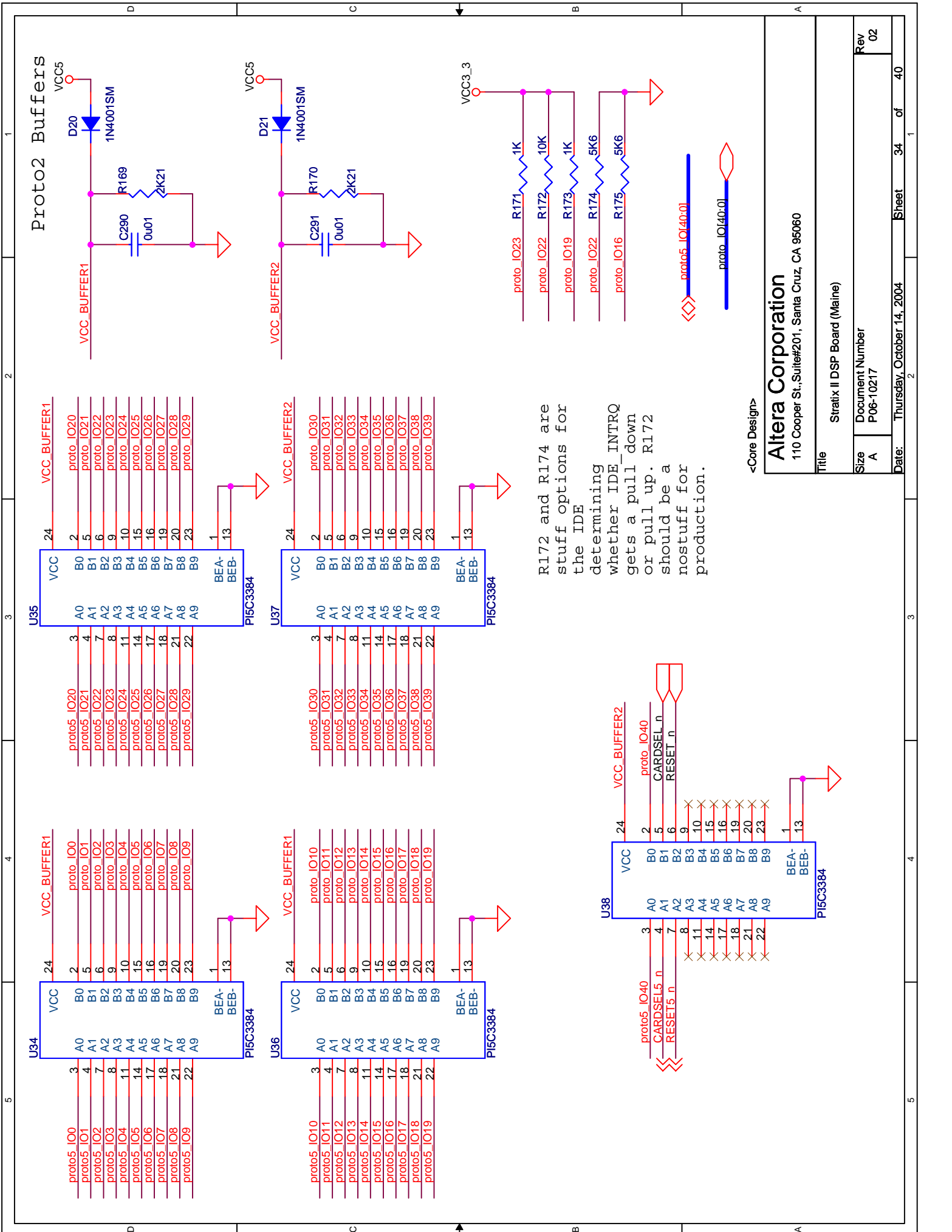
Compact Flash Socket



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Proto2 Buffers

R172 and R174 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R172 should be a nostuff for production.

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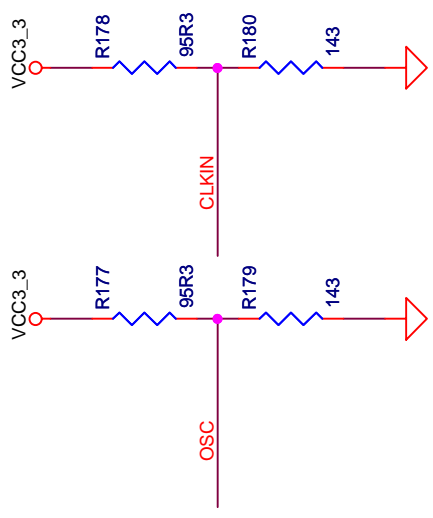
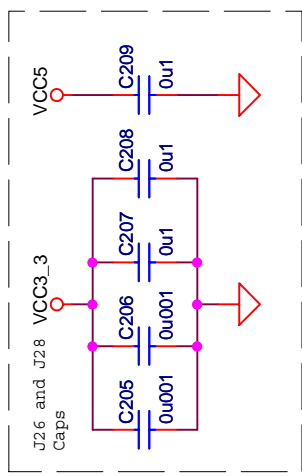
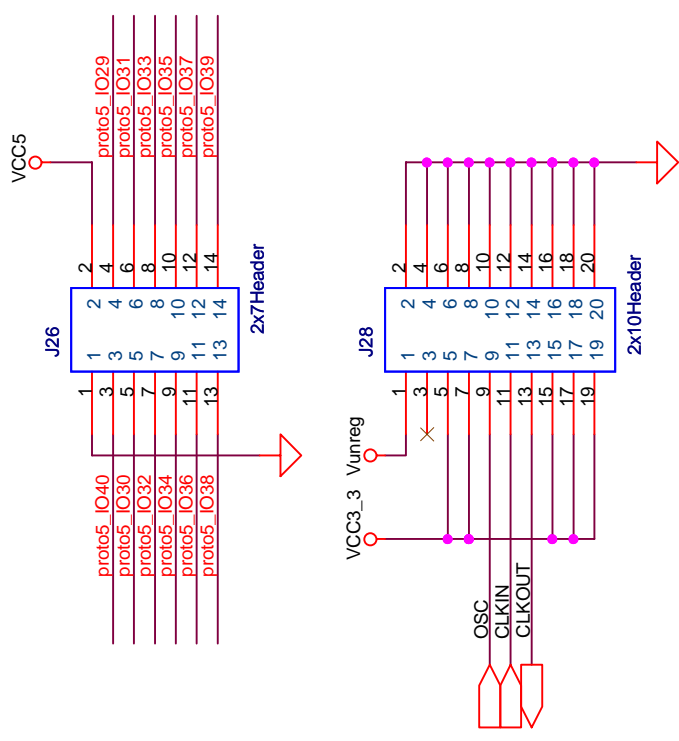
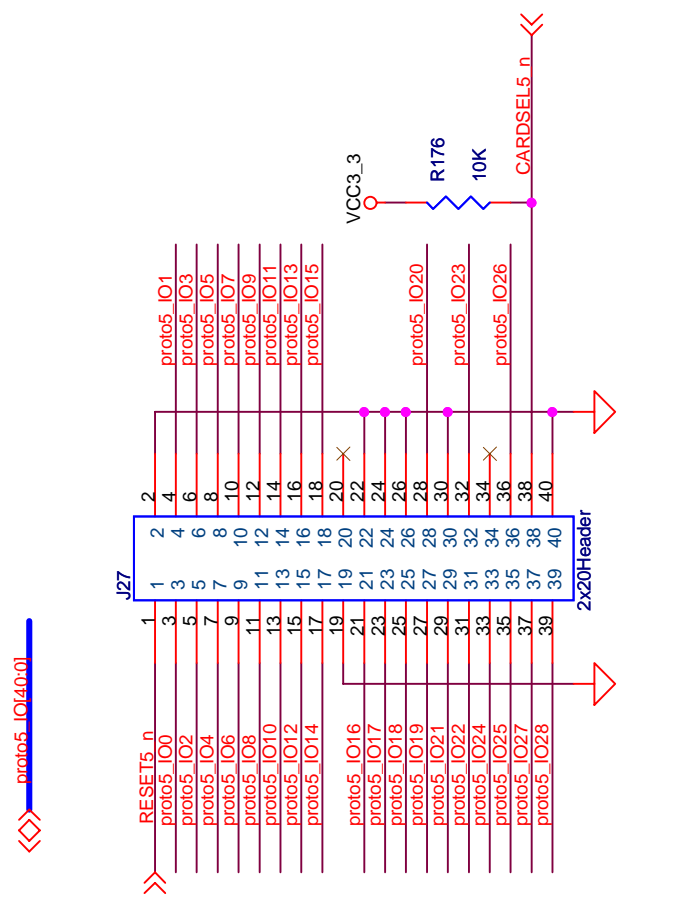
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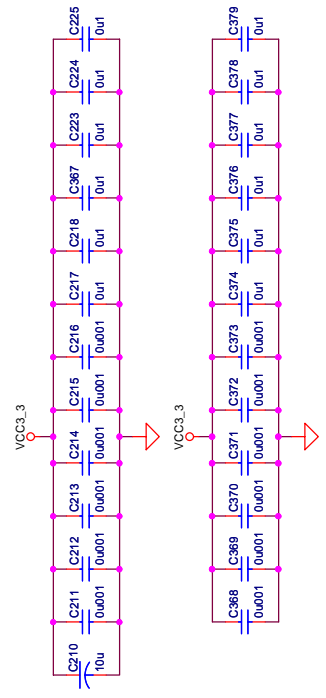
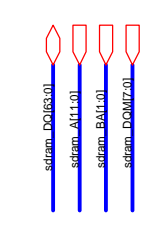
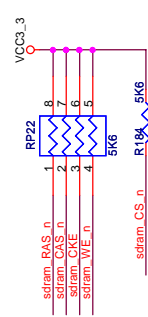
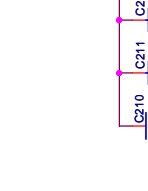
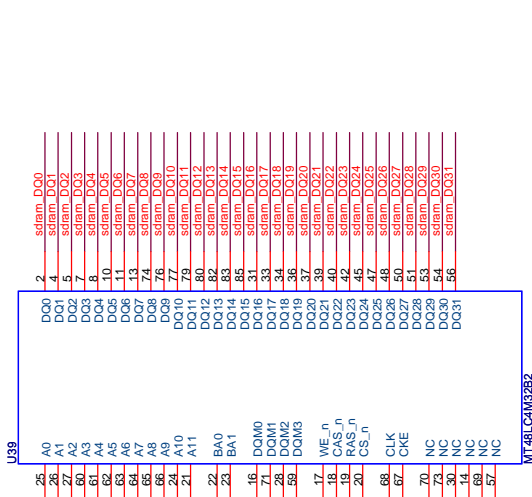
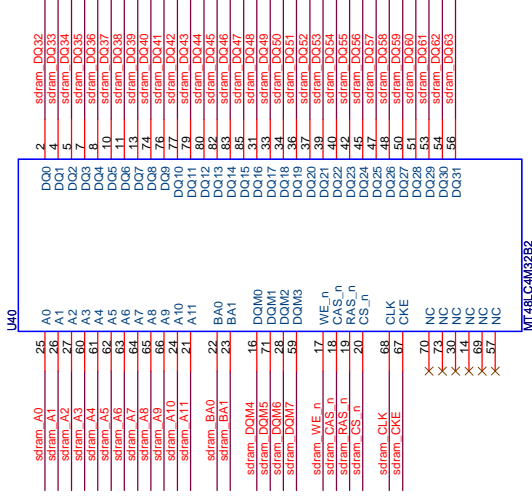
Proto2 Headers



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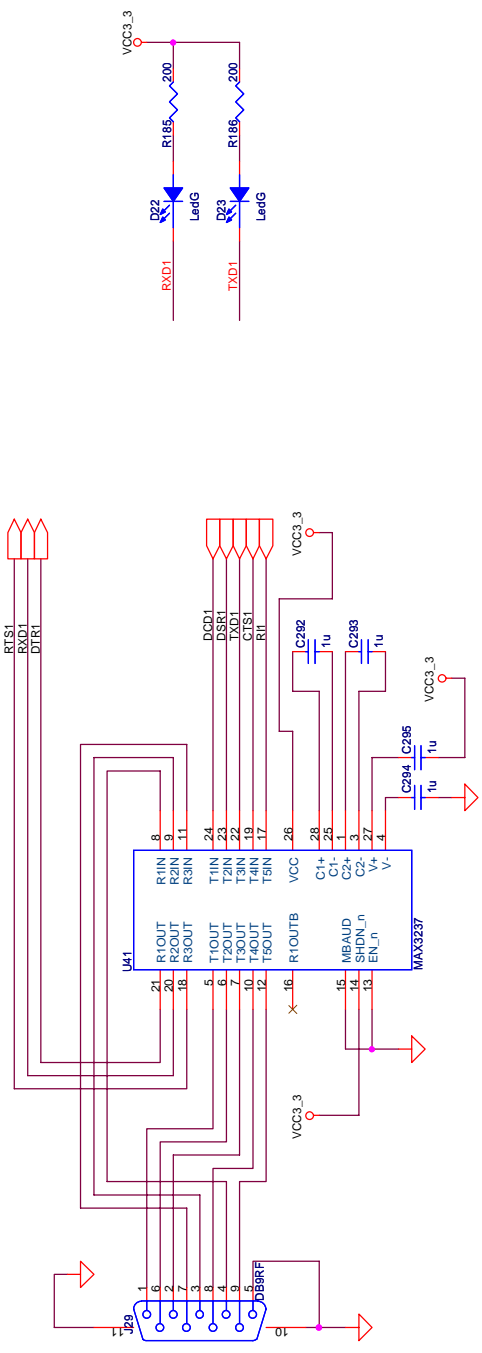
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Serial Ports

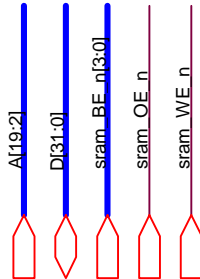
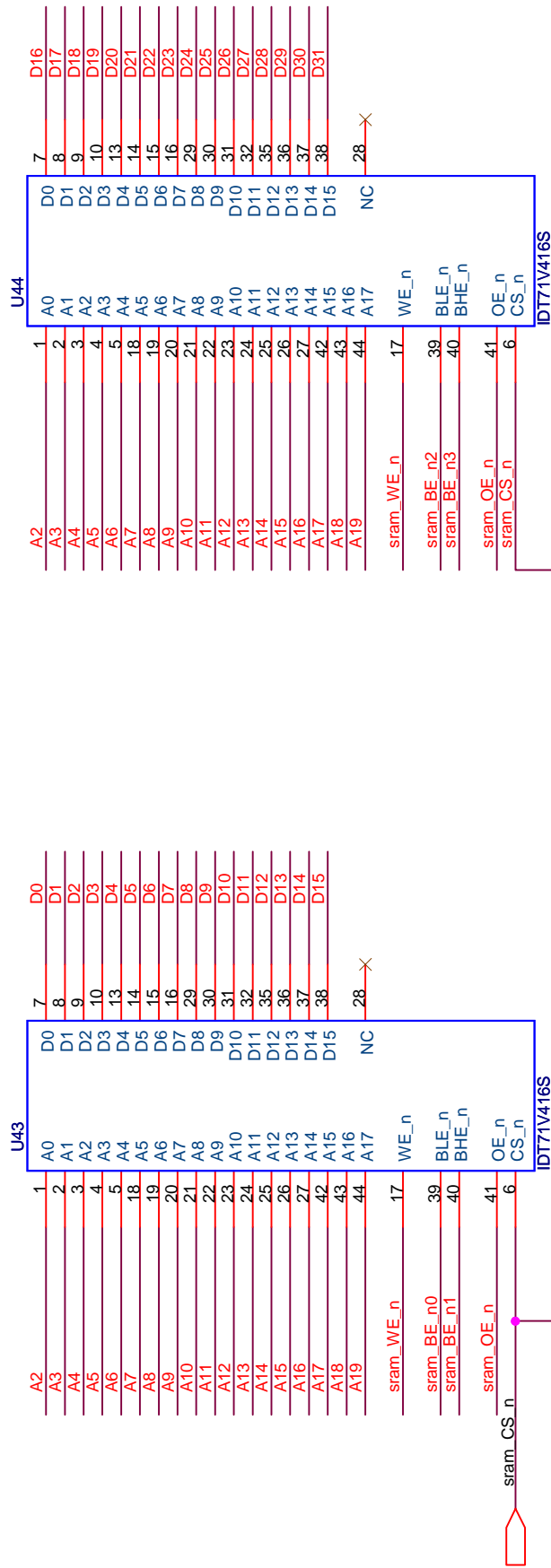


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SRAM



One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

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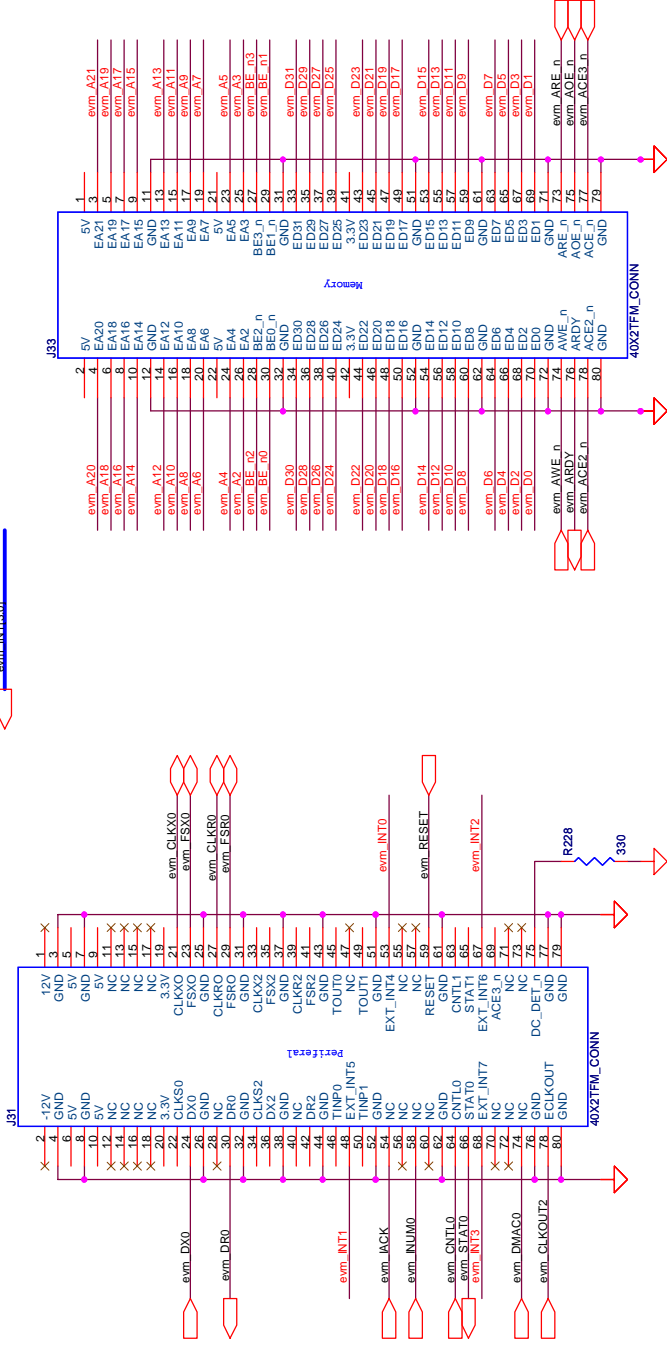
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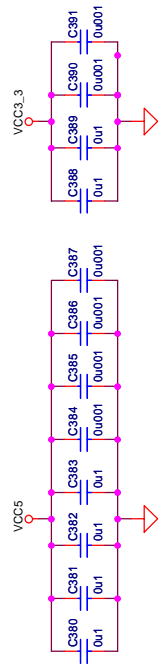
TI EVM Connector



3.00" apart



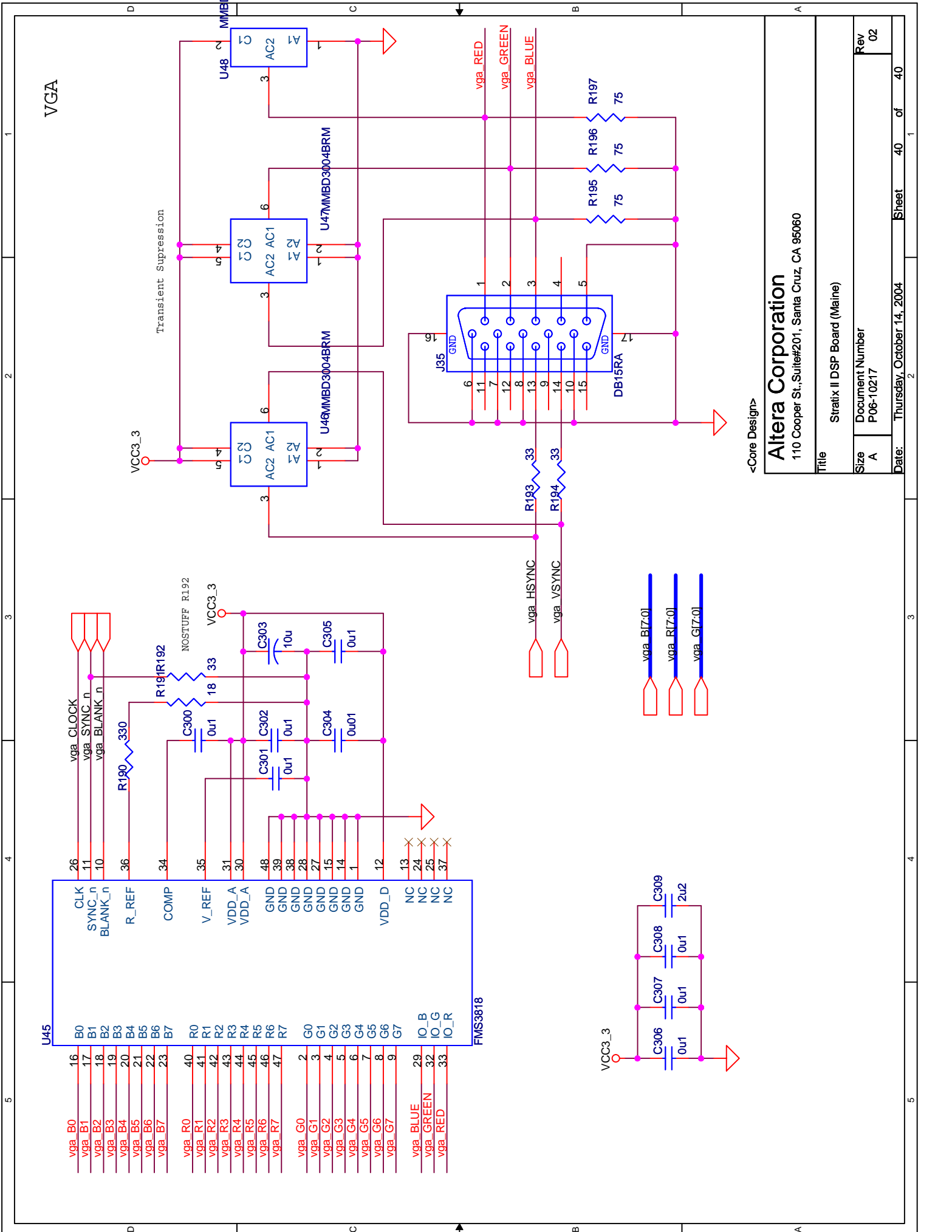
These connectors reference the TI 6416 board



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VGA

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