

This errata sheet provides updated information about known device issues affecting Stratix® IV E devices.

## Production Device Issues for Stratix IV E Devices

Table 1 lists the issues and affected Stratix IV E production devices.

**Table 1. Production Device Issues for Stratix IV E Devices (Part 1 of 2)**

Issue	Affected Devices	Planned Fix
<p><b>“PLL phasedone Signal Stuck at Low”</b></p> <p>In some cases, the Stratix V phase-locked loop (PLL) blocks exhibit the phasedone signal stuck at low during the PLL dynamic phase shift.</p>	All Stratix IV E devices (ES and production)	Quartus II software version 12.0 and later.
<p><b>“Remote System Upgrade”</b></p> <p>The remote system upgrade feature fails when loading an invalid configuration image.</p>	All Stratix IV GX (ES and production) devices	Quartus II software version 9.1 and later.
<p><b>“EDCRC False Errors”</b></p> <p>The error detection CRC (SEU detection) feature may falsely assert the CRC_ERROR signal when no SEU event has occurred.</p>	All production devices	—
<p><b>“I/O Jitter”</b></p> <p>Affected Stratix IV E production devices may exhibit higher than expected jitter on general purpose I/O pins.</p>	EP4SE360, EP4SE530, EP4SE820	EP4SE360 Rev B, EP4SE530 Rev E, EP4SE820 Rev B
<p><b>“Fast Passive Parallel (FPP) Mode Configuration Failures at High DCLK Frequency”</b></p> <p>Stratix IV E configuration might fail in FPP mode when the DCLK frequency is set to 125 MHz with a 60/40 or 40/60 duty cycle.</p>	All production devices	—
<p><b>“FPP Mode Configuration Failures When the Minimum Hold Time (t<sub>DH</sub>) is set to 0 ns or 24 ns”</b></p> <p>Stratix IV E configuration fails in FPP mode when the minimum data hold time (t<sub>DH</sub>) is set to 0 ns for uncompressed and unencrypted configuration data or 24 ns for compressed and/or encrypted data.</p>	All production devices	—
<p><b>“M144K RAM Block Lock-Up”</b></p> <p>M144K RAM blocks may lock up if there is a glitch in the clock source.</p>	All production devices	—

**Table 1. Production Device Issues for Stratix IV E Devices (Part 2 of 2)**

Issue	Affected Devices	Planned Fix
<p><a href="#">“Stratix IV E Power-up Sequencing on Production Devices”</a></p> <p>The device fails to power up and exit POR at low temperatures when <math>V_{CC}</math> is powered after <math>V_{CCAUX}</math>.</p>	All production devices	—
<p><a href="#">“Higher Power Supply Current During Power-Up for <math>V_{CCPD}</math>”</a></p> <p>Higher power-up current requirements are needed for <math>V_{CCPD}</math> power supply.</p>	All production devices	Refer to <a href="#">“Higher Power Supply Current During Power-Up for <math>V_{CCPD}</math>”</a>

## PLL phasedone Signal Stuck at Low

In some cases, the Stratix IV PLL blocks exhibit the phasedone signal stuck at low during the PLL dynamic phase shift. When the PLL phasedone signal is stuck at low, the intended phase shift does not happen. You can recover from the PLL phasedone signal being stuck at low by resetting the PLL or by restarting the phase shift operation by asserting the `phasestep` signal.

### Solution

To resolve the PLL phasedone signal stuck at low issue, the Altera PLL megafunction is enhanced to automatically restart the phase shift operation internally in the Altera PLL megafunction whenever the PLL phasedone signal is stuck at low. Restarting the phase shift operation compensates for the missing phase shift operation and also recovers the phasedone signal.

This Altera PLL megafunction solution will be implemented in the Quartus II software version 12.0 and later. Altera recommends upgrading to the latest Quartus II software, regenerating the PLL megafunction, and recompiling your design.

Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.1 SP1 to upgrade the PLL megafunction with the solution. To download and install the Quartus II software patch, refer to the [PLL Phasedone Stuck at Low Solution](#).




If you need additional support, file a service request using [mySupport](#).

## Remote System Upgrade

The remote system upgrade feature does not operate correctly when you initiate a reconfiguration cycle that goes from a factory configuration image to an invalid application configuration image. In this scenario, the device fails to revert back to the factory configuration image after a configuration error is detected while loading the invalid application configuration image. The failure is indicated by a continuous toggling of the `nSTATUS` pin.

In correct operation, the device reverts to the factory configuration image after a configuration error is detected with the invalid configuration image.

 An invalid application configuration image is classified as one of the following:

- A partially programmed application image
- A blank application image
- An application image assigned with a wrong start address

The remote system upgrade feature works correctly with all other reconfiguration trigger conditions.


This issue is addressed by enabling the Reconfig POF Checking feature in the updated ALTREMOTE\_UPDATE megafunction and is available in the Quartus® II software version 9.1 and later.

For more information about how to enable the Reconfig POF Checking feature, refer to [AN 603: Active Serial Remote System Upgrade Reference Design](#).

## EDCRC False Errors

The error detection cyclic redundancy check (CRC) (single event upset [SEU] detection) feature may falsely assert the CRC\_ERROR signal when no SEU event has occurred. The falsely asserted CRC\_ERROR signal happens because the configuration RAM is incorrectly read for the EDCRC checks. In this scenario, the configuration RAM data and the functionality of the device are not affected.

- If EDCRC is not critical to your system, turn it off.
- If EDCRC is required, insert a soft IP in your design.


 For more support and to request the soft IP, file a service request using [mySupport](#).

## I/O Jitter

Affected Stratix IV E production devices (refer to [Table 1](#)) may exhibit up to  $\pm 50$  ps higher than expected jitter on general purpose I/O pins. I/O pins in LVDS mode (including dynamic phase alignment [DPA] and soft clock data recovery [CDR]) are not affected. The actual amount of additional jitter depends on the device switching activity.

The EP4SE230 production ordering code is not affected.

Altera is fixing this issue in the next revision of production devices, which will meet all current jitter specifications.

 For further support, file a service request using [mySupport](#).

## Fast Passive Parallel (FPP) Mode Configuration Failures at High DCLK Frequency

Stratix IV E devices might fail to configure in FPP mode if the DCLK frequency is set to 125 MHz with a 60/40 or 40/60 duty cycle. When the device fails to configure in FPP mode, the device pulls the nSTATUS pin low and the configuration host may initiate a reconfiguration.

This problem affects all Stratix IV E devices.

For successful FPP configuration at 125 MHz for devices with the density of the EP4SE360 and lower, set the duty cycle to 45/55, 55/45, or higher. These settings correspond to a minimum DCLK high time ( $t_{CH}$ ) and a minimum DCLK low time ( $t_{CL}$ ) of 3.6 ns.

For EP4SE530 devices, reduce the DCLK frequency to 100 MHz or lower and set the duty cycle to 45/55, 55/45, or higher. These settings correspond to a minimum DCLK high time ( $t_{CH}$ ) and a minimum DCLK low time ( $t_{CL}$ ) of 4.5 ns.

For EP4SE820 devices, reduce the DCLK frequency to 80 MHz or lower and set the duty cycle to 45/55, 55/45, or higher. These settings correspond to a minimum DCLK high time ( $t_{CH}$ ) and a minimum DCLK low time ( $t_{CL}$ ) of 5.6 ns.

## FPP Mode Configuration Failures When the Minimum Hold Time ( $t_{DH}$ ) is set to 0 ns or 24 ns

Stratix IV E devices might fail to configure in FPP mode if the minimum hold time ( $t_{DH}$ ) for the configuration data is set to 0 ns for uncompressed and unencrypted configuration data, or 24 ns for compressed and/or encrypted data. When the configuration fails, the device pulls the nSTATUS pin low and the configuration host may initiate a reconfiguration.

This problem affects all Stratix IV E devices.

You can successfully configure the Stratix IV E devices in FPP mode by setting the minimum hold time ( $t_{DH}$ ) for the uncompressed and unencrypted configuration data to 1 ns or higher. For compressed and/or encrypted data, set the minimum hold time ( $t_{DH}$ ) to  $3 * 1/f_{DCLK} + 1$  ns or higher ( $f_{DCLK}$  is your DCLK frequency setting). Alternatively, you can drive the configuration data out on the falling edge of the DCLK.



The MAX II Parallel Flash Loader drives out configuration data on the falling edge of the DCLK. This issue does not affect you if you use the Max II Parallel Flash Loader as the configuration controller.

## M144K RAM Block Lock-Up

M144K blocks may lock up if there is a glitch in the clock source when rden equals 1. In the lock-up state, the RAM block does not respond to read or write operations and requires an FPGA reconfiguration to restore operation. The lock-up occurs within the M144K RAM in the Read Timer Trigger circuitry. A clock glitch may inadvertently freeze the Read Timer Trigger circuitry, locking the RAM block in its last operation. MLABs and M9K RAM blocks are not affected.

The workaround is to add clock-enable logic, an internal phase-locked loop (PLL), or clock-generation logic (for example, a clock divider). You can add clock-enable logic (internal or external) to disable RAM block operation until the clock is stable. You can also gate the clock internally or externally. If FPGA resources permit, you can use an internal PLL or clock-generation logic to ensure a stable clock source at the RAM block input.

The Read Timer circuitry makes RAM block operation independent of the input clock duty cycle, thus maximizing design performance. If you cannot provide a stable clock, use the **DCD** option in the Quartus II software version 9.1 or later to work around this problem. When the M144K block uses the **DCD** option, the block does not exhibit the lock-up behavior, but clock high-time requirements are increased and  $f_{MAX}$  performance is degraded.

If you cannot provide a stable clock input without glitches, to enable the **DCD** option in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **Settings**.
2. In the **Category** list, select **Fitter Settings**.
3. Click **More Settings**.
4. Under **Existing option settings**, set **M144K Block Read Clock Duty Cycle Dependency** to **On**.
5. Click **OK**.
6. Compile your design.

Use the **.qsf** variable instead of the previous instructions to make a global assignment.

**DCD** is on globally by adding the following line to the project's **.qsf** (the default is **Off**):

```
set_global_assignment -name M144K_BLOCK_READ_CLOCK_DUTY_CYCLE_DEPENDENCY ON
```

Alternatively, you can also apply this setting to individual M144K blocks with the Assignment Editor.

The global and per instance assignments can be mixed. For example, you can set **DCD** to **On** globally, but set it to **Off** for an instance. You can also set it to **On** for an instance.

## Stratix IV E Power-up Sequencing on Production Devices

Stratix IV E devices might fail to power up correctly at low temperatures when the  $V_{CC}$  (0.9 V) power supply powers up after the  $V_{CCAUX}$  (2.5 V) power supply. The power-up issue occurs because the FPGA device fails to exit power-on reset (POR), as indicated by the **nSTATUS** pin being stuck low. Configuration cannot begin when the **nSTATUS** pin is low.

The problem affects all Stratix IV E devices. Engineering sample devices are not affected.

Production devices must use the power-up sequence board design modifications to successfully power-up and exit POR on production devices, by fully powering  $V_{CC}$  before  $V_{CCAUX}$  begins to ramp. There is no dependency on the ramp rate for  $V_{CC}$  and  $V_{CCAUX}$ . The published ramp rate specifications still apply.



You can successfully use the hot socketing feature if you use the  $V_{CC}$  before  $V_{CCAUX}$  power sequence board design modification.

Contact Altera for Technical Support if you require assistance with implementing these board design changes.

## Stratix IV E ES Device Issues

Table 2 lists the issues and which Stratix IV E ES devices are affected by each issue.

**Table 2. Issues for Stratix IV E ES Devices**

Issue	Affected Devices	Planned Fix
EDCRC False Errors The error detection CRC (SEU detection) feature may falsely assert the CRC_ERROR signal when no SEU event has occurred.	EP4SE530 ES devices	—
Remote System Upgrade Remote System Upgrade fails when loading an invalid configuration image.	EP4SE530 ES devices	Production devices
M9K/M144K RAM Block Lock-up M9K/M144K RAM blocks may lock up if there is a glitch in the clock source.	EP4SE530 ES devices	None
CRC Error Injection Feature The CRC Error Injection feature may not operate correctly.	EP4SE530 ES devices	Production devices
Higher Power Supply Current During Power-Up for V <sub>CCPD</sub> Higher power-up current requirements are needed for V <sub>CCPD</sub> power supply.	EP4SE530 ES devices	None
M144K Write with Dual-Port Dual-Clock Modes M144K RAM blocks may not operate correctly in dual-port dual-clock modes.	EP4SE530 ES devices	Production devices
Automatic Clock Switchover Automatic clock switchover feature may not operate correctly.	EP4SE530 ES devices	Production devices
CRC Error Detection Feature MLAB RAM blocks may not operate correctly with the CRC Error Detection feature enabled.	EP4SE530 ES devices	Production devices
Higher V <sub>CC</sub> Power Supply Levels Stratix IV E ES devices require higher V <sub>CC</sub> power supply levels.	EP4SE530 ES devices (all speed grades)	Production devices
I/O Jitter Stratix IV E ES devices may exhibit higher than expected jitter on all I/O pins.	EP4SE530 ES devices	Production devices
Higher Minimum f <sub>INPFD</sub> Setting Stratix IV E ES devices may exhibit higher than expected PLL jitter at low f <sub>INPFD</sub> settings.	EP4SE530 ES devices	Production devices
High I/O pin leakage current Top and bottom I/O banks show higher leakage than the published Stratix IV Data Sheet version 2.1 specifications.	EP4SE530 ES devices	EP4SE530 production devices
Higher standby current for V <sub>CC</sub> power supply Higher than specified standby current on the V <sub>CC</sub> supply.	EP4SE530 ES devices	EP4SE530 production devices
Reduced M9K/M144K performance Reduced M9K/M144K performance for Stratix IV E ES devices.	EP4SE530 ES devices	EP4SE530 production devices
DPA misalignment Dynamic phase alignment (DPA) circuitry in Stratix IV E ES devices might get stuck at the initial configured phase or move to the optimum phase after a longer than expected period of time.	EP4SE530 ES devices	For more information, refer to "DPA Misalignment" on page 11.

## EDCRC False Errors

The error detection cyclic redundancy check (CRC) (single event upset [SEU] detection) feature may falsely assert the `CRC_ERROR` signal when no SEU event has occurred. The falsely asserted `CRC_ERROR` signal happens because the configuration RAM is incorrectly read for the EDCRC checks. In this scenario, the configuration RAM data and the functionality of the device are not affected.

- If EDCRC is not critical to your system, turn it off.
- If EDCRC is required, insert a soft IP in your design.



For more support and to request the soft IP, file a service request using [mySupport](#).

## Remote System Upgrade

The remote system upgrade feature does not operate correctly when you initiate a reconfiguration cycle from a factory configuration image to an invalid application configuration image. In this scenario, Stratix IV GX and Stratix IV E devices fail to revert to the factory configuration image after a configuration error is detected while loading the invalid application configuration image. The failure is indicated by a continuous toggling of the `nSTATUS` pin.

In correct operation, Stratix IV GX and Stratix IV E devices revert to the factory configuration image after a configuration error is detected with the invalid configuration image.



An invalid application configuration image is classified as one of the following:

- A partially programmed application image
- A blank application image
- An application image assigned with a wrong start address

The remote system upgrade feature works correctly with all other reconfiguration trigger conditions.

The remote system upgrade feature issue is addressed by using the updated `ALTREMOTE_UPDATE` megafunction and is available in the Quartus II software version 9.1 or later, or contact Altera technical support for the software patch available with the Quartus II software version 9.0 SP2.

## M9K/M144K RAM Block Lock-up

The M9K and M144K blocks can lock up if the clock source glitches when  $rden=1$ , which can occur if the clock source is not from a PLL. In this state, a RAM block no longer responds to read or write operations and requires an FPGA reconfiguration to restore operation. The issue occurs in the Read Timer Trigger circuitry, where a glitch-prone non-PLL clock may inadvertently freeze the Read Timer Trigger circuitry, locking the RAM block in its last operation. All RAM block modes are affected. MLABs are not affected.

The workaround is to add clock-enable logic, an internal PLL, or clock generation logic (for example, a clock divider). You can add clock-enable logic (internal or external) to disable RAM block operation until the clock is stable. You can also gate the clock internally or externally. If FPGA resources permit, you can use an internal PLL or clock generation logic to ensure a stable clock source at the RAM block input.

## CRC Error Injection Feature

The CRC Error Injection feature on Stratix IV E ES devices may not operate correctly when running the `EDERROR_INJECT JTAG` instruction. The `CRC_ERROR` output status pin may remain low, incorrectly indicating no CRC errors.

The CRC Error Injection feature issue only occurs with the error injection block and is fixed in production devices. The CRC Error Detection feature operates correctly as expected, and is not affected by this issue.

If you need to use the CRC Error Injection feature with Stratix IV E ES devices, contact Altera® Technical Support.

## Higher Power Supply Current During Power-Up for $V_{CCPD}$

Stratix IV E ES devices require higher power-up current levels for the  $V_{CCPD}$  power supply than previously specified. The PowerPlay Early Power Estimator (EPE) version 9.0.1 correctly shows the  $V_{CCPD}$  power-on current for Stratix IV E ES devices. The Quartus II software and PowerPlay EPE version 9.1 and later versions correctly show the  $V_{CCPD}$  power-on current for production devices.

Stratix IV E ES and production device functionality is not affected by this issue, even if your  $V_{CCPD}$  power supply is designed with output current levels below what the Quartus II software and/or EPE specify. Stratix IV E ES and production devices will power-up and operate correctly as expected, provided the supplies power up monotonically and the minimum voltage requirement is met.  $V_{CCPD}$  must meet the minimum power supply voltage requirement for the device to exit power-on reset (POR). After the device exits POR, the  $V_{CCPD}$  current requirements return to what is reported by Altera's power estimation tools. Overall thermal power and operating current levels are not affected by this issue.

If there are other devices on the board that share the  $V_{CCPD}$  power supply, you can use the Quartus II software and/or the EPE to estimate power supply current requirements. This analysis may be needed if the other devices on the board have stringent power supply integrity requirements.

There is no planned fix for the higher power-up current requirements.

## M144K Write with Dual-Port Dual-Clock Modes

M144K RAM blocks in dual-port dual-clock modes may fail to operate correctly, affecting applications such as DCFIFO memories, where data is transferred between two separate clock domains.

If you are using Stratix IV E ES devices with the Quartus II software version 9.0, you must recompile your design and manually avoid all use of M144K RAM blocks in dual-port dual-clock modes. The Quartus II software version 9.0 SP1 automatically disables use of dual-port dual-clock modes in all M144K RAM blocks. In both cases, your design's usage of M9K RAM blocks may increase as a result.

This issue is fixed in production devices.



You can download a software patch to help with M144K RAM blocks in dual-port dual-clock mode failure at:

[http://www.altera.com/support/kdb/solutions/rd04092009\\_699.html](http://www.altera.com/support/kdb/solutions/rd04092009_699.html)

## Automatic Clock Switchover

The PLL Automatic Clock Switchover feature may fail to operate correctly on Stratix IV E ES devices when the two clocks are running different frequencies. If both clocks are running at the same frequency, there is no impact to your design. The following modes are affected:

- Automatic
- Automatic with Manual Override

You may observe two possible issues:

- Switchover from `inclk0` to `inclk1`, even though `inclk0` is active (and vice-versa)
- `clkbad[0,1]` status signals may glitch, even if the input clocks are active



Manual clock switchover mode operates correctly as expected and is not affected.

This issue is fixed in production devices.

## CRC Error Detection Feature

The CRC Error Detection feature, when you enable single event upset (SEU) detection, may cause the MLAB RAM blocks to operate incorrectly in Stratix IV E ES devices. Write operations in MLAB RAM blocks are affected with all CRC Error Detection divisor settings.



The CRC Error Detection feature operates correctly as expected. FPGA configuration bits are not affected by this issue.

Disabling the CRC Error Detection feature in your design compilation with the Quartus II software prevents this issue from occurring in Stratix IV E ES devices.

This issue is fixed in production devices.



You can download a software patch to help with the CRC Error Detection feature issue at: [http://www.altera.com/support/kdb/solutions/rd04092009\\_699.html](http://www.altera.com/support/kdb/solutions/rd04092009_699.html)

## Higher $V_{CC}$ Power Supply Levels

Stratix IV E ES devices require higher  $V_{CC}$  power supply levels (Table 3).

**Table 3. Power Supply Levels for Stratix IV E ES Devices**

Power Supply	Power Supply Level (V)	Description
$V_{CC}$	0.95	Core voltage and periphery circuitry power supply
$V_{CCD\_PLL}$	0.95	PLL digital power supply

EP4SE530 ES devices require  $V_{CC}$  and  $V_{CCD\_PLL}$  power supplies set to  $0.95\text{ V} \pm 0.03\text{ V}$  for all speed grades.

Use the Stratix IV E PowerPlay EPE version 9.0.1 or later to estimate current and power/thermal requirements for Stratix IV E ES devices with the required higher power supply levels. The Stratix IV E PowerPlay EPE version 9.0 reflects current and power estimates for production devices at data sheet specifications only.

Production devices will not operate at these higher power supply levels. If needed, design your power supplies to support dropping power supply levels back to data sheet specification for production devices.

There are no reliability issues with Stratix IV E ES devices at these higher power supply levels.

## I/O Jitter

Stratix IV E ES devices may exhibit  $\pm \sim 100$  ps higher than expected jitter on all I/O pins. The actual amount of additional jitter is application and toggle-rate dependent.

Altera fixed the issue in production devices, which meet all current jitter specifications.

If you are using Stratix IV E ES devices, you need to account for this additional timing uncertainty in all I/O timing closure budgets.

## Higher Minimum $f_{INPFD}$ Setting

Stratix IV E ES devices may exhibit higher than expected PLL jitter at low  $f_{INPFD}$  settings. Raising the minimum  $f_{INPFD}$  to 25 MHz removes the additional PLL jitter in Stratix IV E ES devices.

Altera fixed the issue in production devices, which meet the current  $f_{INPFD}$  minimum of 5 MHz.

If you are using Stratix IV E ES devices, review your  $f_{INPFD}$  settings by searching under "Nominal PFD Frequency" in each PLL section of your **.fit.rpt** compilation report file. If needed, recompile your design in the Quartus II software with modified PLL settings to achieve the higher minimum  $f_{INPFD}$ .



For more information about the ALTPLL megafunction, refer to the *Quartus II Handbook* or the *Phase-Locked Loops (ALTPLL) Megafunction User Guide*.

## High I/O Pin Leakage Current

Top and bottom I/O pin leakage current is higher for Stratix IV E ES devices than production devices. Side I/O banks are not affected. For Stratix IV E ES device I/O pin leakage current on top and bottom I/O banks, refer to [Table 4](#).

**Table 4. I/O Pin Leakage Current for Top and Bottom I/O Banks**

Temperature	I/O Bank Voltage (V)					Units
	3.0	2.5	1.8	1.5	1.2	
25°C	35	25	15	11	9	μA
85°C	140	100	60	45	35	μA

These I/O pin leakage current values apply to Stratix IV E ES silicon only and not to production silicon.

## Higher Standby Current for V<sub>CC</sub> Power Supply

You can expect to see higher standby I<sub>CC</sub> values on the V<sub>CC</sub> power supply for Stratix IV E ES devices than indicated in the Quartus II software version 9.0 and the Stratix IV E PowerPlay EPE version 9.0. The higher standby I<sub>CC</sub> current for the V<sub>CC</sub> power supply is fixed in production devices.

Use the Stratix IV E PowerPlay EPE version 9.0.1 or later to estimate current and power/thermal requirements for the Stratix IV E ES device. The Stratix IV E PowerPlay EPE version 9.0 will not be updated with these higher standby current values.

## Reduced M9K/M144K Performance

M9K/M144K f<sub>MAX</sub> and t<sub>CO</sub> performance for Stratix IV E ES devices may be lower than indicated in the Quartus II software version 8.1. Compile your design in the Quartus II software version 9.0 or later to estimate the impact on your design.

## DPA Misalignment

Stratix IV E DPA circuitry for Stratix IV E ES devices occasionally become stuck at the initial configured phase or take significantly longer than expected to select the optimum phase. A non-ideal phase may result in data bit errors, even after the DPA lock signal has gone high. Resetting the DPA circuit may not alleviate the problem; in fact, resetting the DPA circuit might trigger the problem. LVDS receivers configured in DPA mode are affected. LVDS receivers configured in soft CDR mode with 0 parts-per-million (ppm) difference (synchronous interface) are also affected.

For applications with flexibility in the choice of training patterns, Altera recommends choosing bit sequences with more data transitions and a non-cyclical pattern similar to a PRBS or K28.5 code sequence.

For applications using a fixed, cyclical, or data transition sparse training pattern (for example, if you are using the SPI 4.2 protocol, which specifies a training pattern of ten 0s and ten 1s), turn on the **DPA PLL Calibration** option (available in the Quartus II software version 9.0 and later) in the ALTLVDS MegaWizard™ Plug-In Manager.



There are two caveats when enabling the **DPA PLL Calibration** option:

- PLL merging (merging receiver [RX] and RX or merging RX and transmitter [TX] PLL) is not automatically supported by the ALTLVDS megafunction; use the **external PLL** option to handle PLL merging separately.
- Timing for all PLL outputs is pulled in by 1/4 of the voltage controlled oscillator ( $V_{CO}$ ) phase during the PLL calibration process. This different timing must be taken into account for external I/O pin timing interfaces and for clock domain transfers (without a FIFO) when the clocks are not all from this same PLL.



For more information about the **DPA PLL Calibration** option, refer to the *LVDS SERDES Transmitter/Receiver (ALTLVDS\_TX and ALTLVDS\_RX) Megafunction User Guide* planned release corresponding to the Quartus II software version 9.0. Until the User Guide is updated, in the interim, file a service request using [mySupport](#).

## Document Revision History

Table 5 lists the revision history for this Errata Sheet.

**Table 5. Document Revision History (Part 1 of 2)**

Date	Version	Changes
December 2011	2.8	Added the “PLL phasedone Signal Stuck at Low” section.
September 2011	2.7	<ul style="list-style-type: none"> <li>■ Added the “Remote System Upgrade” section.</li> <li>■ Minor text edits.</li> </ul>
June 2011	2.6	Added the “EDCRC False Errors” section.
March 2011	2.5	Update the “I/O Jitter” section of Table 1.
January 2011	2.4	<ul style="list-style-type: none"> <li>■ Updated the “Fast Passive Parallel (FPP) Mode Configuration Failures at High DCLK Frequency” section.</li> <li>■ Converted to the new template.</li> </ul>
May 2010	2.3	<ul style="list-style-type: none"> <li>■ Added the “I/O Jitter” section.</li> </ul>
April 2010	2.2	<ul style="list-style-type: none"> <li>■ Added “Fast Passive Parallel (FPP) Mode Configuration Failures at High DCLK Frequency”</li> <li>■ Added “FPP Mode Configuration Failures When the Minimum Hold Time (tDH) is set to 0 ns or 24 ns”</li> <li>■ Updated “DPA Misalignment” and removed this issue from Production devices section</li> <li>■ Updated “Higher Power Supply Current During Power-Up for VCCPD”</li> </ul>
January 2010	2.1	<ul style="list-style-type: none"> <li>■ Updated “Stratix IV E Power-up Sequencing on Production Devices”.</li> <li>■ Added “DPA Misalignment” section to production devices.</li> </ul>

**Table 5. Document Revision History (Part 2 of 2)**

Date	Version	Changes
November 2009	2.0	Added: <ul style="list-style-type: none"> <li>■ “Stratix IV E Production Device Issues”</li> <li>■ “M144K RAM Block Lock-Up”</li> <li>■ “Stratix IV E Power-up Issue on Production Devices”</li> </ul> Updated the following with link to software patch: <ul style="list-style-type: none"> <li>■ “M144K Write with Dual-Port Dual-Clock Modes”</li> <li>■ “CRC Error Detection Feature”</li> </ul> Updated with fix in “Automatic Clock Switchover”.
August 2009	1.1	Added “Remote System Upgrade”
June 2009	1.0	<ul style="list-style-type: none"> <li>■ M9K/M144K RAM Block Lock-up</li> <li>■ CRC Error Injection Feature</li> <li>■ Higher Power Supply Current During Power-Up for <math>V_{CCPD}</math></li> <li>■ M144K Write with Dual-Port Dual-Clock Modes</li> <li>■ Automatic Clock Switchover</li> <li>■ CRC Error Detection Feature</li> <li>■ Higher <math>V_{CC}</math> Power Supply Levels</li> <li>■ I/O Jitter</li> <li>■ Higher Minimum <math>f_{INPFD}</math> Setting</li> <li>■ High I/O Pin Leakage Current</li> <li>■ Higher Standby Current for <math>V_{CC}</math> Power Supply</li> <li>■ Reduced M9K/M144K Performance</li> <li>■ DPA Misalignment</li> </ul>

