

This document addresses known errata and documentation issues for the Viterbi Compiler version 7.0. Errata are functional defects or errors, which may cause the Viterbi Compiler to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the Viterbi Compiler v7.0.

<i>Table 1. Viterbi Compiler v7.0 Issues</i>	
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For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

www.altera.com/literature/es/es_viterbi_70.pdf

Viterbi Compiler v7.0 Issues

This section describes the Viterbi Compiler v7.0 issues.

Hybrid & Parallel Architectures Can Be Selected Simultaneously

In IP Toolbench, on the Test Data tab if you enter information in Pattern A or Pattern B, the radio buttons on the Architecture and Code Sets tabs do not work correctly. For example, when you click the Architecture tab, both parallel and hybrid radio buttons can be selected simultaneously.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can lead to a misconfiguration of the Viterbi decoder, because it is not clear whether you have parallel or hybrid architecture selected.

Workaround

Only change or enter the information in Pattern A and Pattern B after you have set all other parameters.

Solution Status

This issue will be fixed in a future release of the Viterbi Compiler.

Decimal & Octal Can Be Selected Simultaneously

In IP Toolbench on the Code Sets tab, you can select both **Decimal** and **Octal** or turn them both off, on Linux 64-bit computers.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can lead to a misconfiguration of the Viterbi decoder, by entering erroneous polynomials.

Workaround

Select **Octal** and then select **Decimal** to leave only **Octal** selected.

Solution Status

This issue will be fixed in a future release of the Viterbi Compiler.

IP Functional Simulation Model Simulations Fail

The IP Toolbench-generated ModelSim Tcl script fails to set the timing resolution correctly to 1 ps—it is currently set to 1 ns.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can lead to failed simulations of the Viterbi decoder.

Workaround

Edit the `<variation name>_vsim_script.tcl`. Force the variable `timing_resolution` to 1 ps always.

Solution Status

This issue will be fixed in the next release of the Viterbi Compiler.

VHDL Viterbi Decoders Do Not Simulate in Synopsys VCS

When you simulate a VHDL Viterbi decoder in Synopsys VCS, you receive an error message.

Affected Configurations

This issue affects all VHDL Viterbi decoders.

Design Impact

You cannot simulate a VHDL Viterbi decoder in VCS.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future release of of Synopsys VCS.

Contact Information

For more information, contact Altera's mySupport website at www.altera.com/mysupport and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for Viterbi Compiler v7.0.

<i>Table 2. Viterbi Compiler v7.0 Errata Sheet Revision History</i>		
Version	Date	Errata Summary
1.0	December 2006	First release.



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