11. Hot Socketing and Power-On Reset in Cyclone III Devices

CIII51011-1.2

Introduction

Cyclone® III devices offer hot socketing, also known as hot plug-in, hot insertion, or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Cyclone III board in a system during system operation without causing undesirable effects to the board or to the running system bus.

The hot socketing feature removes complexity when using Cyclone III devices on PCBs containing a mixture of 3.0, 3.3, 2.5, 1.8, 1.5, and 1.2 V devices. With the Cyclone III hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Cyclone III hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Cyclone III devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

This chapter contains the following sections:

- "Cyclone III Hot-Socketing Specifications"
- "Hot-Socketing Feature Implementation in Cyclone III Devices"
- "Power-On Reset Circuitry"

Cyclone III Hot-Socketing Specifications

Cyclone III devices offer hot-socketing capability with all three features listed above without any external components or special design requirements. The hot-socketing feature in Cyclone III devices offers the following capabilities:

- The device can be driven before power-up without any damage to the device itself
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation

☞ Altera® uses GND as reference for the hot-socketing and I/O buffers circuitry designs. You must connect the GND between boards before connecting the V_{CCINT} and the V_{CCIO} power supplies to ensure device reliability and compliance to the hot-socketing specifications.

Devices Can Be Driven Before Power-Up

You can drive signals into the I/O pins, dedicated input pins, and dedicated clock pins of Cyclone III devices before or during power-up or power-down without damaging the device. Cyclone III devices support any power-up or power-down sequence (V_{CCIO} and V_{CCINT}) to simplify system level design.

I/O Pins Remain Tri-stated During Power-Up

A device that does not support hot socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot-socketing situation, the output buffers of the Cyclone III device are turned off during system power-up or power-down. A Cyclone III device also does not drive out until the device is configured and has attained proper operating conditions. The I/O pins are tri-stated until the device enters user mode with a weak pull-up resistor (R) to V_{CCIO}. For more information, refer to Figure 11–1.

You can power up or power down the V_{CCIO}, V_{CCA}, and V_{CCINT} pins in any sequence. The V_{CCIO}, V_{CCA}, and V_{CCINT} must have monotonic rise to their steady state levels. (For more information, refer to Figure 11–3). The maximum power ramp rate for fast POR time is 3 ms, and 50 ms for standard POR time, respectively. The minimum power ramp rate is 50 µs. V_{CCIO} for all I/O banks should be powered-up during device operation. All V_{CCA} pins must be powered to 2.5-V (even when PLLs are not used), and must be powered-up and powered-down at the same time. V_{CCD_PLL} must always be connected to V_{CCINT} through a decoupling capacitor and ferrite bead. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Cyclone III devices meet the following hot socketing specifications:

- The hot-socketing DC specification is $| I_{IOPIN} | < 300$ uA
- The hot-socketing AC specification is $| I_{IOPIN} | < 8$ mA for the ramp rate of 10 ns or more

For ramp rates faster than 10 ns on I/O pins, $|I_{IOPIN}|$ can be obtained with the equation $I = C\ dv/dt$, where C is the I/O pin capacitance and dv/dt is the slew rate. The hot-socketing specification takes into account the pin capacitance but not board trace and external loading capacitance. You must consider additional or separate capacitance for trace, connector, and loading.

I_{IOPIN} is the current for any user I/O pin on the device. The DC specification applies when all V_{CC} supplied to the device is stable in the powered-up or powered-down conditions.

A possible concern for semiconductor devices in general regarding hot socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins may be connected and driven by the active system before the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

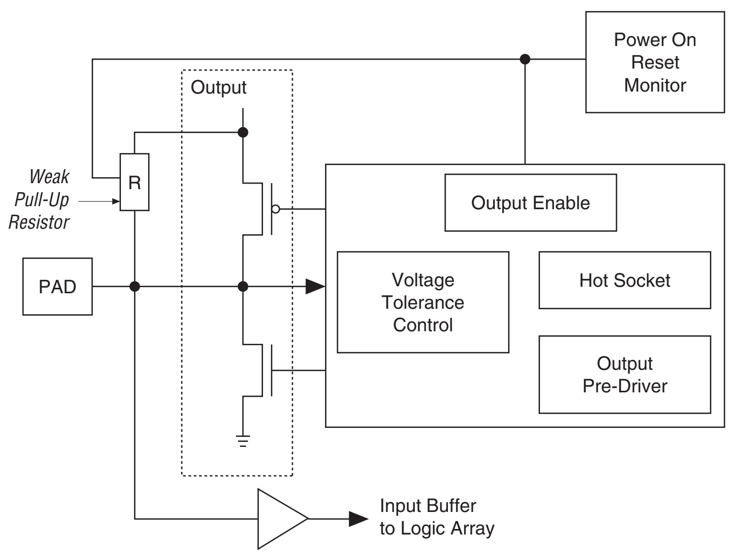
By design of the I/O buffers and hot socketing circuitry, Altera ensures that Cyclone III devices are immune to latch-up during hot socketing.

Hot-Socketing Feature Implementation in Cyclone III Devices

The hot-socketing feature disables the output buffer during power-up (either V_{CCINT} or V_{CCIO} supplies) or power-down. The hot-socket circuit generates an internal `HOTSCKT` signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage. Designs cannot use the `HOTSCKT` signal for other purposes. The `HOTSCKT` signal cuts off the output buffer to ensure that no DC current (except for weak pull-up leakage current) leaks through the pin. When V_{CC} ramps up slowly, V_{CC} is still relatively low, even after the internal `POR` signal (not available to the FPGA fabric used by customer designs) is released and the configuration is finished. The `CONF_DONE`, `nCEO`, and `nSTATUS` pins would fail to respond, as the output buffer cannot drive out because the hot-socketing circuitry keeps the I/O pins tri-stated at this low V_{CC} voltage. Therefore, the hot-socketing circuit has been removed on these configuration output or bidirectional pins to ensure that they are operational during configuration. These pins are expected to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 11–1.

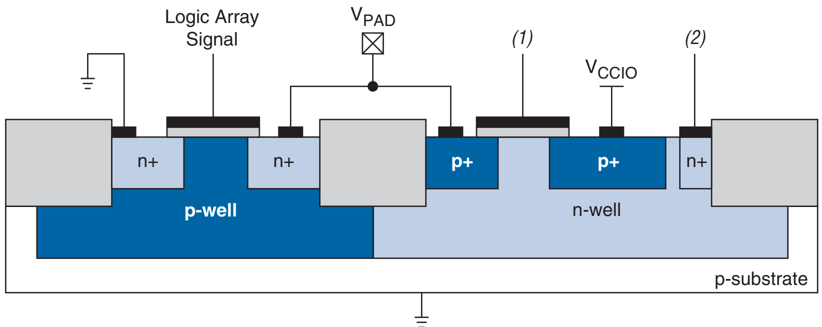
Figure 11–1. Hot Socketing Circuit Block Diagram for Cyclone III Devices



The POR circuit monitors the V_{CCINT}, V_{CCIO}, and V_{CCA}. voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} keeps the I/O pins from floating. The voltage tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not in user mode. The hot socket circuit prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

Figure 11–2 shows a transistor level cross section of the Cyclone III device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot socketing. There is no current path from signal I/O pins to V_{CCINT} or V_{CCIO} during hot socketing. The V_{PAD} leakage current charges the voltage tolerance control circuit capacitance.

Figure 11–2. Transistor Level Diagram of FPGA Device I/O Buffers



Notes to Figure 11–2:

(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.

(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

Cyclone III devices contain POR circuitry to keep the device in a reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the V_{CCINT}, V_{CCIO}, and V_{CCA} pin and tri-states all user I/O pins until the V_{CC} reaches the recommended operating levels. In addition, the POR circuitry also ensures the V_{CCIO} level of I/O banks 1, 6, 7, and 8 that contains configuration pins reach an acceptable level before configuration is triggered.

After the Cyclone III device enters user mode, the POR circuit continues to monitor the V_{CCINT} and V_{CCA} pin so that a brown-out condition during user mode can be detected. If the V_{CCINT} and V_{CCA} voltage sags below the POR trip point during user mode, the POR circuit resets the device. If the V_{CCIO} voltage sags during user mode, the POR circuit does not reset the device.

Wake-Up Time for Cyclone III Devices

In some applications, it may be necessary for a device to wake up very quickly in order to begin operation. The Cyclone III device offers the Fast-On feature to support fast wake-up time applications. For Cyclone III devices, `MSEL[3..0]` pin settings determine the POR time (t_{POR}) of the device. The fast POR ranges from 3 ms to 9 ms while the standard POR ranges from 50 ms to 200 ms.

For more information about the `MSEL[3..0]` pin settings, refer to the *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

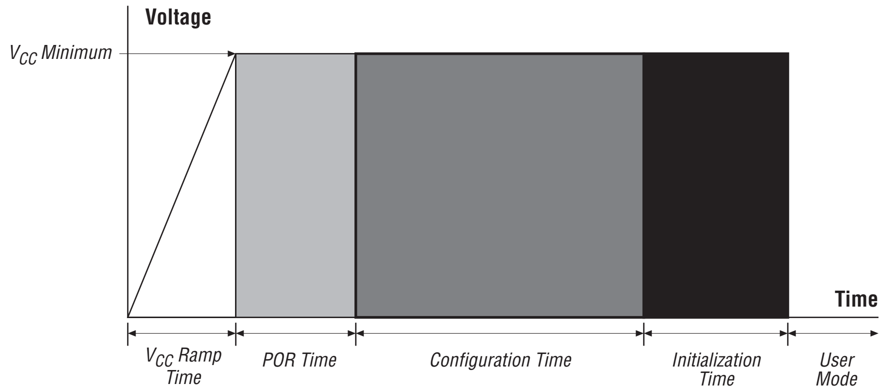
For Cyclone III devices, wake-up time consists of power-up, POR, configuration, and initialization. The device must properly go through all four stages to configure correctly and begin operation. You can calculate wake-up time using equation 11–4:

Equation 11–1.

$$\text{Wake-up Time} = V_{CC}\text{ Ramp Time} + POR\text{ Time} + \text{Configuration Time} + \text{Initialization Time}$$

Figure 11–3 illustrates the components of wake-up time.

Figure 11–3. Cyclone III Wake-Up Time



Note to Figure 11–3:

(1) V_{CC} ramp must be monotonic.

The V_{CC} ramp time and POR time depend on the power supply used in your system and the device `MSEL[3..0]` pin settings.

Configuration time depends on the configuration scheme you chose and the configuration file size. You can calculate configuration time by multiplying the number of bits in the configuration file with the period of the configuration clock. For fast configuration times, you should either use a fast passive parallel (FPP) configuration scheme with maximum DCLK frequency of 100 MHz or an active parallel (AP) configuration scheme with maximum DCLK frequency of 40 MHz. In addition, you can use passive serial (PS) with compression to reduce the configuration file size and speed up the configuration time. Passive parallel configuration mode does not support compression. The t_{CD2UM} or t_{CD2UMC} parameters determine the initialization time.

For more information about the t_{CD2UM} or t_{CD2UMC} parameters and configuration schemes, refer to the *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

If you cannot meet the maximum V_{CC} ramp time requirement, you must use an external component to hold `nCONFIG` low until the power supplies have reached their minimum recommended operating levels. Otherwise, the device may not properly configure and enter user mode.

Conclusion

Cyclone III devices offer hot socketing allowing the device to power-up successfully without any power-sequencing. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Referenced Documents

This chapter references the following document:

- *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*

Document Revision History

Table 11–1 shows the revision history for this chapter.

Table 11–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
October 2008 v1.2	■ Updated chapter to new template ■ Added handnote to the "Cyclone III Hot-Socketing Specifications" section	—
July 2007 v1.1	■ Updated "I/O Pins Remain Tri-stated During Power-Up" section ■ Updated Figure 11–3 ■ Added chapter TOC and "Referenced Documents" section	Added information that the power supply voltages must rise monotonically to their steady state levels
March 2007 v1.0	Initial release.	—

101 Innovation Drive
San Jose, CA 95134
www.altera.com
Technical Support
www.altera.com/support