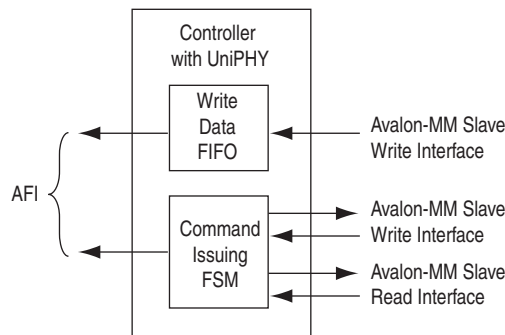


The QDR II and QDR II+ controller translates memory requests from the Avalon Memory-Mapped (Avalon-MM) interface to AFI, while satisfying timing requirements imposed by the memory configurations. QDR II and QDR II+ SRAM has unidirectional data buses, therefore read and write operations are highly independent of each other and each has its own interface and state machine.

## Block Description

This topic describes the blocks in the IP. Figure 5–1 shows a block diagram of the QDR II and QDR II+ SRAM controller architecture.

**Figure 5–1. QDR II and QDR II+ SRAM Controller Architecture Block Diagram**



## Avalon-MM Slave Read and Write Interfaces

The read and write blocks accept read and write requests, respectively, from the Avalon-MM interface. Each block has a simple state machine that represents the state of the command and address registers, which stores the command and address when a request arrives.

The read data passes through without the controller registering it, as the PHY takes care of read latency. The write data goes through a pipeline stage to delay for a fixed number of cycles as specified by the write latency. In the full-rate burst length of four controller, the write data is also multiplexed into a burst of 2, which is then multiplexed again in the PHY to become a burst of 4 in DDR.

The user interface to the controller has separate read and write Avalon-MM interfaces because reads and writes are independent of each other in the memory device. The separate channels give efficient use of available bandwidth.

## Command Issuing FSM

The command-issuing full-state machine (FSM) has two states: INIT and INIT\_COMPLETE. In the INIT\_COMPLETE state, commands are issued immediately as requests arrive using combinational logic and do not require state transitions.

## AFI

In the full-rate burst length of two configuration, the controller can issue both read and write commands in the same clock cycle. In the memory device, both commands are clocked on the positive edge, but the read address is clocked on the positive edge, while the write address is clocked on the negative edge. Care must be taken on how these signals are ordered in the AFI.

For the half-rate burst length of four configuration the controller also issues both read and write commands, but the AFI width is doubled to fill two memory clocks per controller clock. As the controller only issues one write command and one read command per controller clock, the AFI read and write signals corresponding to the other memory cycle are tied to no operation (NOP).

For information on the AFI, refer to [AFI 3.0 Specification](#).

## Avalon-MM and Memory Data Width

[Table 5-1](#) shows the data width ratio between the memory interface and the Avalon-MM interface. The half-rate controller does not support burst-of-2 devices because it under-uses the available memory bandwidth. Regardless of full or half-rate decision and the device burst length, the Avalon-MM interface must supply all the data for the entire memory burst in a single clock cycle. Therefore the Avalon-MM data width of the full-rate controller with burst-of-4 devices is four times the memory data width. For width-expanded configurations, the data width is further multiplied by the expansion factor (not shown in [table 5-1](#) and [5-2](#)).

**Table 5-1. Data Width Ratio**

Memory Burst Length	Half-Rate Designs	Full-Rate Designs
QDR II 2-word burst	No Support	2:1
QDR II and II+ 4-word burst	4:1	

## Signal Description

This topic discusses the signals for each interface.

For information on the AFI signals, refer to [AFI 3.0 Specification](#).

## Avalon-MM Slave Read Interface

Table 5-2 shows the list of signals of the controller's Avalon-MM slave read interface.

**Table 5-2. Avalon-MM Slave Read Signals**

Signal	Width	Direction	Avalon-MM Signal Type
avl_r_ready	1	Out	waitrequest_n
avl_r_read_req	1	In	read
avl_r_addr	≤20	In	address
avl_r_rdata_valid	1	Out	readdatavalid
avl_r_rdata	16, 18, 36, 72, 144	Out	readdata
avl_r_size	$\log_2(\text{MAX\_BURST\_SIZE}) + 1$	In	burstcount



The data width of the Avalon-MM interface is restricted to powers of two when using SOPC Builder or Qsys. Non-power-of-two data widths are supported when using the MegaWizard Plug-In Manager.



For more information about the Avalon interface, refer to [Avalon Interface Specifications](#).

## Avalon-MM Slave Write Interface

Table 5-3 shows the list of signals of the controller's Avalon-MM slave write interface.

**Table 5-3. Avalon-MM Slave Write Signals**

Signal	Width	Direction	Avalon-MM Signal Type
avl_w_ready	1	Out	waitrequest_n
avl_w_write_req	1	In	write
avl_w_addr	≤20	In	address
avl_w_wdata	18, 36, 72, 144	In	writedata
avl_w_be	2,4,8,16	In	byteenable
avl_w_size	$\log_2(\text{MAX\_BURST\_SIZE}) + 1$	In	burstcount



For more information about the Avalon interface, refer to [Avalon Interface Specifications](#).

## Document Revision History

Table 5-4 lists the revision history for this document.

**Table 5-4. Document Revision History**

Date	Version	Changes
November 2011	3.1	Harvested Controller chapter from 11.0 QDR II and QDR II+ SRAM Controller with UniPHY User Guide.