

This chapter describes the memory solutions that Altera provides.

Altera provides the fastest, most efficient, and lowest latency memory controllers. The controllers are designed to allow you to easily interface with today's higher speed memories.

Altera supports a wide variety of memory interfaces suitable for applications ranging from routers and switches to video cameras. You can easily implement Altera's intellectual property (IP) using the memory MegaCore functions through the Quartus II software. The Quartus II software also provides an external memory toolkit that helps you test the implementation of the IP in the FPGA device.

- Refer to the [External Memory Interface Spec Estimator](#) page for the maximum speed that supported by Altera FPGAs.

## Soft and Hard Memory IP

Altera's latest devices, the 28-nm FPGAs provide two types of memory solutions: soft memory IP and hard memory IP. Arria V and Cyclone V devices offer both soft and hard memory IP, while Stratix V devices offer only soft memory IP.

The soft memory IP gives you the flexibility to design your own interfaces to meet your system requirements and still benefit from the industry leading performance. The hard memory IP is designed to give you a complete out-of-the-box experience when designing a memory controller.

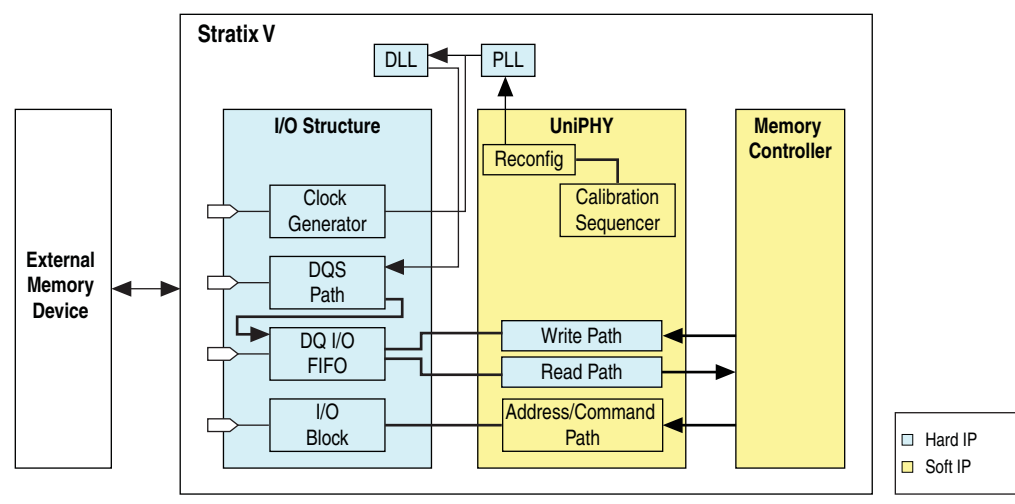
Table 1-1 lists the features of the soft and hard memory IP.

**Table 1-1. Features of the Soft and Hard Memory IP**

Soft Memory IP	Hard Memory IP
<ul style="list-style-type: none"> <li>■ Consists of a DDR2 or DDR3 SDRAM high-performance memory controller with UniPHY IP.</li> <li>■ Has hardened read and write data paths to ensure your design meets timing at the highest speeds. The data paths include I/O, phase-locked loops (PLLs), delay-locked loop (DLL), and read and write FIFO buffers.</li> <li>■ Allows you to choose the location to place the memory controller and the ability to size the memory controller based on the system requirements, especially in the Stratix V devices.</li> </ul>	<ul style="list-style-type: none"> <li>■ Consists of a DDR2 or DDR3 SDRAM high-performance memory controller with a hard UniPHY IP, and a multiport front-end block.</li> <li>■ Has a fixed location on the die and a fixed maximum width; <math>\times 32</math> for Arria V devices and <math>\times 16</math> for Cyclone V devices.</li> <li>■ Runs at full rate to allow decreased latency and to minimize the required bus width of signals going into the core of the device.</li> <li>■ Simplifies the overall memory design in Arria V and Cyclone V devices, and provides a truly out-of-the-box experience for every designer.</li> </ul>

Figure 1-1 shows the hardened data paths in the soft memory IP of a Stratix V device.

**Figure 1-1. Hardened Data Paths in the Soft Memory IP**



## Memory Solutions

Altera FPGAs achieve optimal memory interface performance with external memory IP. The IP provides the following components:

- Physical layer interface (PHY) which handles the timing on the data path itself.
- Memory controller block which implements all the memory commands and addresses.
- Multiport front-end (MPFE) block which allows multiple processes inside the FPGA device to share a common bank of memory. The MPFE block is a new feature in Arria V and Cyclone V devices.

These blocks are critical to the design and the use of the memory interface block.

Altera provides modular memory solutions that allow you to customize your memory interface design to any of the following configurations:

- PHY with your own controller
- PHY with Altera controller
- PHY with Altera controller and the MPFE block

You can also build a custom PHY, a custom controller, or both, as desired.

Table 1–2 shows the recommended memory types and controllers that Altera offers with the PHY IP.

**Table 1–2. Altera Memory Types, PHY, and Controllers in the Quartus II Software (Part 1 of 2)**


Quartus II Version	Memory	PHY IP	Controller IP
11.1	DDR/DDR2/DDR3	ALTMEMPHY (AFI) <sup>(1)</sup>	HPC II
	DDR2/DDR3	UniPHY	HPC II
	QDR II/QDR II+	UniPHY	QDR/RLD II controller
	RLDRAM II	UniPHY	QDR/RLD II controller
	Other	ALTDQ_DQS <sup>(2)</sup>	Custom
	Other	ALTDQ_DQS2 <sup>(3)</sup>	Custom
11.0	DDR/DDR2/DDR3	ALTMEMPHY (AFI)	HPC II
	DDR2/DDR3	UniPHY	HPC II
	QDR II/QDR II+	UniPHY	QDR/RLD II controller
	RLDRAM II	UniPHY	QDR/RLD II controller
	Other	ALTDQ_DQS <sup>(2)</sup>	Custom
	Other	ALTDQ_DQS2 <sup>(3)</sup>	Custom
10.1	DDR/DDR2/DDR3	ALTMEMPHY (AFI)	HPC HPC II
	DDR2/DDR3	UniPHY Nios-based Sequencer	HPC II
	QDR II/QDR II+	UniPHY RTL Sequencer	QDR/RLD II controller
	RLDRAM II	UniPHY RTL Sequencer	QDR/RLD II controller
	Other	ALTDQ_DQS <sup>(2)</sup>	Custom
	Other	ALTDQ_DQS2 <sup>(3)</sup>	Custom
10.0	DDR/DDR2/DDR3	ALTMEMPHY (AFI)	HPC HPC II
	DDR2/DDR3	UniPHY Nios-based Sequencer	HPC II
	QDR II/QDR II+	UniPHY RTL Sequencer	QDR/RLD II controller
	RLDRAM II	UniPHY RTL Sequencer	QDR/RLD II controller
	Other	ALTDQ_DQS <sup>(2)</sup>	Custom
	Other	ALTDQ_DQS2 <sup>(3)</sup>	Custom

**Table 1-2. Altera Memory Types, PHY, and Controllers in the Quartus II Software (Part 2 of 2)**

Quartus II Version	Memory	PHY IP	Controller IP
9.1	DDR/DDR2/DDR3	ALTMEMPHY (AFI)	HPC HPC II
	QDR II/QDR II+	UniPHY	QDR II controller
	RLDRAM II	UniPHY	RLDRAM II controller
	Other	ALTDQ_DQS <sup>(2)</sup>	Custom

**Note to Table 1-2:**

- (1) AFI = Altera PHY interface
- (2) Applicable for Arria II, Stratix III, and Stratix IV devices.
- (3) Applicable only for Arria V and Stratix V devices.

 For more information about the controllers with the UniPHY or the ALTMEMPHY IP, refer to the *Functional Descriptions* section in **Volume 3** of the *External Memory Interface Handbook*.

For more information about the ALTDQ\_DQS megafunction, refer to the *ALTDLL and ALTDQ\_DQS Megafunctions User Guide*.

For more information about the ALTDQ\_DQS2 megafunction, refer to the *ALTDQ\_DQS2 Megafunction User Guide*.

For more information and design example about custom PHY, refer to the [Design Example - Stratix III ALTDQ DQS DDR2 SDRAM](#) page.

## Low Latency

Altera generally offers low latency solutions that are drastically better than Altera's competitors. Altera's 28-nm FPGA devices have a balanced clocked network in the periphery to reduce switching noise. The hardened read data FIFO buffer guarantees timing and makes it easier for the fitter to place the controller. Together with the latest UniPHY IP, these design changes provide drastic reduction in latency.

[Table 1-3](#) shows latency comparison for Altera and its closest competition.

**Table 1-3. Latency Comparison for Quarter-Rate DDR3 SDRAM Controllers**

Latency Type	Latency (Memory Clock Cycles)		Advantage
	Competitor <sup>(1)</sup>	Altera	
Write Command	46	29	Altera
Read Command	46	29	Altera
Read Data	31	11	Altera

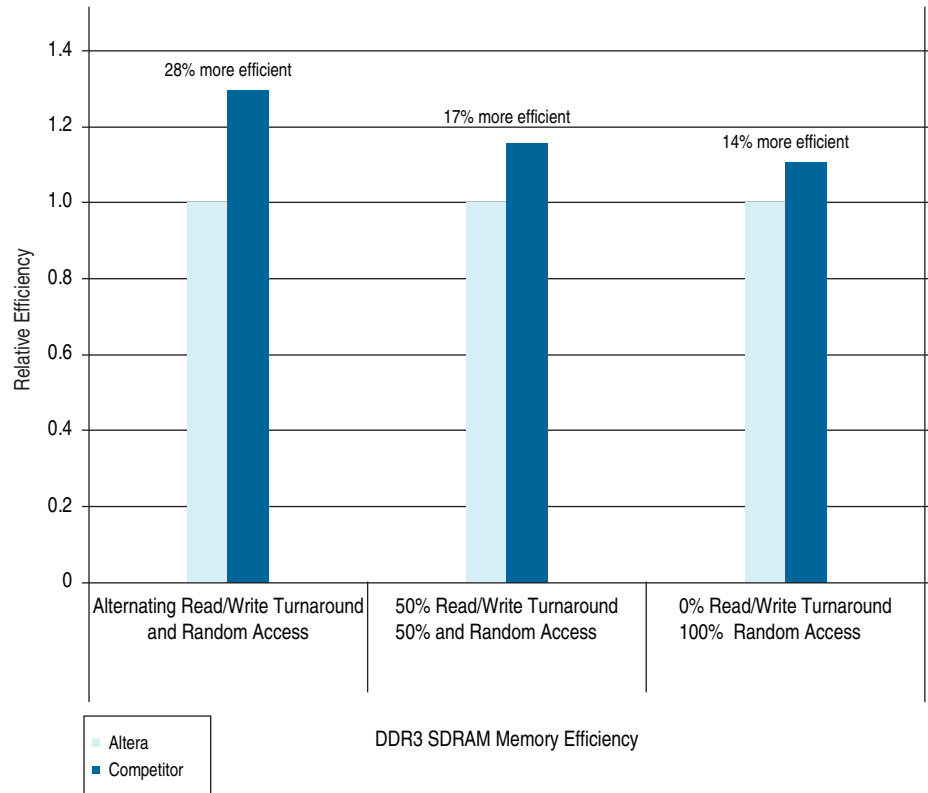
**Note to Table 1-3:**

- (1) Does not include AXI latency.

## Efficiency

Altera memory controllers are also highly efficient. Figure 1-2 shows the memory efficiency of a DDR3 SDRAM memory controller with UniPHY IP.

**Figure 1-2. Memory Efficiency of DDR3 SDRAM Memory Controllers with UniPHY**



## Document Revision History

Table 1-4 shows the revision history for this document.

**Table 1-4. Document Revision History**

Date	Version	Changes
November 2011	1.0	Initial release.