

Introduction

HardCopy® II devices are low-cost, high-performance structured ASICs with pin-outs, densities, and architecture that complement Stratix® II devices. HardCopy II device features, such as phase-locked loops (PLLs), memory, and I/O elements (IOEs), are functionally and electrically equivalent to the Stratix II FPGA features. The combination of Stratix II FPGAs for in-system prototype and design verification, HardCopy II devices for high-volume production, and the Quartus® II software for design, provide a complete, low-risk design solution.

HardCopy II devices improve on the successful and proven methodology of the two previous generations of HardCopy series devices. Altera® HardCopy II devices use the same base arrays across multiple designs for a given device density and are customized using only two metal layers. HardCopy II devices offer up to 90% cost reduction compared to Stratix II FPGA prototypes.

The Quartus II software provides a complete set of tools, common for both designing Stratix II FPGA prototypes and for quickly migrating the design to a HardCopy II companion device. HardCopy II devices are also supported through other front-end design tools from Synopsys, Synplicity, and Mentor Graphics®.

Feature Overview

HardCopy II structured ASICs are manufactured on a 1.2 V, 90 nm all-layer-copper metal fabrication process (up to nine layers of metal). HardCopy II devices offer the following features:

- Fine-grained *HCell* architecture resulting in a low-cost, high-performance, low-power structured ASIC
- Customized using only two metal layers for fast turn-around times and low non-recurring expenses (NRE)
- Fully tested prototypes are available in approximately 10 to 12 weeks from the date of your design submission
- Support for instant-on or instant-on-after-50-ms power-up modes
- Preserves the design functionality of a Stratix II FPGA prototype
- 1,000,000 to 3,600,000 usable gates for both logic and DSP functions

- System performance up to 350 MHz
- Up to 50% power reduction (dynamic and static) for typical designs compared to Stratix II FPGA prototypes



The actual performance and power consumption improvements mentioned in this datasheet are design-dependent.

- Internal Memory
 - Up to 8,847,360 RAM bits available (including parity bits)
 - True dual-port memory, suitable for use in first-in-first-out (FIFO) buffers
- Phase-Locked Loops (PLLs)
 - Up to 16 global clocks with 24 clocking resources per device region
 - Clock control block supports dynamic clock network enable/disable and dynamic global clock network source selection
 - Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device which provide identical features as the FPGA counterparts, including spread spectrum, programmable bandwidth, clock switchover, real-time PLL reconfiguration, advanced multiplication, and phase shifting
- I/O Standards and Intellectual Property (IP)
 - Support for numerous single-ended and differential I/O standards such as LVTTTL, LVCMOS, PCI, PCI-X, SSTL, HSTL, and LVDS
 - High-speed differential I/O support on up to 116 channels with dynamic phase alignment (DPA) circuitry for 1-Gigabit-per-second (Gbps) performance
 - Support for high-speed networking and communications bus standards including Parallel RapidIO, SPI-4 Phase 2 (POS-PHY Level 4), HyperTransport™ technology, and SFI-4
 - Support for high-speed external memory, including DDR and DDR2 SDRAM, RLDRAM II, QDR II SRAM, and SDR SDRAM
 - Support for multiple intellectual property megafunctions from Altera MegaCore® functions, and Altera Megafunction Partners Program (AMPPSM) megafunctions
- Packaging
 - Pin-compatible with Stratix II FPGA prototypes
 - Up to 951 user I/O pins available
 - Available in wire bond and flip-chip space-saving FineLine BGA packages (Table 1-3).

The HardCopy II device family consists of five devices. [Table 1-1](#) summarizes the features available in the HardCopy II devices.

Feature	HC210W (1)	HC210	HC220	HC230	HC240
ASIC equivalent gates (2)	1,000,000	1,000,000	1,900,000	2,900,000	3,600,000
M4K RAM blocks (4 Kbits plus parity)	190	190	408	614	768 (3)
M-RAM blocks (512 Kbits plus parity)	0	0	2	6	9
Total RAM bits (including parity bits)	875,520	875,520	3,059,712	6,368,256	8,847,360
Enhanced PLLs	2	2	2	4	4
Fast PLLs	2	2	2	4	8
Maximum user I/O pins (4), (5)	308	334	494	698	951

Notes to Table 1-1:

- (1) HC210W devices are in a wire bond package. All other HardCopy II devices and Stratix II FPGAs use a flip-chip package. Devices in a wire bond package offer different performance and signal integrity characteristics compared to devices in a flip-chip package.
- (2) This is the number of ASIC equivalent gates available in the HardCopy II base array, shared between both adaptive logic module (ALM) logic and DSP functions from a Stratix II FPGA prototype. Each Stratix II adaptive logic module (ALM) is equal to approximately 30 ASIC equivalent gates. The number of ASIC equivalent gates usable is bounded by the number of ALMs in the companion Stratix II FPGA device.
- (3) Total number of usable M4K blocks is 768, which allows migration compatibility when prototyping with an EP2S180 device. This may be different from the Quartus II software total physical M4K count of the HC240.
- (4) The I/O pin counts include the dedicated CLK input pins, which can be used for clock signals or data inputs.
- (5) The Quartus III I/O pin counts include an additional pin (P_LLENA), which is not available as a general-purpose I/O pin. The P_LLENA pin can only be used to enable the PLLs.

Migration and Packaging Overview

HardCopy II devices offer pin-to-pin compatibility to the Stratix II prototype, which makes them drop-in replacements for the FPGAs. Therefore, the same system board and software developed for prototyping and field trials can be retained, enabling the fastest time-to-market for high-volume production. When migrating a specific Stratix II FPGA to a HardCopy II device, there are a number of FPGA prototype choices, as shown in [Table 1–2](#). Depending on the design resource needs, designers can choose an appropriate HardCopy II device.

Table 1–2. Stratix II FPGA to HardCopy II Migration Paths

HardCopy II Device	Package	Stratix II Device				
		EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
HC210W	484-pin FineLine BGA (1)	✓	✓	✓ (2)		
HC210	484-pin FineLine BGA	✓	✓	✓ (2)		
HC220	672-pin FineLine BGA		✓			
HC220	780-pin FineLine BGA			✓	✓ (2)	
HC230	1,020-pin FineLine BGA			✓	✓	✓ (2)
HC240	1,020-pin FineLine BGA					✓
HC240	1,508-pin FineLine BGA					✓

Notes to Table 1–2:

- (1) The HC210W device uses a wire bond package while the Stratix II FPGA prototype device uses a pin-compatible flip-chip package.
- (2) Depending on design specific resource utilization, an opportunistic migration path may exist between this device pair. Be sure to confirm your design is a potential candidate for such a path by fitting with the Quartus II software and consulting an Altera applications engineer.

HardCopy II devices are available in the packages shown in [Table 1–3](#).

Package	484-Pin FineLine BGA (3)	484-Pin FineLine BGA (3)	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
Type	Wire bond	Flip-chip	Flip-chip	Flip-chip	Flip-chip	Flip-chip
Dimension						
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm ²)	529	529	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	23 × 23	27 × 27	29 × 29	33 × 33	40 × 40
Device	Maximum User I/O Pins					
HC210W	308					
HC210		334				
HC220			492	494		
HC230					698	
HC240					742	951

Notes to Table 1–3:

- (1) The Quartus III I/O pin counts include an additional pin (P_{LENA}) which is not available as a general-purpose I/O pin. The P_{LENA} pin can only be used to enable the PLLs.
- (2) The I/O pin counts include the dedicated CLK input pins, which can be used for clock signals or data inputs.
- (3) The EP2S90 FPGA prototype uses a 484-pin hybrid FineLine BGA package. For more information, refer to the *Stratix II Device Handbook*.

Document Revision History

[Table 1–4](#) shows the revision history for this chapter.

Date and Document Version	Changes Made	Summary of Changes
September 2008, v2.6	Updated chapter number and metadata.	—
June 2007, v2.5	Minor text edits.	—

Table 1–4. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
December 2006 v2.4	<ul style="list-style-type: none"> ● Minor updates for the Quartus II software version 6.1.0 ● Merged Table 1-3 and Table 1-4 ● Added revision history 	A minor update to the chapter, due to changes in the Quartus II software version 6.1 release. Merged Table 1-3 and Table 1-4.
March 2006, v2.3	<ul style="list-style-type: none"> ● Updated Table 1-1 and Table 1-3. ● Minor edits and clarifications throughout. 	
October 2005, v2.2.	Updated graphics	
July 2005, v2.2.	Updated graphics	
May 2005, v2.0	<ul style="list-style-type: none"> ● Updated Table 1–1. ● Updated migration process time. ● Updated “Features” section. 	
January 2005 v1.0	Added document to the HardCopy Series Handbook.	