

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All HardCopy<sup>®</sup> II structured ASICs provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1-1990 specification. The BST architecture offers the capability to efficiently test components on printed circuit boards (PCBs) with tight lead spacing by testing pin connections, without using physical test probes, and capturing functional data while a device is in normal operation. Boundary-scan cells in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results.

A device using the JTAG interface uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. The TCK pin has an internal weak pull-down resistor, while the TDI, TMS, and TRST pins have weak internal pull-up resistors. The TDO output is powered by V<sub>CCIO</sub>. HardCopy II devices support the JTAG instructions shown in [Table 3-1](#).

**Table 3-1. HardCopy II JTAG Instructions (Part 1 of 2)**

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST (1)	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit BYPASS register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.

<b>JTAG Instruction</b>	<b>Instruction Code</b>	<b>Description</b>
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ (1)	00 0000 1011	Places the 1-bit BYPASS register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP (1)	00 0000 1010	Places the 1-bit BYPASS register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.

Note to Table 3–1:

- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.



The BSDL files for HardCopy II devices are different from the corresponding Stratix® II FPGAs. For more information, or to receive BSDL files for IEEE Std. 1149.1- compliant Hardcopy II devices, visit the Altera website at [www.altera.com](http://www.altera.com).

The HardCopy II device instruction register length is 10 bits and the USERCODE register length is 32 bits. The USERCODE registers are not reprogrammable and are mask-programmed. The designer can choose an appropriate 32 bit sequence which will be programmed into the USERCODE registers.

Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for HardCopy II devices.

**Table 3–2. HardCopy II Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
HC210W	1050
HC210	1050
HC220	1530
HC230	2154
HC240	2910

**Table 3–3. 32-Bit HardCopy II Device IDCODE**

Device	IDCODE (32 Bits) (1)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) (2)
HC210W	0000	0010 0000 1100 0001	000 0110 1110	1
HC210	0000	0010 0000 1100 0010	000 0110 1110	1
HC220	0000	0010 0000 1100 0011	000 0110 1110	1
HC230	0000	0010 0000 1100 0100	000 0110 1110	1
HC240	0000	0010 0000 1100 0101	000 0110 1110	1

Notes to Table 3–3:

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) of IDCODE is always 1.

## Boundary-Scan Test (BST) on HardCopy II Devices

In order to run the boundary-scan test on HardCopy II devices, you need two files:

1. The generic HardCopy II BSDL file you can download from the Altera website at [www.altera.com](http://www.altera.com).
2. The PIN file for your design from the Quartus II software.

With these two files, you must run through a tool called the BSDLCustomizer.

BSDLCustomizer is a TCL script which is used to modify the BSDL file's port definitions and boundary-scan chain groups' attributes according to the design and pin assignments from the Quartus II software PIN file.

Once you run the generic BSDL file and your PIN file through the BSDLCustomizer tool, a modified BSDL file is created which should be used for the boundary-scan test.

Before running the boundary scan test on your board make sure that the nCONFIG pin is externally pulled low and that the nSTATUS pin is low.

For more information on the BSDLCustomizer tool, refer to the *BSDLCustomizer User Guide* that you can download with the BSDLCustomizer tool from the Altera website at [www.altera.com](http://www.altera.com).

Figure 3–1 shows the timing requirements for the JTAG signals.

**Figure 3–1. HardCopy II JTAG Waveforms**

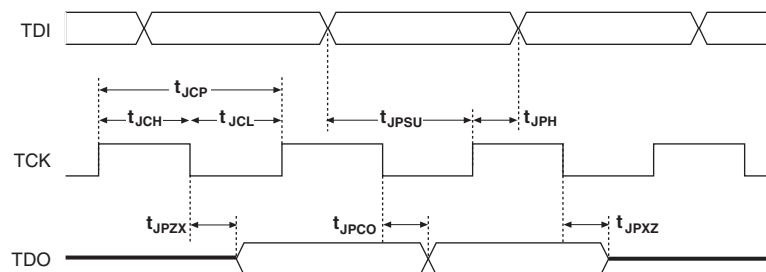


Table 3–4 shows the JTAG timing parameters and values for HardCopy II devices.

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	30		ns
$t_{JCH}$	TCK clock high time	13		ns
$t_{JCL}$	TCK clock low time	13		ns
$t_{JPSU}$	JTAG port setup time	3		ns

**Table 3–4. HardCopy II JTAG Timing Parameters and Values (Part 2 of 2)**

Symbol	Parameter	Min	Max	Unit
$t_{JPH}$	JTAG port hold time	5		ns
$t_{JPCO}$	JTAG port clock to output		11	ns
$t_{JPZX}$	JTAG port high impedance to valid output		14	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		14	ns
$t_{JSSU}$	Capture register setup time	4		ns
$t_{JSH}$	Capture register hold time	5		ns



For more information on JTAG or boundary-scan testing, refer to AN 39: *IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*.



Like Stratix II FPGAs, HardCopy II devices support the SignalTap® II embedded logic analyzer, which monitors design operation over a period of time through the JTAG interface. The SignalTap II logic analyzer is a useful feature during the FPGA prototyping phase, but should be removed if not needed once the design has been migrated to a HardCopy II device. HardCopy II is a mask programmed device, and the Signal Tap logic cannot be eliminated after the HardCopy II device is fabricated.

## Document Revision History

Table 3–5 shows the revision history for this chapter.

**Table 3–5. Document Revision History (Part 1 of 2)**

Date and Document Version	Changes Made	Summary of Changes
September 2008, v2.4	Updated chapter number and metadata.	—
June 2007, v2.3	<ul style="list-style-type: none"> <li>Added resource information</li> <li>Figure 3–1 changes</li> <li>New section on Boundary-Scan Test (BST) on HardCopy II devices.</li> </ul>	—
December 2006 v2.2	<ul style="list-style-type: none"> <li>Minor updates for Quartus II 6.1.0 software version</li> <li>Added revision history</li> </ul>	Updated for Quartus II 6.1 software version.
October 2005, v2.1	Updated graphics.	—

**Table 3–5. Document Revision History (Part 2 of 2)**

<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
May 2005, v2.0	Updated Table 3-2.	—
January 2005 v1.0	Added document to the HardCopy Series Handbook.	—