Section I. HardCopy III Device Datasheet

This section provides the datasheet for the HardCopy® III device family. This section includes the following chapter:

- Chapter 1, DC and Switching Characteristics of HardCopy III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

1. DC and Switching Characteristics of HardCopy III Devices

HIII52001-4.0

Electrical Characteristics

This chapter provides information about the absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for HardCopy® III devices. Altera offers HardCopy III devices in commercial and industrial grades.

Operating Conditions

When implementing HardCopy III devices in a system, the system rates the devices according to a set of defined parameters. To maintain the highest performance and reliability, you must consider the operating requirements described in this chapter. HardCopy III devices are not speed binned because HardCopy III devices function at a target frequency based on timing constraints, and operate at either commercial or industrial temperatures.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for HardCopy III devices. Experiments with the device and theoretical modeling of breakdown and damage mechanisms provide these values.

Table 1–1 lists the absolute maximum ratings for a HardCopy III device.

Conditions beyond those listed in Table 1–1 can cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time can have adverse effects on the device.

Table 1–1. HardCopy III Device Absolute Maximum Ratings – Preliminary (Part 1 of 2) *(Note 1)*

Symbol	Parameter	Minimum	Maximum	Unit
V_{CCL}	Core voltage power supply	–0.5	1.35	V
V_{CC}	I/O registers power supply	–0.5	1.35	V
V_{CCD_PLL}	PLL digital power supply	–0.5	1.35	V
V_{CCA_PLL}	PLL analog power supply	–0.5	3.75	V
V_{CCPT} *(2)*	Power supply for the temperature sensing diode	–0.5	3.75	V
V_{CCPGM}	Configuration pins power supply	–0.5	3.9	V
V_{CCPD}	I/O predriver power supply	–0.5	3.9	V
V_{CCIO}	I/O power supply	–0.5	3.9	V
V_{CC_CLKIN}	Differential clock input power supply (top and bottom I/O banks only)	–0.5	3.75	V

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Table 1–1. HardCopy III Device Absolute Maximum Ratings – Preliminary (Part 2 of 2) *(Note 1)*

Symbol	Parameter	Minimum	Maximum	Unit
V_{CCBAT} *(3)*	Battery back-up power supply for design security volatile key register	—	—	V
V_I	DC input voltage	–0.5	4.0	V
T_J	Operating junction temperature	–55	125	°C
I_{OUT}	DC output current, per pin	–25	40	mA
T_{STG}	Storage temperature (no bias)	–65	150	°C

Notes to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins and not the power supply.
(2) Stratix III devices use this power supply for programmable power technology.
(3) HardCopy III devices do not use this power supply.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

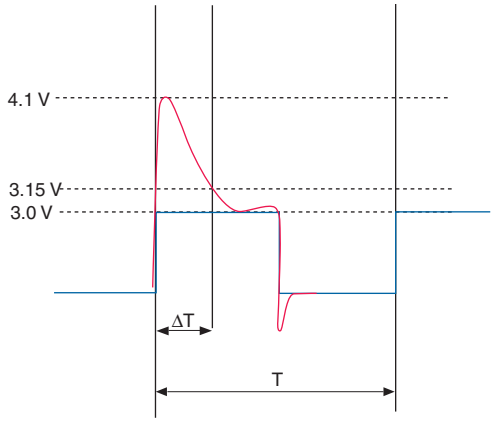
Table 1–2 lists the maximum allowed input overshoot voltage. The maximum allowed overshoot duration is the percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

Table 1–2. Maximum Allowed Overshoot During Transitions – Preliminary

Symbol	Parameter	Condition	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC Input Voltage	4	100.000	%
		4.05	79.330	%
		4.1	46.270	%
		4.15	27.030	%
		4.2	15.800	%
		4.25	9.240	%
		4.3	5.410	%
		4.35	3.160	%
		4.4	1.850	%
		4.45	1.080	%
		4.5	0.630	%
		4.55	0.370	%
		4.6	0.220	%
		4.65	0.130	%
		4.7	0.074	%
		4.75	0.043	%
		4.8	0.025	%
		4.85	0.015	%

Figure 1–1 shows the methodology to determine the overshoot duration. The color red indicates the overshoot voltage and is present at the HardCopy III pin, up to 4.1 V. From Table 1–2, for an overshoot of up to 4.1 V, the percentage of high time for overshoot is greater than 3.15 V can be as high as 46% over an 11.4 year period. (delta T/T) × 100 is the calculation for the percentage of high-time. This 11.4 year period assumes that you turned on the device with 100% I/O toggle rate and 50% duty cycle signal. Lifetimes increase for lower I/O toggle rates and situations in which the device is in an idle state.

Figure 1–1. Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for HardCopy III devices. Table 1–3 lists the steady-state voltage and current values expected from HardCopy III devices. All supplies must reach their full-rail values in t_{RAMP} maximum monotonically. Table 1–3 also lists the minimum and maximum specifications. These specifications bound allowed ripple on power supplies.

Table 1–3. HardCopy III Device Recommended Operating Conditions – Preliminary (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCL} *(1)*	Core voltage power supply for internal logic and input buffers	—	0.87	0.9	0.93	V
V_{CC} *(1)*	I/O registers power supply	—	0.87	0.9	0.93	V
V_{CCD_PLL} *(1)*	PLL digital power supply	—	0.87	0.9	0.93	V
V_{CCA_PLL}	PLL analog power supply	—	2.375	2.5	2.625	V
V_{CCPT} *(2)*	Power supply for the temperature sensing diode	—	2.375	2.5	2.625	V
V_{CCPGM}	Configuration pins power supply, 3.0 V	—	2.85	3.0	3.15	V
	Configuration pins power supply, 2.5 V	—	2.375	2.5	2.625	V
	Configuration pins power supply, 1.8 V	—	1.71	1.8	1.89	V
V_{CCPD} *(3)*	I/O predriver power supply, 3.0 V	—	2.85	3.0	3.15	V
	I/O predriver power supply, 2.5 V	—	2.375	2.5	2.625	V

Table 1–3. HardCopy III Device Recommended Operating Conditions – Preliminary (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O power supply, 3.0 V	—	2.85	3.0	3.15	V
	I/O power supply, 2.5 V	—	2.375	2.5	2.625	V
	I/O power supply, 1.8 V	—	1.71	1.8	1.89	V
	I/O power supply, 1.5 V	—	1.425	1.5	1.575	V
	I/O power supply, 1.2 V	—	1.14	1.2	1.26	V
V_{CC_CLKIN}	Differential clock input power supply (1.2V)	—	1.075	1.2	1.325	V
		—	1.375	1.5	1.625	V
		—	1.675	1.8	1.925	V
		—	2.375	2.5	2.625	V
		—	2.875	3.0	3.125	V
V_{CCBAT} *(4)*	Battery back-up power supply for design security volatile key register	—	—	—	—	V
V_I	DC input voltage	—	–0.3	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Normal POR (PORSEL=0)	50 µs	—	100	ms
		Fast POR (PORSEL=1)	50 µs	—	4	ms

Notes to Table 1–3:

(1) In Stratix III devices, V_{CCL} can also be 1.1 V, while V_{CC} and V_{CCD_PLL} are 1.1 V. In HardCopy III devices, all three supplies are 0.9 V.
(2) Stratix III devices use this power supply for programmable power technology.
(3) V_{CCPD} is either 2.5 V or 3.0 V. For a 3.0-V I/O standard, V_{CCPD} = 3.0 V. For a 2.5 V or lower I/O standard, V_{CCPD} = 2.5 V.
(4) HardCopy III devices do not use this power supply.

DC Characteristics

This section lists the input pin capacitances, on-chip termination (OCT) tolerance, and hot socketing specifications.

Supply Current

Standby current is the current the device draws after the device enters user mode with no inputs or outputs toggling and no activity in the device. Because these currents vary largely with the resources used, use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

Table 1–4 lists supply current specifications for V_{CC_CLKIN} and V_{CCPGM}. Use the EPE to get supply current estimates for the remaining power supplies.

Table 1–4. Supply Current Specifications for V_{CC_CLKIN} and V_{CCPGM} – Preliminary *(Note 1)*

Symbol	Parameter	Min	Max	Unit
I_{CLKIN}	V_{CC_CLKIN} current specifications	0	TBD	mA
I_{PGM}	V_{CCPGM} current specifications	0	TBD	mA

Note to Table 1–4:

(1) Pending silicon characterization.

I/O Pin Leakage Current

Table 1–5 lists HardCopy III I/O pin leakage current specifications.

Table 1–5. HardCopy III I/O Pin Leakage Current – Preliminary *(Note 1)*, *(2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOMAX}$ to 0 V	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOMAX}$ to 0 V	–10	—	10	µA

Notes To Table 1–5:

(1) This value is for normal device operation. The value may vary during power up. This applies for all V_{CCIO} settings (3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10 mA I/O leakage current limit is applicable when the internal clamping diode is off. You can observe a higher current when the diode is on.

OCT Specifications

If you enabled OCT calibration, calibration is automatically performed at power up for I/Os connected to the calibration block. Table 1–6 lists the HardCopy III OCT calibration block accuracy specifications.

Table 1–6. HardCopy III OCT Calibration Accuracy Specifications – Preliminary (Part 1 of 2) *(Note 1)*

Symbol	Description	Conditions	Calibration Accuracy		Unit
			Commercial *(2)*	Industrial	
25–Ω R_S 3.0/2.5	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0/2.5 V	TBD	—	%
50–Ω R_S 3.0/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0/2.5 V	TBD	—	%
50–Ω R_T 2.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5 V	TBD	—	%
25–Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8 V	TBD	—	%
50–Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	TBD	—	%
50–Ω R_T 1.8	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	TBD	—	%
50–Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	TBD	—	%

Table 1–6. HardCopy III OCT Calibration Accuracy Specifications – Preliminary (Part 2 of 2) *(Note 1)*

Symbol	Description	Conditions	Calibration Accuracy		Unit
			Commercial *(2)*	Industrial	
50–Ω R_T 1.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	TBD	—	%
50–Ω R_S 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	TBD	—	%
50–Ω R_T 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	TBD	—	%

Notes to Table 1–6:

(1) OCT calibration accuracy is valid at the time of calibration only.

(2) Pending silicon characterization.

The accuracy listed in Table 1–6 is valid at the time of calibration. If the voltage or temperature changes, the termination resistance value varies. Table 1–7 lists the resistance tolerance for HardCopy III on-chip termination.

Table 1–7. OCT Resistance Tolerance Specification for I/Os – Preliminary *(Note 1)*

Symbol	Description	Resistance Tolerance		Unit
		Commercial Max	Industrial Max	
R_{OCT_UNCAL}	Internal series termination without calibration	TBD	—	%
R_{OCT_CAL}	Internal series termination with calibration	*(2)*	—	%

Notes to Table 1–7:

(1) Pending silicon characterization.

(2) For resistance tolerance after power-up calibration, refer to Table 1–8.

Table 1–8 lists OCT variation with temperature and voltage after power-up calibration.

The R_{CAL} is calibrated OCT at power-up. ΔT and ΔV are variations in temperature and voltage (V_{CCIO}) at power-up.

Table 1–8. OCT Variation after Power-up Calibration – Preliminary (Part 1 of 2) *(Note 1)*, *(2)*

Symbol	Description	V_{CCIO} (V)	Commercial Typical	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	TBD	%/mV
		2.5	TBD	%/mV
		1.8	TBD	%/mV
		1.5	TBD	%/mV
		1.2	TBD	%/mV

Table 1–8. OCT Variation after Power-up Calibration – Preliminary (Part 2 of 2) ***(Note 1), (2)***

Symbol	Description	V_{CCIO} (V)	Commercial Typical	Unit
dR/dT	OCT variation with temperature without recalibration	3.0	TBD	%/°C
		2.5	TBD	%/°C
		1.8	TBD	%/°C
		1.5	TBD	%/°C
		1.2	TBD	%/°C

Notes to Table 1–8:

(1) Valid for V_{CCIO} range of ± 5% and temperature range of 0° to 85° C.

(2) Pending silicon characterization.

To determine OCT variation without recalibration, use Table 1–8 and Equation 1–1.

Equation 1–1.

$$R_{OCT} = R_{CAL}\left(1 + \frac{dR}{dT} \times \Delta T + \frac{dR}{dV} \times \Delta V\right)$$

Pin Capacitance

Table 1–9 lists the HardCopy III device family pin capacitance.

Table 1–9. HardCopy III Device Capacitance – Preliminary ***(Note 1)***

Symbol	Parameter	Typical	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	TBD	pF
C_{IOLR}	Input capacitance on left and right I/O pins	TBD	pF
C_{CLKTB}	Input capacitance on top and bottom dedicated clock input pins	TBD	pF
C_{CLKLR}	Input capacitance on left and right dedicated clock input pins	TBD	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	TBD	pF
C_{CLK1}, C_{CLK3}, C_{CLK8}, and C_{CLK10}	Input capacitance for dedicated clock input pins	TBD	pF

Note to Table 1–9:

(1) Pending silicon characterization.

Hot Socketing

Table 1–10 lists the hot socketing specifications for HardCopy III devices.

Table 1–10. HardCopy III Hot Socketing Specifications – Preliminary ***(Note 1)***

Symbol	Parameter	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA for t_{RISE} > 10 ns

Note to Table 1–10:

(1) Pending silicon characterization.

Internal Weak Pull-Up Resistor

Table 1–11 lists the weak pull-up resistor values for HardCopy III devices.

Table 1–11. HardCopy III Internal Weak Pull-Up Resistor – Preliminary *(Note 1)*, *(2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Value of I/O pin pull-up resistor before and during user mode, if you enabled the pull-up resistor option	V_{CCIO} = 3.0 V ± 5% *(3)*	—	25	—	kΩ
		V_{CCIO} = 2.5 V ± 5% *(3)*	—	25	—	kΩ
		V_{CCIO} = 1.8 V ± 5% *(3)*	—	25	—	kΩ
		V_{CCIO} = 1.5 V ± 5% *(3)*	—	25	—	kΩ
		V_{CCIO} = 1.2 V ± 5% *(3)*	—	25	—	kΩ

Notes to Table 1–11:

(1) Pending silicon characterization.

(2) All I/O pins have an option to enable weak pull-up except test and JTAG pins.

(3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Table 1–12 through Table 1–17 list input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for all I/O standards supported by HardCopy III devices. For an explanation of terms used in Table 1–12 through Table 1–17, refer to Table 1–31 on page 1–21. V_{OL} and V_{OH} values are valid at the corresponding I_{OL} and I_{OH}, respectively.

Table 1–12. Single-Ended I/O Standards Specifications — Preliminary

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V **LVTTL**	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V **LVCMOS**	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5-V **LVTTL/ LVCMOS**	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.2	2.1	0.1	–0.1
		2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
		2.5	2.625	–0.3	0.7	1.7	3.6	0.7	1.7	2	–2
1.8-V **LVTTL/ LVCMOS**	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5-V **LVTTL/ LVCMOS**	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2-V **LVTTL/ LVCMOS**	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
3.0-V **PCI**	2.85	3	3.15	—	0.3 × V_{CCIO}	0.5 × V_{CCIO}	3.6	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5
3.0-V **PCI-X**	2.85	3	3.15	—	0.35 × V_{CCIO}	0.5 × V_{CCIO}	—	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5

For an example of a voltage referenced receiver input waveform and an explanation of terms used in Table 1–13, refer to Figure 1–6 on page 1–23.

Table 1–13. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications – Preliminary

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 CLASS I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 CLASS I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 CLASS I, II	1.425	1.5	1.575	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	0.47 × V_{CCIO}	V_{REF}	0.53 × V_{CCIO}
HSTL-18 CLASS I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 CLASS I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 CLASS I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—

Table 1–14. Single-Ended SSTL and HSTL I/O Standards Signal Specifications – Preliminary

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 CLASS I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	VTT – 0.57	VTT + 0.57	8.1	–8.1
SSTL-2 CLASS II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	VTT – 0.76	VTT + 0.76	16.2	–16.2
SSTL-18 CLASS I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	VTT – 0.475	VTT + 0.475	6.7	–6.7
SSTL-18 CLASS II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 CLASS I	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 CLASS II	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
HSTL-18 CLASS I	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 CLASS II	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 CLASS I	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 CLASS II	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 CLASS I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 CLASS II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16

For receiver input and transmitter output waveforms, and for all differential I/O standards (**LVDS**, **mini-LVDS**, **RSDS**), refer to Figure 1–2 on page 1–21. V_{CC_CLKIN} is the power supply for differential column clock input pins. V_{CCPD} is the power supply for row I/Os and all other column I/Os.

Table 1–15. Differential SSTL I/O Standard Specifications – Preliminary

I/O Standard	V_{CCIO} (V)			$V_{SWING\ (DC)}$ (V)		$V_{X\ (AC)}$ (V)			$V_{SWING\ (AC)}$ (V)		$V_{OX\ (AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 CLASS I, CLASS II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.2	—	V_{CCIO}/2 + 0.2	0.6	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.15	—	V_{CCIO}/2 + 0.15
SSTL-18 CLASS I, CLASS II	1.71	1.8	1.89	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.125	—	V_{CCIO}/2 + 0.125
SSTL-15 CLASS I, CLASS II	1.425	1.5	1.575	0.2	—	—	V_{CCIO}/2	—	0.4	—	—	V_{CCIO}/2	—

Table 1–16. Differential HSTL I/O Standards Specifications – Preliminary

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 CLASS I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 CLASS I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 CLASS I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.3	V_{CCIO} + 0.48

Table 1–17. Differential I/O Standard Specifications – Preliminary (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(1)*			V_{OCM} (V) *(1)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
2.5-V **LVDS** (Row I/O)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.05 *(2)*	*Dmax* ≤ 700 Mbps	1.8 *(2)*	0.247	—	0.6	1.125	1.25	1.375
	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	1.05 *(2)*	*Dmax* > 700 Mbps	1.55 *(2)*	—	—	—	—	—	—
2.5-V **LVDS** (Column I/O)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.05 *(2)*	*Dmax* ≤ 700 Mbps	1.8 *(2)*	0.247	—	0.6	1.0	1.25	1.5
	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	1.05 *(2)*	*Dmax* > 700 Mbps	1.55 *(2)*	—	—	—	—	—	1.5
RSDS (Row I/O)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (Column I/O)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (Row I/O)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.4
Mini-LVDS (Column I/O)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.5

Table 1–17. Differential I/O Standard Specifications – Preliminary (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(1)*			V_{OCM} (V) *(1)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL *(3)*	2.375 *(4)*	2.5 *(4)*	2.625 *(4)*	300	—	—	0.6	*Dmax* ≤ 700 Mbps	1.8 *(5)*	—	—	—	—	—	—
	—	—	—	—	—	—	0.6	*Dmax* ≤ 700 Mbps	1.6 *(5)*	—	—	—	—	—	—

Notes to Table 1–17:

(1) R_L range: 90 ≤ R_L ≤ 110 Ω.

(2) For data rate: D_{max} > 700 Mbps, the minimum input voltage is 1.0 V, the maximum input voltage is 1.6 V. For D_{max} ≤ 700 Mbps, the minimum input voltage is 0 V, the maximum input voltage is 1.85 V.

(3) Column and Row I/O banks support **LVPECL** I/O standards for input operation only on dedicated clock input pins. Differential clock inputs in column I/O use V_{CC_CLKIN}, which should be powered by 2.5 V. V_{CCPD} powers differential clock inputs in row I/Os.

(4) Power supply for column I/O **LVPECL** differential clock input buffer is V_{CC_CLKIN}.

(5) For data rate D_{max} > 700 Mbps, the minimum input voltage is 0.85 V, and the maximum input voltage is 1.75 V. For data rate D_{max} ≤ 700 Mbps, the minimum input voltage is 0.45 V, and the maximum input voltage is 1.95 V.

Power Consumption

Altera offers the Excel-based EPE and the Quartus® II PowerPlay Power Analyzer feature to estimate power for your design.

Use the interactive Excel-based EPE before designing the HardCopy device to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of your design after the placement and routing is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

For supply current estimates for V_{CCPGM} and V_{CC_CLKIN}, refer Table 1–4 on page 1–5. Use the EPE and PowerPlay Power Analyzer for current estimates of the remaining power supplies.

For more information about power estimation tools, refer to the *Power Play Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Device Handbook*.

Switching Characteristics

This section provides performance characteristics of HardCopy III core and periphery blocks for commercial grade devices. HardCopy III devices can meet, at minimum, the –3 speed grade of the Stratix III devices. Silicon characterization determines the actual performance of the HardCopy III devices. The following items define the characteristics:

- **Preliminary**—Created using simulation results, process data, and other known parameters.
- **Final**—Based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

Core Performance Specifications

This sections describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), TriMatrix, configuration, and JTAG specifications.

Clock Tree Specifications

Table 1–18 lists clock tree performance specifications for the logic array, DSP blocks, and TriMatrix Memory blocks for HardCopy III devices.

Table 1–18. HardCopy III Clock Tree Performance – Preliminary ***(Note 1)***

Device	Commercial Grade (MHz)	Unit
HC325	600	MHz
HC335	600	MHz

Note to Table 1–18:

(1) Pending silicon characterization.

PLL Specifications

Table 1–19 lists the HardCopy III PLL specifications when operating in both the commercial junction temperature range (0° to 85° C) and the industrial junction temperature range (–40° to 100°C). For a PLL block diagram, refer to Figure 1–4 on page 1–22.

Table 1–19. HardCopy III PLL Specifications – Preliminary (Part 1 of 2) ***(Note 1)***

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	5	—	717 *(2)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating range	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	—	—	600 *(3)*	MHz
f_{OUT_EXT}	Output frequency for external clock output	—	—	717 *(3)*	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chain	—	—	—	scanclk cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	—	—	scanclk cycles
$f_{SCANCLK}$	`scanclk` frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device power up *(4)*	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth *(5)*	—	4	—	MHz

Table 1–19. HardCopy III PLL Specifications – Preliminary (Part 2 of 2) ***(Note 1)***

Symbol	Parameter	Min	Typ	Max	Unit
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on *areset* signal	10	—	—	ns
t_{INCCJ} *(4)*	Input clock cycle-to-cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p–p)
	Input clock cycle-to-cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p–p)
t_{OUTPJ_DC} *(6)*	Period jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p–p)
	Period jitter for dedicate clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p–p)
t_{OUTCCJ_DC} *(6)*	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p–p)
	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p–p)
t_{OUTPJ_IO} *(6)*	Period jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p–p)
	Period jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p–p)
t_{OUTCCJ_IO} *(6)*	Cycle-to-cycle jitter for clock output on regular I/O ($F_{OUT} \geq$ 100 MHz)	—	—	600	ps (p–p)
	Cycle-to-cycle jitter for clock output on regular I/O ($F_{OUT} <$ 100 MHz)	—	—	60	mUI (p–p)
f_{DRIFT}	Frequency drift after disabling `PFDENA` for duration of 100 ms	—	—	±10	%

Notes to Table 1–19:

(1) Pending silicon characterization.

(2) The I/O maximum frequency limits this specification in the Quartus II software. The maximum I/O frequency is different for each I/O standard.

(3) The lower of the two: I/O f_{MAX} or f_{OUT} of the PLL limits this specification.

(4) A high input jitter directly affects the PLL output jitter. You must provide a clean clock source, which is less than 200 ps, to have low PLL output clock jitter.

(5) External feedback mode does not support high bandwidth PLL settings.

(6) Peak-to-peak jitter with a probability level of 10^{-12}(14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when you apply an input jitter of 30 ps.

DSP Block Specifications

Table 1–20 lists the HardCopy III DSP performance specifications.

Table 1–20. HardCopy III DSP Block Performance Specifications – Preliminary (Part 1 of 2) ***(Note 1)***, ***(2)***

Mode	Number of Multipliers	Max	Unit
9 × 9-bit multiplier (a, c, e, g) *(3)*	1	365	MHz
9 × 9-bit multiplier (b, d, f, h) *(3)*	1	410	MHz
12 × 12-bit multiplier (a, e) *(4)*	1	365	MHz
12 × 12-bit multiplier (b, d, f, h) *(4)*	1	410	MHz
18 × 18-bit multiplier	1	495	MHz
36 × 36-bit multiplier	1	365	MHz
Double mode	1	365	MHz
18 × 18-bit multiply adder	2	405	MHz
18 × 18-bit multiply adder	4	405	MHz
18 × 18-bit multiply adder with loop back *(5)*	2	405	MHz
18 × 18-bit multiply accumulator	4	390	MHz
18 × 18-bit multiply adder with chainout	4	390	MHz

Table 1–20. HardCopy III DSP Block Performance Specifications – Preliminary (Part 2 of 2) *(Note 1), (2)*

Mode	Number of Multipliers	Max	Unit
Input Cascade Independent output of 4 18 × 18 bit multiplier	4	455	MHz
36-bit shift (32-bit data)	1	390	MHz

Notes to Table 1–20:

(1) Maximum is for fully pipelined block with **round** and **saturation** disabled.

(2) Pending silicon characterization.

(3) The DSP block implements eight independent 9 × 9-bit multipliers using a, b, c, and d for the top half of the DSP block and e, f, g, and h for the bottom DSP half block multipliers.

(4) The DSP block implements six independent 12 × 12-bit multipliers using a, b, and d for the top half of the DSP half block and e, f, and h for the bottom DSP half block multipliers.

(5) Maximum for non-pipelined block with loopback input registers disabled with **round** and **saturation** disabled.

TriMatrix Memory Block Specifications

Table 1–21 lists the HardCopy III TriMatrix memory block specifications.

Table 1–21. HardCopy III TriMatrix Memory Block Performance Specifications – Preliminary (Part 1 of 3) *(Note 1)*

Memory	Mode	TriMatrix Memory	Performance (Flipchip Package)		Performance (Wirebond Package)		Unit
			Commercial Speed Grade	Industrial Speed Grade	Commercial Speed Grade	Industrial Speed Grade	
MLAB	Single port 16 × 10	1	500	500	375	375	MHz
	Simple dual-port 16 × 20	1	500	500	375	375	MHz
	ROM 64 × 10	1	500	500	375	375	MHz
	ROM 32 × 20	1	500	500	375	375	MHz
M9K	Single-port 8K × 1	1	540	540	378	378	MHz
	Single-port 4K × 2 or 2K × 4	1	540	540	378	378	MHz
	Single-port 1K × 9, 512 × 18, or 256 × 36	1	540	540	378	378	MHz
	Simple dual-port, 8K × 1	1	490	490	343	343	MHz
	Simple dual-port, 4K × 2 or 2K × 4	1	490	490	343	343	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36	1	490	490	343	343	MHz
	Simple dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to “Old Data”	1	340	340	238	238	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36 with the read-during-write option set to “Old Data”	1	340	340	238	238	MHz
	True dual-port, 8K × 1	1	430	430	301	301	MHz

Table 1–21. HardCopy III TriMatrix Memory Block Performance Specifications – Preliminary (Part 2 of 3) ***(Note 1)***

Memory	Mode	TriMatrix Memory	Performance (Flipchip Package)		Performance (Wirebond Package)		Unit
			Commercial Speed Grade	Industrial Speed Grade	Commercial Speed Grade	Industrial Speed Grade	
M9K	True dual-port, 4K × 2 or 2K × 4	1	430	430	301	301	MHz
	True dual-port, 1K × 9 or 512 × 18	1	430	430	301	301	MHz
	True dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to “Old Data”	1	335	335	235	235	MHz
	True dual-port, 1K × 9 or 512 × 18 with the read-during-write option set to “Old Data”	1	335	335	235	235	MHz
	ROM 1P, 8K × 1, 4K × 2, or 2K × 4	1	540	540	378	378	MHz
	ROM 1P, 1K × 9, 512 × 18, or 256 × 36	1	540	540	378	378	MHz
	ROM 2P, 8K × 1, 4K × 2, or 2K × 4	1	540	540	378	378	MHz
	ROM 2P, 1K × 9, or 512 × 18	1	540	540	378	378	MHz
	Min Pulse Width (Clock High Time)	—	800	800	1067	1067	ps
	Min Pulse Width (Clock Low Time)	—	625	625	469	469	ps
M144K	True dual-port 16K × 9 or 8K × 18	1	375	350	263	245	MHz
	True dual-port 4K × 36	1	375	350	263	245	MHz
	Simple dual-port 16K × 9 or 8K × 18	1	435	375	305	263	MHz
	Simple dual-port 4K × 36 or 2K × 72	1	435	375	305	263	MHz
	ROM 1 Port	1	500	450	350	315	MHz
	ROM 2 Port	1	465	425	326	298	MHz
	Single-port 16K × 9 or 8K × 18	1	440	400	308	280	MHz
	Single-port 4K × 36	1	440	400	308	280	MHz
	True dual-port 16K × 9, 8K × 18, or 4K × 36 with the read-during-write option set to “Old Data”	1	230	225	161	158	MHz

Table 1–21. HardCopy III TriMatrix Memory Block Performance Specifications – Preliminary (Part 3 of 3) *(Note 1)*

Memory	Mode	TriMatrix Memory	Performance (Flipchip Package)		Performance (Wirebond Package)		Unit
			Commercial Speed Grade	Industrial Speed Grade	Commercial Speed Grade	Industrial Speed Grade	
M144K	Simple dual-port 16K × 9, 8K × 18, 4K × 36, or 2K × 72 with the read-during-write option set to "Old Data"	1	240	225	168	156	MHz
	Simple dual-port 2K × 64 (with ECC)	1	300	295	210	207	MHz
	Min Pulse Width (Clock High Time)	—	1382	1382	1843	1843	ps
	Min Pulse Width (Clock Low Time)	—	625	690	833	920	ps

Note to Table 1–21:

(1) Pending silicon characterization.

JTAG Specifications

Table 1–22 lists the JTAG timing parameters and values for HardCopy III devices. For JTAG timing requirements, refer to Figure 1–3 on page 1–22.

Table 1–22. HardCopy III JTAG Timing Parameters and Values – Preliminary

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
t_{JPSU} (TDI)	JTAG port setup time for TDI	1	—	ns
t_{JPSU} (TMS)	JTAG port setup time for TMS	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Periphery Performance

This section describes the periphery performance, including high-speed I/O, external memory interface, and OCT calibration block specifications.

High-Speed I/O Specifications

For definitions of high-speed timing specifications, refer to Table 1–31 on page 1–21.

Table 1–23 lists the high-speed I/O timing for HardCopy III devices.

Table 1–23. High-Speed I/O Specifications—Preliminary (Part 1 of 2) ***(Note 1), (2), (3)***

Symbol	Conditions	Flipchip			Wirebond		
		Min	Typ	Max	Min	Typ	Max
Transmitter							
Dedicated LVDS—f_{HSDR} (data rate)	SERDES factor J = 3 to 10	150	—	1250	150	—	840
	SERDES factor J = 2, uses DDR registers	*(5)*	—	1250	*(5)*	—	840
	SERDES factor J = 1, uses SDR register	*(5)*	—	717	*(5)*	—	450
LVDS_E_3R—$f_{HSDRDPA}$ (data rate)	SERDES factor J =4 to 10	*(5)*	—	1000	*(5)*	—	640
LVDS_E_1R—$f_{HSDRDPA}$ (data rate)		*(5)*	—	200	*(5)*	—	170
t_x Jitter	Total Jitter for data rate, 600 Mbps - 1.6G bps	—	—	160	—	—	160
	Total Jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1
t_{DUTY}	Tx output clock duty cycle	45	50	55	45	50	55
t_{RISE} and t_{FALL}	Dedicated LVDS	—	—	200	—	200	—
	LVDS_E_3R	—	—	350	—	350	—
	LVDS_E_1R	—	—	500	—	500	—
TCCS	Dedicated LVDS	—	—	100	—	—	200
	LVDS_E_3R/ LVDS_E_1R	—	—	250	—	—	250
Receiver							
$f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10	150	—	1250	150	—	840
DPA Mode							
DPA run length	—	—	—	10000	—	—	10000

Table 1–23. High-Speed I/O Specifications—Preliminary (Part 2 of 2) ***(Note 1), (2), (3)***

Symbol	Conditions	Flipchip			Wirebond		
		Min	Typ	Max	Min	Typ	Max
Soft CDR mode							
Soft-CDR PPM tolerance	—	—	—	300	—	—	
Non DPA Mode							
Sampling Window	All differential I/O standards	—	—	300	—	—	400

Notes to Table 1–23:

(1) Numbers are preliminary pending characterization.
(2) When J = 3 to 10, the SERDES block is used.
(3) When J = 1 or 2, the SERDES block is bypassed.
(4) Clock boost factor (Ω) is the ratio between the input data rate to the input clock rate.
(5) The minimum specification is dependent on the clock source (for example, PLL and clock pin) and the clock routing resource (global, regional, or local) is used.
(6) Pending silicon characterization.

Table 1–24 lists the DPA lock time specifications.

Table 1–24. DPA Lock Time Specifications – Preliminary ***(Note 1)***

Standard	Training Pattern	Transition Density	Min	Typ	Max	Unit
SPI-4	00000000001111111111	10%	TBD	—	—	Number of repetitions
Parallel Rapid I/O	00001111	25%	TBD	—	—	Number of repetitions
	10010000	50%	TBD	—	—	Number of repetitions
Miscellaneous	10101010	100%	TBD	—	—	Number of repetitions
	01010101	100%	TBD	—	—	Number of repetitions

Note to Table 1–24:

(1) Pending silicon characterization.

External Memory I/O Timing Specifications

Table 1–25 and Table 1–26 list HardCopy III device timing uncertainties on the read and write data paths. Use these specifications to determine timing margins for source synchronous paths between the HardCopy III device and the external memory device. For timing diagram, refer to Figure 1–5 on page 1–23.

Table 1–25. Sampling Window (SW), Read Side – Preliminary *(Note 1)*

Location *(2)*	Memory Type	Sampling Window (ps)	
		Setup	Hold
VIO	DDR3	344	85
	DDR2	213	162
	DDR1	236	178
	QDRII / II +	218	203
	RLDRAM II	198	183
HIO	DDR3	344	85
	DDR2	213	162
	DDR1	236	178
	QDRII / II +	218	203
	RLDRAM	198	183

Notes to Table 1–25:

(1) Pending silicon characterization.

(2) VIO (vertical I/O) refers to I/Os in the top and bottom banks; HIO (horizontal I/O) refers to I/Os in the left and right banks.

Table 1–26. Transmitter Channel-to-Channel Skew (TCCS), Write Side – Preliminary *(Note 1)*

Location *(2)*	Memory Type	TCCS (ps)	
		Setup	Hold
VIO	DDR3	344	347
	DDR2	270	380
	DDR1	275	396
	QDRII / II +	294	408
	RLDRAM II	288	392
HIO	DDR3	344	347
	DDR2	270	380
	DDR1	275	396
	QDRII / II +	294	408
	RLDRAM II	288	392

Notes to Table 1–26:

(1) Pending silicon characterization.

(2) VIO (vertical I/O) refers to I/Os in the top and bottom banks; HIO (horizontal I/O) refers to I/Os in the left and right banks.

DLL and DQS Logic Block Specifications

Table 1–27 lists the delay-locked loop (DLL) frequency range specifications for HardCopy III devices.

Table 1–27. HardCopy III DLL Frequency Range Specifications – Preliminary *(Note 1)*

Frequency Mode	Frequency Range (MHz)	Resolution (Degrees)
0	TBD	22.5
1	TBD	30
2	TBD	36
3	TBD	45
4	TBD	30
5	TBD	36
6	TBD	45

Note to Table 1–27:

(1) Pending silicon characterization.

Table 1–28 lists the DQS phase offset delay per setting for HardCopy III devices.

Table 1–28. Average DQS Phase Offset Delay per Setting – Preliminary *(Note 1)*, *(2)*, *(3)*, *(4)*

Min	Typ	Max	Unit
7	11	15	ps

Notes to Table 1–28:

(1) The valid settings for phase offset are –64 to +63 for frequency modes 0 to 3 and –32 to +31 for frequency modes 4 to 6.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear with a cumulative delay variation of ±20ps for all speed grades.

(4) Pending silicon characterization.

OCT Calibration Block Specifications

Table 1–29 lists the OCT calibration block specifications for HardCopy III devices.

Table 1–29. OCT Calibration Block Specification – Preliminary

Symbol	Description	Min	Typical	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks.	—	—	20	MHz
t_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S and RT calibration.	—	1000	—	cycles
$t_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out per OCT calibration block.	—	28	—	cycles
t_{RS_RT}	Time required to switch from R_S to R_T dynamically.	—	2.5	—	ns

Duty Cycle Distortion (DCD) Specifications

Table 1–30 lists the worst case DCD for HardCopy III devices. Detailed information on DCD is published after characterization.

Table 1–30. DCD on HardCopy III I/O Pins – Preliminary *(Note 1)*, *(2)*

Symbol	Min	Max	Unit
Output Duty Cycle	45	55	%

Notes to Table 1–30:

(1) Preliminary DCD specification applies to clock outputs from PLLs, global clock tree, IOE driving dedicated, and general purpose I/O pins.

(2) Detailed DCD specifications pending silicon characterization.

Glossary

Table 1–31 lists the glossary for this chapter.

Table 1–31. Glossary Table (Part 1 of 4)

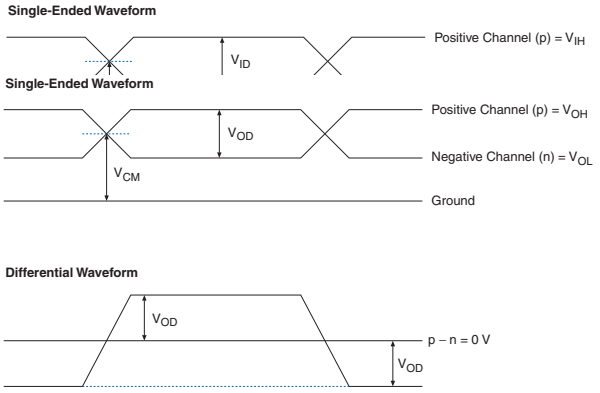
Letter	Subject	Definitions
A	—	—
B	—	—
C	—	—
D	Differential I/O Standards	**Figure 1–2. Receiver Input Waveforms** 
E	—	—
F	f_{HSCLK}	High-speed I/O Block: High-speed receiver/transmitter input and output clock frequency.
	f_{HSDR}	High-speed I/O Block: Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O Block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G	—	—
H	—	—
I	—	—

Table 1–31. Glossary Table (Part 2 of 4)

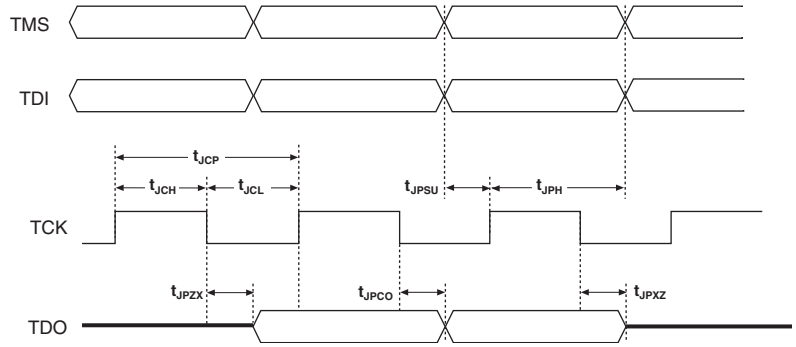
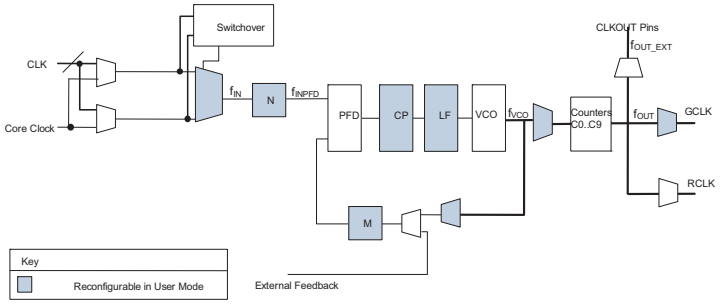
Letter	Subject	Definitions
J	J	High-speed I/O Block: Deserialization factor (width of parallel data bus).
J	JTAG Timing Specifications	**Figure 1–3. JTAG Timing Specifications** 
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Specifications	The block diagram shown in the following figure highlights the PLL specification parameters: **Figure 1–4. Diagram of PLL Specifications** ***(Note 1)***  **Note to Figure 1–4:** (1) Core clock can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to HardCopy III device).

Table 1–31. Glossary Table (Part 3 of 4)

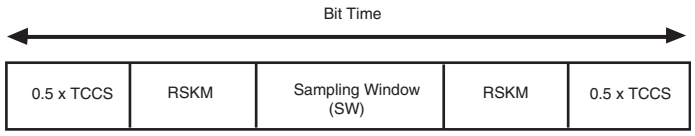
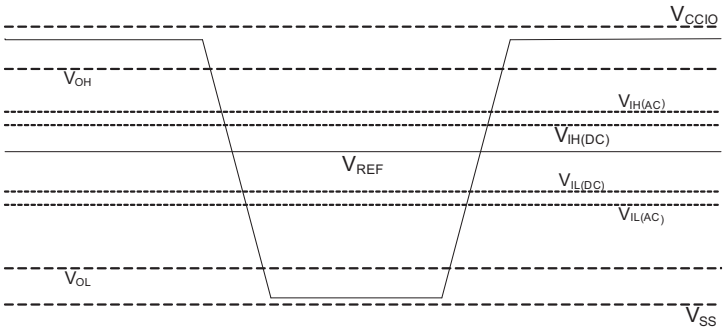
Letter	Subject	Definitions
S	SW (sampling window)	The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. **Figure 1–5. Timing Diagram** 
	Single-ended Voltage Referenced I/O Standard	The JEDEC standard for **SSTI** and **HSTL** I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state maintains as long as the input stays beyond the DC threshold. This approach provides predictable receiver timing in the presence of input waveform ringing. **Figure 1–6. Single-Ended Voltage Referenced I/O Standard** 
T	t_C	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and the slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is in the TCCS measurement (refer to Figure 1–5 under **S** in this table).
	t_{DUTY}	High-speed I/O Block: Duty cycle on high-speed transmitter output clock. Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on PLL clock input
	t_{OUTPJ_IO}	Period jitter on general purpose I/O driven by a PLL
	t_{OUTPJ_DC}	Period jitter on dedicated clock output driven by a PLL
	t_{RISE}	Signal low-to-high transition time (20–80%)
U	—	—

Table 1–31. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage: Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input that the device accepts as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input that the device accepts as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
W	W	High-speed I/O Block: Clock boost factor
X	—	—
Y	—	—
Z	—	—

Document Revision History

Table 1–32 lists the revision history for this document.

Table 1–32. Document Revision History

Date	Version	Changes
January 2011	4.0	■ Updated Table 1–19, Table 1–21, and Table 1–23. ■ Removed "External Memory Interface Specifications" and "I/O Timing" sections . ■ Added a note to Table 1–23. ■ Updated the "Glossary" section. ■ Made general editorial changes. ■ Updated to the new document template.
June 2009	3.0	Added new part numbers and clock tree performance specifications (Table 1–18).
December 2008	2.0	■ Updated Table 1–3. ■ Updated Table 1–19. ■ Updated Table 1–23. ■ Made minor editorial changes.
May 2008	1.0	Initial release.