

This section provides the datasheet for the HardCopy® IV device family. This section includes the following chapter:

- [Chapter 1, DC and Switching Characteristics of HardCopy IV Devices](#)

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

Electrical Characteristics

This chapter covers the electrical characteristics for HardCopy® IV devices.

Operating Conditions

When implementing HardCopy IV devices in a system, the system rates the devices according to a set of defined parameters. To maintain the highest possible performance and reliability, consider the operating requirements described in this chapter. HardCopy IV devices are not speed binned, such as the Stratix® IV devices, because HardCopy IV devices function at a target frequency based on timing constraints. Altera offers HardCopy IV devices in commercial and industrial grades.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for HardCopy IV devices. Experiments with the device and theoretical modeling of breakdown and damage mechanisms provide these values. These conditions do not imply the functional operation of the device.

Table 1–1 lists the absolute maximum ratings for a HardCopy IV device.



Conditions other than those listed in Table 1–1 and Table 1–3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1. HardCopy IV Device Absolute Maximum Ratings—Preliminary (Part 1 of 2) (Note 1)

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	–0.5	1.35	V
V_{CCPT} (2)	Power supply for programmable power technology	—	—	V
V_{CCPGM}	Configuration pins power supply	–0.5	3.75	V
V_{CCAUX}	Power supply for temperature sensing diode and POR	–0.5	3.75	V
V_{CCBAT} (3)	Battery back-up power supply for design security volatile key register	—	—	V
V_{CCPD}	I/O predriver power supply	–0.5	3.75	V
V_{CCIO}	I/O power supply	–0.5	3.9	V
V_{CC_CLKIN}	Differential clock input power supply	–0.5	3.75	V
V_{CCD_PLL}	Phase-locked loop (PLL) digital power supply	–0.5	1.35	V
V_{CCA_PLL}	PLL analog power supply	–0.5	3.75	V
V_I	DC input voltage	–0.5	4.0	V

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Table 1–1. HardCopy IV Device Absolute Maximum Ratings—Preliminary (Part 2 of 2) (Note 1)

Symbol	Description	Minimum	Maximum	Unit
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	C
T_{STG}	Storage temperature (No bias)	–65	150	C

Notes to Table 1–1:

- (1) Supply voltage specifications apply to voltage readings taken at the device pins and not the power supply.
- (2) HardCopy IV devices do not require programmable power technology.
- (3) HardCopy IV devices do not use this power supply.

Table 1–2 lists the power supply absolute maximum ratings for HardCopy IV GX transceiver.

Table 1–2. HardCopy IV GX Transceiver Power Supply Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	–0.5	3.75	V
V_{CCA_R}	Transceiver high voltage power (right side)	–0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP digital power (right side)	–0.5	1.35	V
V_{CCHIP_R}	Transceiver hard IP digital power (left side)	–0.5	1.35	V
V_{CCR_L}	Receiver power (left side)	–0.5	1.35	V
V_{CCR_R}	Receiver power (right side)	–0.5	1.35	V
V_{CCT_L}	Transmitter power (left side)	–0.5	1.35	V
V_{CCT_R}	Transmitter power (right side)	–0.5	1.35	V
V_{CCL_GXBLn} (1)	Transceiver clock power (left side)	–0.5	1.35	V
V_{CCL_GXBRn} (1)	Transceiver clock power (right side)	–0.5	1.35	V
V_{CCH_GXBLn} (1)	Transmitter output buffer power (left side)	–0.5	1.65	V
V_{CCH_GXBRn} (1)	Transmitter output buffer power (right side)	–0.5	1.65	V

Note to Table 1–2:

- (1) The V_{CCH} and V_{CCL} powers are per transceiver block.

Maximum Allowed Overshoot or Undershoot Voltage

Table 1-3 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is a percentage of high-time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

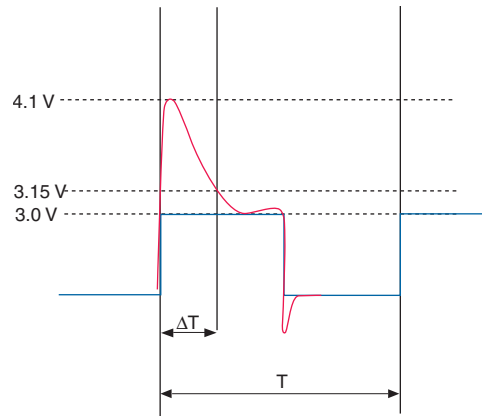
During transitions, input signals may overshoot to the voltage shown in Table 1-3 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1-3. Maximum Allowed Overshoot During Transitions—Preliminary

Symbol	Description	Condition	Overshoot Duration as Percentage of High Time	Unit
Vi (AC)	AC input voltage	4.0 V	100.000	%
		4.05 V	79.330	%
		4.1 V	46.270	%
		4.15 V	27.030	%
		4.2 V	15.800	%
		4.25 V	9.240	%
		4.3 V	5.410	%
		4.35 V	3.160	%
		4.4 V	1.850	%
		4.45 V	1.080	%
		4.5 V	0.630	%
		4.55 V	0.370	%
		4.6 V	0.220	%
		4.65 V	0.130	%
		4.7 V	0.074	%
		4.75 V	0.043	%
4.8 V	0.025	%		
4.85 V	0.015	%		

Figure 1-1 shows the methodology to determine overshoot duration. The color red shows the overshoot voltage and is present at the HardCopy IV pin, up to 4.1 V. In Table 1-3, for an overshoot of up to 4.1 V, the percentage of high time for overshoot is greater than 3.15 V can be as high as 46% over an 11.4 year period. The percentage of high time is $(\Delta T/T) \times 100$. This 11.4 year period assumes that you turned on the device with 100% I/O toggle rate and 50% duty cycle signal. Lifetimes increase for lower I/O toggle rates and situations in which the device is in an idle state.

Figure 1-1. Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for HardCopy IV devices. Table 1-4 shows the steady-state voltage and current values expected from HardCopy IV devices. All supplies must reach their full-rail values in t_{RAMP} maximum monotonically. The minimum and maximum specifications listed in Table 1-4 binds the allowed ripple on power supplies.

Table 1-4. HardCopy IV Device Recommended Operating Conditions—Preliminary (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	—	0.87	0.90	0.93	V
$V_{CCPT} (1)$	Power supply for programmable power technology	—	—	—	—	V
V_{CCAUX}	Power supply for the temperature sensing diode and POR	—	2.375	2.5	2.625	V
V_{CCPD}	I/O predriver (3.0 V) power supply	—	2.85	3	3.15	V
	I/O predriver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V

Table 1-4. HardCopy IV Device Recommended Operating Conditions—Preliminary (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V _{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V _{CCA_PLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _{CCD_PLL}	PLL digital voltage regulator power supply	—	0.87	0.90	0.93	V
V _{CC_CLKIN}	Differential clock input power supply	—	1.075	1.2	1.325	V
	Differential clock input power supply	—	1.375	1.5	1.625	V
	Differential clock input power supply	—	1.675	1.8	1.925	V
	Differential clock input power supply	—	2.375	2.5	2.625	V
	Differential clock input power supply	—	2.875	3.0	3.125	V
V _{CCBAT} (2)	Battery back-up power supply (for design security volatile key register)	—	—	—	—	V
V _I	DC input voltage	—	-0.5	—	3.6	V
V _O	Output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	-40	—	100	°C
t _{RAMP}	Power supply ramp time	Normal POR (PORSEL = 1)	0.05	—	100	ms
		Fast POR (PORSEL = 1) (3)	0.05	—	4	ms

Notes to Table 1-4:

- (1) HardCopy IV devices do not require programmable power technology.
- (2) HardCopy IV devices do not require this power supply.
- (3) If the PORSEL pin is connected to V_{CC}, all supplies must ramp up in 4 ms.

Table 1-5 shows the transceiver power supply recommended operating conditions.

Table 1-5. HardCopy IV GX Transceiver Power Supply Recommended Operating Conditions (Part 1 of 2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V _{CCA_L}	Transceiver high voltage power (left side)	2.85 or 2.375	3.0 or 2.5 (3)	3.15 or 2.625	V
V _{CCA_R}	Transceiver high voltage power (right side)				V
V _{CCHIP_L} (1)	Transceiver hard IP digital power (right side)	0.87	0.90	0.93	V
V _{CCHIP_R} (1)	Transceiver hard IP digital power (left side)				V
V _{CCR_L}	Receiver power (left side)	1.05	1.1	1.15	V
V _{CCR_R}	Receiver power (right side)				V
V _{CCT_L}	Transmitter power (left side)	1.05	1.1	1.15	V
V _{CCT_R}	Transmitter power (right side)				V

Table 1-5. HardCopy IV GX Transceiver Power Supply Recommended Operating Conditions (Part 2 of 2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCL_GXBLn} (2)	Transceiver clock power (left side)	1.05	1.1	1.15	V
V_{CCL_GXBRn} (2)	Transceiver clock power (right side)				V
V_{CCH_GXBLn} (2)	Transmitter output buffer power (left side)	1.33 or 1.425	1.4 or 1.5 (4)	1.47 or 1.575	V
V_{CCH_GXBRn} (2)	Transmitter output buffer power (right side)				V

Notes to Table 1-5:

- (1) If $V_{CCHIP_L/R}$ is connected to the same power supply source as V_{CC} , the recommended minimum and maximum operating supply levels are 0.87 V and 0.93 V respectively.
- (2) The V_{CCH} and V_{CCL} powers are per transceiver block.
- (3) $V_{CCA_L/R}$ must be connected to a 3.0 V supply if the clock multiplier unit phase-locked loops (CMU PLLs), receiver clock data recovery (CDR), or both are configured at a base data rate > 4.25Gbps. For data rates up to 4.25 Gbps, you can connect $V_{CCA_L/R}$ to either 3.0 V or 2.5 V.
- (4) For data rates up to 6.5 Gbps, you can connect $V_{CCH_GXBL/R}$ to either 1.4 V or 1.5 V.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination (OCT) tolerance, and hot socketing specifications.

Supply Current

Standby current is the current the device draws after configuration, with no inputs or outputs toggling and no activity in the device. Because these currents vary with the resources you use, use the Excel-based PowerPlay Early Power Estimator (EPE) to get supply current estimates for your design.

Table 1-6 lists supply current specifications for V_{CC_CLKIN} and V_{CCPGM} . Use the PowerPlay EPE to get supply current estimates for the remaining power supplies.

Table 1-6. Supply Current Specifications for V_{CC_CLKIN} and V_{CCPGM} —Preliminary (Note 1)

Symbol	Parameter	Min	Max	Unit
I_{CLKIN}	V_{CC_CLKIN} current specifications	0	TBD	mA
I_{PGM}	V_{CCPGM} current specifications	0	TBD	mA

Note to Table 1-6:

- (1) Pending silicon characterization.

I/O Pin Leakage Current

Table 1-7 lists the HardCopy IV I/O pin leakage current specifications.

Table 1-7. HardCopy IV I/O Pin Leakage Current—Preliminary (Note 1), (2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_i	Input pin	$V_i = 0_V$ to $V_{CCIOMAX}$	-10	—	10	μA
I_{oz}	Tristated I/O pin	$V_o = 0_V$ to $V_{CCIOMAX}$	-10	—	10	μA

Notes to Table 1-7:

- (1) This value is for normal device operation. The value may vary during power up. This applies for all V_{CCIO} settings (3.0, 2.5, 1.8, 1.5, and 1.2 V).
- (2) The 10 mA I/O leakage current limit is applicable when the internal clamping diode is off. You can observe a higher current when the diode is on.

OCT Specifications

If you enabled OCT calibration, calibration is automatically performed at power up for I/Os connected to the calibration block. Table 1-8 lists the HardCopy IV OCT calibration block accuracy specifications.

Table 1-8. HardCopy IV OCT With Calibration Specification for I/Os—Preliminary (Note 1)

Symbol	Description	Conditions	Calibration Accuracy		Unit
			Commercial (2)	Industry	
25-Ω R _S 3.0/2.5	Internal series termination with calibration (25-Ω setting)	V _{CCIO} = 3.0 or 2.5 V	TBD	—	%
50-Ω R _S 3.0/2.5	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 3.0 or 2.5 V	TBD	—	%
50-Ω R _T 2.5	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 2.5 V	TBD	—	%
25-Ω R _S 1.8	Internal series termination with calibration (25-Ω setting)	V _{CCIO} = 1.8 V	TBD	—	%
50-Ω R _S 1.8	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 1.8 V	TBD	—	%
50-Ω R _T 1.8	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 1.8 V	TBD	—	%
50-Ω R _S 1.5	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 1.5 V	TBD	—	%
50-Ω R _T 1.5	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 1.5 V	TBD	—	%
50-Ω R _S 1.2	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 1.2 V	TBD	—	%
50-Ω R _T 1.2	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 1.2 V	TBD	—	%

Notes to Table 1-8:

- (1) OCT calibration accuracy is valid at the time of calibration only.
- (2) Pending silicon characterization.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. If the voltage or temperature changes, the termination resistance value varies. Table 1-9 lists the resistance tolerance for HardCopy IV OCT.

Table 1-9. I/O OCT Resistance Tolerance—Preliminary (Note 1)

Symbol	Description	Resistance Tolerance		
		Commercial Max	Industrial Max	Unit
R _{OCT_CAL}	Internal series or parallel OCT with calibration	(2)	—	%
R _{OCT_UNCAL}	Internal series or parallel OCT without calibration	TBD	—	%

Notes to Table 1-9:

- (1) Pending silicon characterization.
- (2) For resistance tolerance after power-up calibration, refer to Table 1-10.

Table 1-10 lists OCT variation with temperature and voltage after power-up calibration. Use Table 1-10 and Equation 1-1 to determine the OCT variation when voltage and temperature vary after power-up calibration.

Equation 1-1. OCT Variation Without Recalibration (Note 1)

$$R_{OCT} = R_{CAL} \left(1 + \frac{dR}{dT} \times \Delta T + \frac{dR}{dV} \times \Delta V \right)$$

Note to Equation 1-1:

- (1) R_{CAL} is calibrated OCT at power up. ΔT and ΔV are variations in temperature and voltage about temperature and V_{CCIO} values, respectively, at power up.

Table 1-10. OCT Variation after Power-Up Calibration—Preliminary (Note 1), (2)

Symbol	Description	V_{CCIO} (V)	Commercial Typical	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	TBD	% / mV
		2.5	TBD	
		1.8	TBD	
		1.5	TBD	
		1.2	TBD	
dR/dT	OCT variation with temperature without recalibration	3.0	TBD	% / °C
		2.5	TBD	
		1.8	TBD	
		1.5	TBD	
		1.2	TBD	

Notes to Table 1-10:

- (1) Valid for V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C .
 (2) Pending silicon characterization.

Pin Capacitance

Table 1-11 lists the HardCopy IV device family pin capacitance.

Table 1-11. HardCopy IV Device Capacitance—Preliminary (Part 1 of 2) (Note 1)

Symbol	Description	Typical	Unit
C_{IOTB}	Input capacitance on top or bottom I/O pins	TBD	pF
C_{IOLR}	Input capacitance on left or right I/O pins	TBD	pF
C_{CLKTB}	Input capacitance on top or bottom dedicated clock input pins	TBD	pF
C_{CLKLR}	Input capacitance on left or right dedicated clock input pins	TBD	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output or feedback pins	TBD	pF

Table 1-11. HardCopy IV Device Capacitance—Preliminary (Part 2 of 2) (Note 1)

Symbol	Description	Typical	Unit
C_{CLK1} C_{CLK3} C_{CLK8} C_{CLK10}	Input capacitance for dedicated clock input pins	TBD	pF

Note to Table 1-11:

- (1) Pending silicon characterization.

Hot Socketing

Table 1-12 lists the hot socketing specification for HardCopy IV devices.

Table 1-12. HardCopy IV Hot Socketing Specifications—Preliminary (Note 1)

Symbol	Description	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	300 μ A
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA for $t_{RISE} > 10$ ns

Note to Table 1-12:

- (1) Pending silicon characterization.

Internal Weak Pull-Up Resistor

Table 1-13 lists the weak pull-up resistor values for HardCopy IV devices.

Table 1-13. HardCopy IV Internal Weak Pull-Up Resistor—Preliminary (Note 1), (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	The value of I/O pin pull-up resistor before and during user mode, if the pull-up resistor option is enabled.	$V_{CC10} = 3.0\text{ V} \pm 5\%$ (3)	—	25	—	k Ω
		$V_{CC10} = 2.5\text{ V} \pm 5\%$ (3)	—	25	—	k Ω
		$V_{CC10} = 1.8\text{ V} \pm 5\%$ (3)	—	25	—	k Ω
		$V_{CC10} = 1.5\text{ V} \pm 5\%$ (3)	—	25	—	k Ω
		$V_{CC10} = 1.2\text{ V} \pm 5\%$ (3)	—	25	—	k Ω

Notes to Table 1-13:

- (1) Pending silicon characterization.
 (2) All I/O pins have an option to enable weak pull-up except test and JTAG pins.
 (3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CC10} .

I/O Standard Specifications

Table 1-14 through Table 1-19 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by HardCopy IV devices. These tables also show the HardCopy IV device family I/O standard specifications. For an explanation of terms used in Table 1-14 through Table 1-19, refer to the “Glossary” on page 1-36. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.

Table 1-14. Single-Ended I/O Standards—Preliminary

I/O Standard	V_{CCIO} (V)			V_L (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.0-V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5-V LVTTTL/LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.2	2.1	0.1	-0.1
								0.4	2	1	-1
								0.7	1.7	2	-2
1.8-V LVTTTL/LVCMOS	1.71	1.8	1.89	-0.3	$0.35 * V_{CCIO}$	$0.65 * V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5-V LVTTTL/LVCMOS	1.425	1.5	1.575	-0.3	$0.35 * V_{CCIO}$	$0.65 * V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 * V_{CCIO}$	$0.75 * V_{CCIO}$	2	-2
1.2-V LVTTTL/LVCMOS	1.14	1.2	1.26	-0.3	$0.35 * V_{CCIO}$	$0.65 * V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 * V_{CCIO}$	$0.75 * V_{CCIO}$	2	-2
3.0-V PCI	2.85	3	3.15	—	$0.3 * V_{CCIO}$	$0.5 * V_{CCIO}$	3.6	$0.1 * V_{CCIO}$	$0.9 * V_{CCIO}$	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 * V_{CCIO}$	$0.5 * V_{CCIO}$	—	$0.1 * V_{CCIO}$	$0.9 * V_{CCIO}$	1.5	-0.5

For an example of a voltage referenced receiver input waveform and explanation of terms used in Table 1-15, refer to Figure 1-10 on page 1-39.

Table 1-15. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications—Preliminary

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.51 * V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.48 * V_{CCIO}$	$0.5 * V_{CCIO}$	$0.52 * V_{CCIO}$	—	$V_{CCIO}/2$	—

Table 1-16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications—Preliminary

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{ol} (mA)$	$I_{oh} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.57$	$V_{TT} + 0.57$	8.1	-8.1
SSTL-2 Class II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.76$	$V_{TT} + 0.76$	16.2	-16.2
SSTL-18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	$V_{TT} - 0.475$	$V_{TT} + 0.475$	6.7	-6.7
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	8	-8
SSTL-15 Class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	16	-16
HSTL-18 Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 * V_{CCIO}$	$0.75 * V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 * V_{CCIO}$	$0.75 * V_{CCIO}$	16	-16

For receiver input and transmitter output waveforms and for all differential I/O standards (LVDS, mini-LVDS, and RSDS), refer to Figure 1-5 on page 1-37 and Figure 1-6 on page 1-37. $V_{CC,CLKIN}$ is the power supply for differential column clock input pins. V_{CCPD} is the power supply for row I/Os and all other column I/Os.

Table 1-17. Differential SSTL I/O Standard Specifications—Preliminary

I/O Standard	$V_{CCIO} (V)$			$V_{SWING(DC)} (V)$		$V_{X(AC)} (V)$			$V_{SWING(AC)} (V)$		$V_{OX(AC)} (V)$		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.6	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$
SSTL-18 Class I, II	1.71	1.8	1.89	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	—	$V_{CCIO}/2$	—	0.4	—	—	$V_{CCIO}/2$	—

Table 1-18. Differential HSTL I/O Standard Specifications—Preliminary

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.8	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.7	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.2	—	—	0.5 * V _{CCIO}	—	0.4 * V _{CCIO}	0.5 * V _{CCIO}	0.6 * V _{CCIO}	0.3	—

Table 1-19. Differential I/O Standard Specifications—Preliminary (Note 1)

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)			V _{ICM(DC)} (V)			V _{OD} (V) (2)			V _{OCM} (V) (2)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
2.5-V LVDS (HIO)	2.375	2.5	2.625	100	V _{CM} - 1.25 V	—	0.05 (4)	D _{MAX} ≤ 700 Mbps	1.8 (4)	0.247	—	0.6	1.125	1.25	1.375
						—	1.05 (4)	D _{MAX} > 700 Mbps	1.55 (4)	—	—	—	—	—	
2.5-V LVDS (VIO)	2.375	2.5	2.625	100	V _{CM} - 1.25 V	—	0.05 (4)	D _{MAX} ≤ 700 Mbps	1.8 (4)	0.247	—	0.6	1	1.25	1.5
						—	1.05 (4)	D _{MAX} > 700 Mbps	1.55 (4)	—	—	—	—	—	
RSDS (HIO)	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (VIO)	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.4
Mini-LVDS (VIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.5
LVPECL (VIO) (5)	2.375 (6)	2.5 (6)	2.625 (6)	300	—	—	0.6	D _{MAX} ≤ 700 Mbps	1.8 (3)	—	—	—	—	—	—
	—	—	—	—	—	—	0.6	D _{MAX} > 700 Mbps	1.6 (3)	—	—	—	—	—	—

Notes to Table 1-19:


- (1) VIO (vertical I/O) is top and bottom I/Os; HIO (horizontal I/O) is left and right I/Os.
- (2) RL range: 90 ≤ RL ≤ 110 Ω
- (3) For D_{MAX} > 700 Mbps, the minimum input voltage is 0.85 V; the maximum input voltage is 1.75 V. For F_{MAX} ≤ 700 Mbps, the minimum input voltage is 0.45 V; the maximum input voltage is 1.95 V.
- (4) For data rate: D_{MAX} > 700 Mbps, the minimum input voltage is 1.0 V, the maximum input voltage is 1.6 V. For D_{MAX} ≤ 700 Mbps, the minimum input voltage is 0 V, the maximum input voltage is 1.85 V.
- (5) Column and row I/O banks support LVPECL I/O standards for input operation only on dedicated clock input pins. Differential clock inputs in column I/O use V_{CC_CLKIN}, which must be powered by 2.5 V. Differential clock inputs in row I/Os are powered by V_{CCPD}.
- (6) The power supply for column I/O LVPECL differential clock input buffer is V_{CC_CLKIN}.

Power Consumption

Altera offers the Excel-based PowerPlay EPE and the Quartus® II PowerPlay Power Analyzer feature to estimate power consumption for your design.

Use the interactive Excel-based PowerPlay EPE before designing your HardCopy IV device to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of your design after placement and routing is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.

For supply current estimates for V_{CCPGM} and $V_{CC,CLKIN}$, refer to [Table 1-6 on page 1-6](#). Use the PowerPlay EPE and Power Analyzer for current estimates of the remaining power supplies.

 For more information about power estimation tools, refer to the [PowerPlay Early Power Estimator](#) page on the Altera website and the [PowerPlay Power Analysis](#) chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of HardCopy IV core and periphery blocks for commercial grade devices.

HardCopy IV devices can meet, at minimum, the -3 speed grade of the Stratix IV devices. Silicon characterization determines the actual performance of the HardCopy IV devices. These characteristics are **Preliminary** or **Final**, as defined in the following:

- **Preliminary**—Created using simulation results, process data, and other known parameters.
- **Final**—Based on actual silicon characterization and testing.

These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

Transceiver Performance Specifications

This section describes transceiver performance specifications. [Table 1-20](#) lists HardCopy IV GX transceiver specifications.

Table 1-20. HardCopy IV GX Transceiver Specifications (Part 1 of 6)

Symbol	Parameter	Min	Typ	Max	Unit
Reference Clock					
Input frequency from REFCLK input pins	—	50	—	672	MHz
Phase frequency detector (CMU PLL and receiver CDR)	—	50	—	325	MHz

Table 1-20. HardCopy IV GX Transceiver Specifications (Part 2 of 6)

Symbol	Parameter	Min	Typ	Max	Unit
Absolute Vmax for a REFCLK pin	—	—	—	1.6	V
Operational Vmax for a REFCLK pin	—	—	—	1.5	V
Absolute Vmin for a REFCLK pin	—	-0.4	—	—	V
Rise/fall time	—	—	—	0.2	UI
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	1600	mV
Spread-spectrum modulating clock frequency	PCI Express	30	—	33	kHz
Spread-spectrum downspread	PCI Express	—	0 to -0.5%	—	—
OCT resistors	—	—	100	—	Ω
VICM (AC coupled)	—	—	1100	—	mV
VICM (DC coupled)	HCSL I/O standard for PCI Express reference clock	250	—	550	mV
Rref	—	—	2000 \pm 1%	—	Ω
Transceiver Clocks					
Calibration block clock frequency	—	10	—	125	MHz
fixedclk clock frequency	PCI Express Receiver Detect	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5 or 37.5 (2)	—	50	—
Transceiver block minimum power-down pulse width	—	—	1	—	μ s
Receiver					
Data rate (Single width, non-PMA Direct)	—	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct)	—	1000	—	6500	Mbps
Data rate (Single width, PMA Direct)	—	600	—	3250	Mbps
Data rate (Double width, PMA Direct)	—	1000	—	6500	Mbps

Table 1-20. HardCopy IV GX Transceiver Specifications (Part 3 of 6)

Symbol	Parameter	Min	Typ	Max	Unit
Absolute Vmax for a receiver pin (3)	—	—	—	1.6	V
Operational Vmax for a receiver pin	—	—	—	1.5	V
Absolute Vmin for receiver pin	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage VID (diff p-p)	VICM = 0.82-V setting	—	—	2.7	V
	VICM = 1.1-V setting (4)	—	—	1.6	V
Minimum peak-to-peak differential input voltage VID (diff p-p)	Data Rate = 600 Mbps to 5 Gbps	100	—	—	mV
	Data Rate > 5 Gbps	165	—	—	mV
VICM	VICM = 0.82-V setting	—	820	—	mV
	VICM = 1.1-V setting (4)	—	1100	—	mV
Differential OCT resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Return loss differential mode	PCI Express	50 MHz to 1.25 GHz: -10dB		—	—
	XAUI	100 MHz to 2.5 GHz: -10dB		—	—
	(OIF) CEI	100 MHz to 4.875 GHz: -8dB 4.875GHz to 10GHz: 16.6 dB/decade slope		—	—
Return loss common mode	PCI Express	50 MHz to 1.25 GHz: -6dB		—	—
	XAUI	100 MHz to 2.5 GHz: -6dB		—	—
	(OIF) CEI	100 MHz to 4.875 GHz: -6dB 4.875GHz to 10GHz: 16.6 dB/decade slope		—	—
Programmable PPM detector (5)	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000	—	—	ppm
Run length	—	—	80	—	Ui
Programmable equalization	—	—	—	16	dB
Signal detect/loss threshold	PCI Express (PIPE) Mode	65	—	175	mV
CDR LTR time (6)	—	—	—	75	μs
CDR minimum T1b (7)	—	15	—	—	μs
LTD lock time (8)	—	0	100	4000	ns

Table 1-20. HardCopy IV GX Transceiver Specifications (Part 4 of 6)

Symbol	Parameter	Min	Typ	Max	Unit
Data lock time from rx_freqlocked (9)	—	—	—	4000	ns
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	7872	reconfig_clk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	dB
	DC Gain Setting = 1	—	3	—	dB
	DC Gain Setting = 2	—	6	—	dB
	DC Gain Setting = 3	—	9	—	dB
	DC Gain Setting = 4	—	12	—	dB
Transmitter					
Data rate (Single width, non-PMA Direct)	—	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct)	—	1000	—	6500	Mbps
Data rate (Single width, PMA Direct) (10)	—	600	—	3250	Mbps
Data rate (Double width, PMA Direct) (10)	—	1000	—	6500	Mbps
VOCM	0.65-V setting	—	650	—	mV
Differential OCT resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Return loss differential mode	PCI Express	50 MHz to 1.25 GHz: -10 dB		—	—
	XAUI	312 MHz to 625 MHz: -10 dB 625 MHz to 3.125 GHz: -10 dB/decade slope		—	—
	(OIF) CEI	100 MHz to 4.875 GHz: -8 dB 4.875 GHz to 10 GHz: 16.6 dB/decade slope		—	—
Return loss common mode	PCI Express	50 MHz to 1.25 GHz: -6 dB		—	—
	(OIF) CEI	100 MHz to 4.875 GHz: -6 dB 4.875 GHz to 10 GHz: 16.6 dB/decade slope		—	—
Rise time	—	50	—	200	ps
Fall time (11)	—	50	—	200	ps
Intra differential pair skew	—	—	—	15	ps

Table 1-20. HardCopy IV GX Transceiver Specifications (Part 5 of 6)

Symbol	Parameter	Min	Typ	Max	Unit
Intra-transceiver block skew $\times 4$ PMA and PCS bonded	XAUI, PCI Express (PIPE) $\times 4$, Basic $\times 4$	—	—	120	ps
Inter-transceiver block skew $\times 8$ PMA and PCS bonded	PCI Express (PIPE) $\times 8$, Basic $\times 8$	—	—	500	ps
Inter-transceiver block skew $\times N$ PMA-Only bonded (12)	$N < 18$ channels located across three transceiver blocks with the source CMU PLL located in the center transceiver block	—	—	400	ps
CMU PLL0 and CMU PLL1					
Supported Data Range	—	600	—	6500	Mbps
CMU PLL lock time from pll_powerdown deassertion	—	—	—	100	μ s
ATX PLL					
Supported Data Range (13)	/L = 1	4800 to 5400 and 6000 to 6375	—	—	Mbps
	/L = 2	2400 to 2700 and 3000 to 3187.5	—	—	Mbps
	/L = 4	1200 to 1350 and 1500 to 1593.75	—	—	Mbps

Table 1-20. HardCopy IV GX Transceiver Specifications (Part 6 of 6)

Symbol	Parameter	Min	Typ	Max	Unit
Transceiver-HCell Logic Interface					
Interface speed (non-PMA Direct)	—	25	—	250	MHz
Interface speed (PMA Direct)	—	50	—	325	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles		—	—

Notes to Table 1-20:

- (1) The -2X speed grade is the fastest speed grade offered in the following HardCopy IV GX devices: HC4GX15LF780N, HC4GX25LF780N, HC4GX25LF1152N, HC4GX25FF1152N, HC4GX35FF1152N, HC4GX35LF1517N and HC4GX35FF1517N.
- (2) The minimum `reconfig_clk` frequency is 2.5 MHz if you configure the transceiver channel in transmitter only mode. The minimum `reconfig_clk` frequency is 37.5 MHz if you configure the transceiver channel in receiver only or receiver and transmitter mode. For more information, refer to *HardCopy IV GX Dynamic Reconfiguration* chapter in volume 3 of the *HardCopy IV Device Handbook*.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) Use the 1.1-V RX VICM setting if the input serial data standard is **LVDS** and the link is DC coupled.
- (5) The rate matcher supports only up to ± 300 ppm.
- (6) The duration for `rx_pll_locked` signal goes high from `rx_analogreset` deassertion. For more information, refer to [Figure 1-2 on page 1-19](#).
- (7) The duration for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` signal goes high and before `rx_locktodata` is asserted in manual mode. For more information, refer to [Figure 1-2 on page 1-19](#).
- (8) The duration for to recover valid data after the `rx_locktodata` signal is asserted in manual mode. For more information, refer to [Figure 1-2 on page 1-19](#).
- (9) The duration for to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. For more information, refer to [Figure 1-3 on page 1-19](#).
- (10) A general- purpose PLL (GPPLL) may be required to meet PMA-HardCopy fabric interface timing above certain data rates and this requirement is the same as PMA-FPGA fabric interface. For more information, refer to section “Left/Right PLL Requirements in Basic (PMA Direct) Mode” in the *Stratix IV Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.
- (11) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (12) For applications that require low transmit lane-to-lane skew, use Basic (PMA Direct) xN to achieve PMA-Only bonding across all channels in the link. You can bond all channels on one side of your device by configuring the channels in Basic (PMA-Direct) xN mode. For more information about clocking requirements in Basic (PMA-Direct) xN mode, refer to the “Basic (PMA Direct) Mode Clocking” section in the *Stratix IV Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.
- (13) The Quartus II software automatically selects the appropriate /L divider depending upon the configured data rate.

Figure 1-2 shows the lock time parameters in manual mode. Figure 1-3 shows the lock time parameters in automatic mode.


 LTD = Lock-To-Data; LTR = Lock-To-Reference

Figure 1-2. Lock Time Parameters for Manual Mode

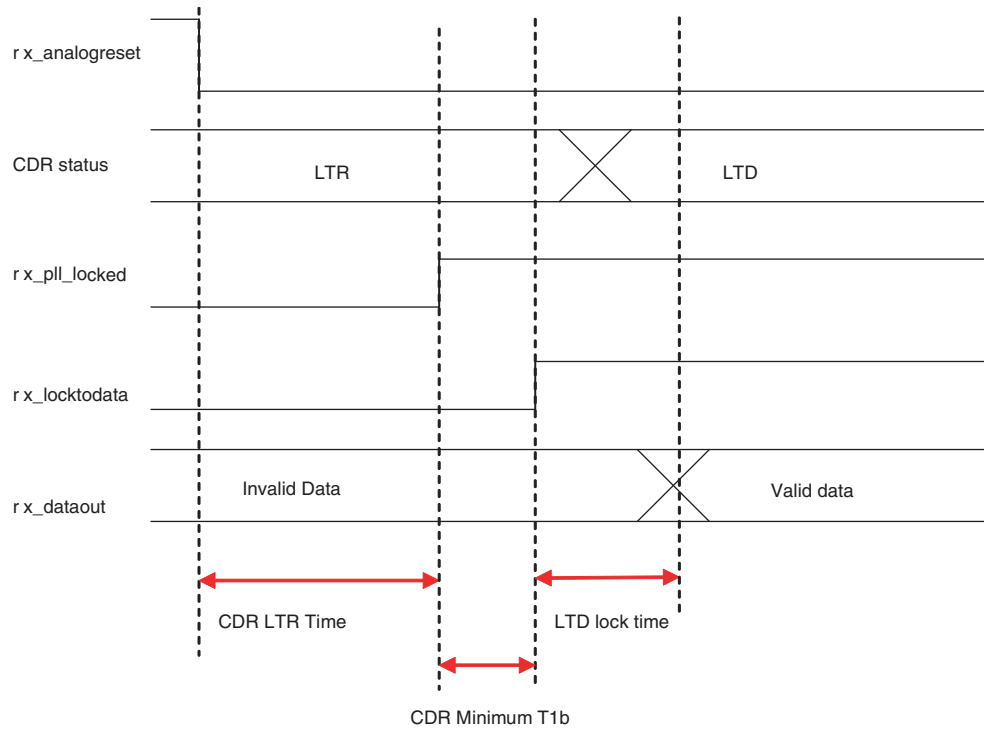


Figure 1-3. Lock Time Parameters for Automatic Mode

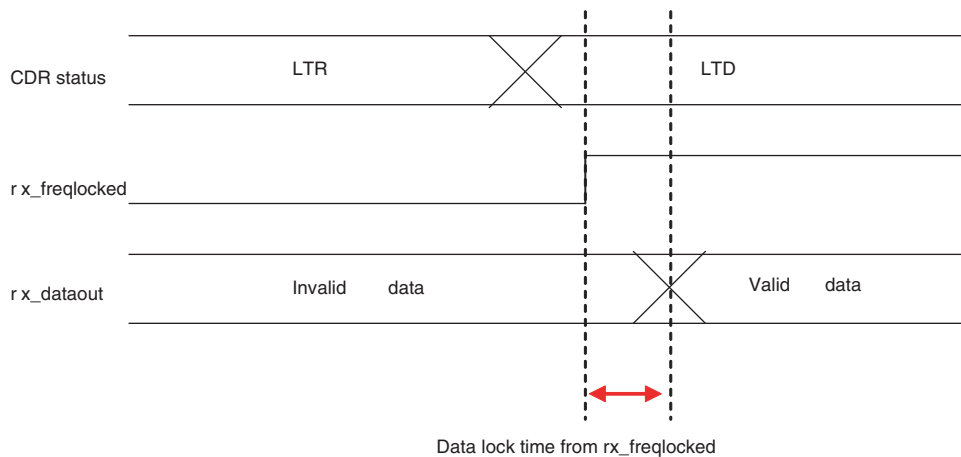


Table 1–21 through Table 1–24 list the typical V_{OD} for various differential termination settings for HardCopy IV GX devices.

Table 1–21. Typical VOD Setting, TX Term = 85 Ω

Symbol	VOD Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	170± 20%	340± 20%	510± 20%	595± 20%	680± 20%	765± 20%	850± 20%	1020± 20%

Table 1–22. Typical VOD Setting, TX Term = 100 Ω

Symbol	VOD Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	200± 20%	400± 20%	600± 20%	700± 20%	800± 20%	900± 20%	1000± 20%	1200± 20%

Table 1–23. Typical VOD Setting, TX Term = 120 Ω

Symbol	VOD Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	240± 20%	480± 20%	600± 20%	720± 20%	840± 20%	960± 20%	1080± 20%	1200± 20%

Table 1–24. Typical VOD Setting, TX Term = 150 Ω

Symbol	VOD Setting (mV)					
	0	1	2	3	4	5
VOD differential peak-to-peak Typical (mV)	300± 20%	600± 20%	900± 20%	1050± 20%	1200± 20%	1350± 20%

Table 1–25 lists typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–25 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.



To estimate the pre-emphasis level for your specific data rate and pattern, run simulations using the HardCopy IV high-speed serial interface (HSSI) HSPICE models.

Table 1-25. Transmitter Pre-emphasis Levels for HardCopy IV Devices

Pre-emphasis First Post-Tap Setting	VOD Setting							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	—	0.7	0	0	0	0	0	0
2	—	1	0.3	0	0	0	0	0
3	—	1.5	0.6	0	0	0	0	0
4	—	2	0.7	0.3	0	0	0	0
5	—	2.7	1.2	0.5	0.3	0	0	0
6	—	3.1	1.3	0.8	0.5	0.2	0	0
7	—	3.7	1.8	1.1	0.7	0.4	0.2	0
8	—	4.2	2.1	1.3	0.9	0.6	0.3	0
9	—	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	—	5.4	2.8	1.9	1.4	1	0.7	0.3
11	—	6	3.2	2.2	1.7	1.2	0.9	0.4
12	—	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	—	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	—	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	—	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	—	—	4.9	3.7	2.9	2.2	1.7	0.9
17	—	—	5.3	4	3.1	2.4	1.8	1.1
18	—	—	5.7	4.4	3.4	2.6	2	1.2
19	—	—	6.1	4.7	3.6	2.8	2.2	1.4
20	—	—	6.6	5.1	4	3.1	2.4	1.5
21	—	—	7	5.4	4.3	3.3	2.7	1.7
22	—	—	8	6.1	4.8	3.8	3	2
23	—	—	9	6.8	5.4	4.3	3.4	2.3
24	—	—	10	7.6	6	4.8	3.9	2.6
25	—	—	11.4	8.4	6.8	5.4	4.4	3
26	—	—	12.6	9.4	7.4	5.9	4.9	3.3
27	—	—	—	10.3	8.1	6.4	5.3	3.6
28	—	—	—	11.3	8.8	7.1	5.8	4
29	—	—	—	12.5	9.6	7.7	6.3	4.3
30	—	—	—	—	11.4	9	7.4	—
31	—	—	—	—	12.9	10	8.2	—

Table 1–26 lists HardCopy IV GX transceiver jitter specifications for all supported protocols.

Table 1–26. HardCopy IV GX Transceiver Block Jitter Specification (Note 1), (2) (Part 1 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
SONET/SDH Transmit Jitter Generation (3)					
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS23	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS23	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS23	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS23	—	—	0.01	UI
SONET/SDH Receiver Jitter Tolerance (3)					
Jitter tolerance at 622.08Mbps	Jitter frequency = 0.03KHz Pattern = PRBS23	> 15	> 15	> 15	UI
	Jitter frequency = 25KHz Pattern = PRBS24	> 1.5	> 1.5	> 1.5	UI
	Jitter frequency = 250KHz Pattern = PRBS25	> 0.15	> 0.15	> 0.15	UI
Jitter tolerance at 2488.32Mbps	Jitter frequency = 0.06KHz Pattern = PRBS23	> 15	> 15	> 15	UI
	Jitter frequency = 100KHz Pattern = PRBS24	> 1.5	> 1.5	> 1.5	UI
	Jitter frequency = 1MHz Pattern = PRBS25	> 0.15	> 0.15	> 0.15	UI
	Jitter frequency = 10MHz Pattern = PRBS26	> 0.15	> 0.15	> 0.15	UI
Fibre Channel Transmit Jitter Generation (4), (12)					
Total jitter FC-1	Pattern = CRPAT	—	—	0.23	UI
Deterministic jitter FC-1	Pattern = CRPAT	—	—	0.11	UI
Total jitter FC-2	Pattern = CRPAT	—	—	0.33	UI
Deterministic jitter FC-2	Pattern = CRPAT	—	—	0.2	UI
Total jitter FC-4	Pattern = CRPAT	—	—	0.52	UI
Deterministic jitter FC-4	Pattern = CRPAT	—	—	0.33	UI
Fibre Channel Receiver Jitter Tolerance (4), (13)					
Deterministic jitter FC-1	Pattern = CJTPAT		> 0.37		UI
Random jitter FC-1	Pattern = CJTPAT		> 0.31		UI
Sinusoidal jitter FC-1	Fc/25000		> 1.5		UI
	Fc/1667		> 0.1		UI
Deterministic jitter FC-2	Pattern = CJTPAT		> 0.33		UI

Table 1-26. HardCopy IV GX Transceiver Block Jitter Specification (Note 1), (2) (Part 2 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
Random jitter FC-2	Pattern = CJTPAT		> 0.29		UI
Sinusoidal jitter FC-2	Fc/25000		> 1.5		UI
	Fc/1667		> 0.1		UI
Deterministic jitter FC-4	Pattern = CJTPAT		> 0.33		UI
Random jitter FC-4	Pattern = CJTPAT		> 0.29		UI
Sinusoidal jitter FC-4	Fc/25000		> 1.5		UI
	Fc/1667		> 0.1		UI
XAUI Transmit Jitter Generation (5)					
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	UI
XAUI Receiver Jitter Tolerance (5)					
Total jitter	—		> 0.65		UI
Deterministic jitter	—		> 0.37		UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1		UI
PCI Express Transmit Jitter Generation (6)					
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	UI
Total jitter at 5 Gbps (Gen2)	Compliance pattern	—	—	—	UI
PCI Express Receiver Jitter Tolerance (6)					
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6		UI
Total jitter at 2.5 Gbps (Gen2)	Compliance pattern	—	—	—	UI
Serial RapidIO Transmit Jitter Generation (7)					
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	UI
Serial RapidIO Receiver Jitter Tolerance (7)					
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.37		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.55		UI

Table 1–26. HardCopy IV GX Transceiver Block Jitter Specification (Note 1), (2) (Part 3 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 8.5		UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1		UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1		UI
GIGE Transmit Jitter Generation (8)					
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	UI
GIGE Receiver Jitter Tolerance (8)					
Deterministic jitter (peak-to-peak)	Pattern = CJPAT		> 0.4		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.66		UI
HiGig Transmit Jitter Generation (9)					
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
HiGig Receiver Jitter Tolerance (9)					
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
	Jitter Frequency = 1.875 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI

Table 1–26. HardCopy IV GX Transceiver Block Jitter Specification (Note 1), (2) (Part 4 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
(OIF) CEI Transmitter Jitter Generation (10)					
Total jitter (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS15 BER = 10exp-12	—	—	—	UI
(OIF) CEI Receiver Jitter Tolerance (10)					
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-12	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-13	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-12	—	—	—	UI
	Jitter Frequency = 3.82 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-12	—	—	—	UI
	Jitter Frequency = 20 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-12	—	—	—	UI
SDI Transmitter Jitter Generation (11)					
Alignment jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.2	—	—	UI
	Data Rate = 2.97 Gbps (3G) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.3	—	—	UI
SDI Receiver Jitter Tolerance (11)					
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar		> 2		UI
	Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar		> 0.3		UI
	Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar		> 0.3		UI

Table 1–26. HardCopy IV GX Transceiver Block Jitter Specification (Note 1), (2) (Part 5 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 1		UI
	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 0.2		UI
	Jitter Frequency = 148.5 MHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 0.2		UI

Notes to Table 1–26:

- (1) Dedicated `refclk` pins drive the input reference clocks.
- (2) Jitter numbers specified are valid for the stated conditions only.
- (3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
- (4) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.1.0.
- (5) The jitter number for XAUI are compliant to the IEEE802.3ae-2002 Specification.
- (6) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
- (7) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
- (8) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (9) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
- (10) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
- (11) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
- (12) The fibre channel transmitter jitter generation numbers are compliant to the specification at δ_T interoperability point.
- (13) The fibre channel receiver jitter tolerance numbers are compliant to the specification at δ_R interoperability point.

Core Performance Specifications

This section describes the clock tree, PLL, DSP, TriMatrix, and configuration and JTAG specifications.

Clock Tree Specifications

Table 1–27 lists clock tree performance specifications for the logic array, DSP blocks, and TriMatrix memory blocks for HardCopy IV devices.

Table 1–27. HardCopy IV Clock Tree Performance—Preliminary (Note 1)

Device	Commercial Grade (MHz)	Unit
HC4E25	600	MHz
HC4E35	600	MHz

Note to Table 1–27:

- (1) Pending silicon characterization.

PLL Specifications

Table 1–28 describes the HardCopy IV PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C). For a PLL block diagram, refer to Figure 1–8 on page 1–38.

Table 1–28. HardCopy IV PLL Specifications—Preliminary (Part 1 of 2) (Note 1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	5	—	717 (2)	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating range	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	—	—	600 (3)	MHz
f_{OUT_EXT}	Output frequency for external clock input (–3 speed grade)	—	—	717 (3)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chain	—	—	—	scanclk cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	—	—	scanclk cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device power	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (8)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on a reset signal	10	—	—	ns
t_{INCCJ} (4), (5)	Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} (6)	Period jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC} (6)	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} (6)	Period Jitter for clock output on regular IO ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for clock output on regular IO ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} (6)	Cycle-to-cycle jitter for clock output on regular IO ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle jitter for clock output on regular IO ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)

Table 1-28. HardCopy IV PLL Specifications—Preliminary (Part 2 of 2) (Note 1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{CASC_OUTPJ_DC}}$ (5), (6)	Period Jitter for dedicated clock output in cascaded PLLs ($F_{\text{OUT}} \geq 100$ MHz)	—	—	250	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs ($F_{\text{OUT}} < 100$ MHz)	—	—	25	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for duration of 100 us	—	—	± 10	%

Notes to Table 1-28:

- (1) Pending silicon characterization.
- (2) This specification is limited in Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (3) This specification is limited by the lower of the two: I/O F_{MAX} or F_{OUT} of the PLL.
- (4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 120 ps.
- (5) F_{REF} is f_{IN}/N when $N = 1$.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1-38.
- (7) The cascaded PLL specification is only applicable in Upstream PLL ($0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$ MHz) and Downstream PLL (Downstream PLL BW > 2 MHz) conditions.
- (8) High bandwidth PLL settings are not supported in external feedback mode.

DSP Block Specifications

Table 1-29 describes the HardCopy IV DSP block performance specifications.

Table 1-29. HardCopy IV DSP Block Performance Specifications—Preliminary (Note 1), (2)

Mode	Number of Multipliers	Max	Unit
9 × 9-bit multiplier	1	410	MHz
12 × 12-bit multiplier	1	410	MHz
18 × 18-bit multiplier	1	495	MHz
36 × 36-bit multiplier	1	365	MHz
18 × 18-bit multiply accumulator	4	390	MHz
18 × 18-bit multiply adder	4	405	MHz
18 × 18-bit multiply adder-signed full precision	2	405	MHz
18 × 18-bit multiply adder with loopback (3)	2	405	MHz
36-bit shift (32 bit data)	1	390	MHz
Double mode	1	365	MHz

Notes to Table 1-29:

- (1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.
- (2) Pending silicon characterization.
- (3) Maximum is for non-pipelined block with loopback input registers disabled and **Round** and **Saturation** disabled.

TriMatrix Memory Block Specifications

Table 1-30 lists the HardCopy IV TriMatrix memory block specifications.

Table 1-30. HardCopy IV TriMatrix Memory Block Performance Specifications - Preliminary (Note 1) (Part 1 of 2)

Memory	Mode	TriMatrix Memory	Performance (Flipchip Package)		Performance (Wirebond Package)		Unit
			Commercial Speed Grade	Industrial Speed Grade	Commercial Speed Grade	Industrial Speed Grade	
MLAB	Single port 16 × 10	1	500	500	375	375	MHz
	Simple dual-port 16 × 20	1	500	500	375	375	MHz
	ROM 64 × 10	1	500	500	375	375	MHz
	ROM 32 × 20	1	500	500	375	375	MHz
M9K	Single-port 8K × 1	1	540	540	378	378	MHz
	Single-port 4K × 2 or 2K × 4	1	540	540	378	378	MHz
	Single-port 1K × 9, 512 × 18, or 256 × 36	1	540	540	378	378	MHz
	Simple dual-port, 8K × 1	1	490	490	343	343	MHz
	Simple dual-port, 4K × 2 or 2K × 4	1	490	490	343	343	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36	1	490	490	343	343	MHz
	Simple dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to "Old Data"	1	340	340	238	238	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36 with the read-during-write option set to "Old Data"	1	340	340	238	238	MHz
	True dual-port, 8K × 1	1	430	430	301	301	MHz
	True dual-port, 4K × 2 or 2K × 4	1	430	430	301	301	MHz
	True dual-port, 1K × 9 or 512 × 18	1	430	430	301	301	MHz
	True dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to "Old Data"	1	335	335	235	235	MHz
	True dual-port, 1K × 9 or 512 × 18 with the read-during-write option set to "Old Data"	1	335	335	235	235	MHz
	ROM 1P, 8K × 1, 4K × 2, or 2K × 4	1	540	540	378	378	MHz

Table 1-30. HardCopy IV TriMatrix Memory Block Performance Specifications - Preliminary (Note 1) (Part 2 of 2)

Memory	Mode	TriMatrix Memory	Performance (Flipchip Package)		Performance (Wirebond Package)		Unit
			Commercial Speed Grade	Industrial Speed Grade	Commercial Speed Grade	Industrial Speed Grade	
M9K	ROM 1P, 1K × 9, 512 × 18, or 256 × 36	1	540	540	378	378	MHz
	ROM 2P, 8K × 1, 4K × 2, or 2K × 4	1	540	540	378	378	MHz
	ROM 2P, 1K × 9, or 512 × 18	1	540	540	378	378	MHz
	Min Pulse Width (Clock High Time)	—	800	800	1067	1067	ps
	Min Pulse Width (Clock Low Time)	—	625	625	469	469	ps
M144K	True dual-port 16K × 9 or 8K × 18	1	375	350	263	245	MHz
	True dual-port 4K × 36	1	375	350	263	245	MHz
	Simple dual-port 16K × 9 or 8K × 18	1	435	375	305	263	MHz
	Simple dual-port 4K × 36 or 2K × 72	1	435	375	305	263	MHz
	ROM 1 Port	1	500	450	350	315	MHz
	ROM 2 Port	1	465	425	326	298	MHz
	Single-port 16K × 9 or 8K × 18	1	440	400	308	280	MHz
	Single-port 4K × 36	1	440	400	308	280	MHz
	True dual-port 16K × 9, 8K × 18, or 4K × 36 with the read-during-write option set to "Old Data"	1	230	225	161	158	MHz
	Simple dual-port 16K × 9, 8K × 18, 4K × 36, or 2K × 72 with the read-during-write option set to "Old Data"	1	240	225	168	156	MHz
	Simple dual-port 2K × 64 (with ECC)	1	300	295	210	207	MHz
	Min Pulse Width (Clock High Time)	—	1382	1382	1843	1843	ps
	Min Pulse Width (Clock Low Time)	—	625	690	833	920	ps

Note to Table 1-30:

(1) Pending silicon characterization.

JTAG Specification

Table 1–31 lists the JTAG timing parameters and values for HardCopy IV devices. For JTAG timing requirements, refer to the “High-speed I/O Block” row in Table 1–39 on page 1–36.

Table 1–31. HardCopy IV JTAG Timing Parameters and Values—Preliminary

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU (TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (1)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (1)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (1)	ns

Note to Table 1–31:

- (1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, $t_{JPCO} = 12$ ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface, and OCT calibration block specifications.

High-Speed I/O Specification

Table 1–32 shows the high-speed I/O timing for HardCopy IV devices.

Table 1–32. High-Speed I/O Specifications—Preliminary (Part 1 of 2) (Note 1), (2), (3)

Symbol	Conditions	FlipChip			Wirebond		
		Min	Typ	Max	Min	Typ	Max
Transmitter							
Dedicated LVDS— f_{HSDR} (data rate)	SERDES factor J = 3 to 10	150	—	1250	150	—	840
	SERDES factor J = 2, uses DDR registers	(5)	—	1250	(5)	—	840
	SERDES factor J = 1, uses SDR register	(5)	—	717	(5)	—	450
LVDS_E_3R— $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10	(5)	—	1000	(5)	—	640
LVDS_E_1R— $f_{HSDRDPA}$ (data rate)		(5)	—	200	(5)	—	170
t_x Jitter	Total Jitter for data rate, 600 Mbps - 1.6G bps	—	—	160	—	—	160
	Total Jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1
t_{DUTY}	Tx output clock duty cycle	45	50	55	45	50	55

Table 1-32. High-Speed I/O Specifications—Preliminary (Part 2 of 2) (Note 1), (2), (3)

Symbol	Conditions	FlipChip			Wirebond		
		Min	Typ	Max	Min	Typ	Max
t_{RISE} and t_{FALL}	Dedicated LVDS	—	—	200	—	200	—
	LVDS_E_3R	—	—	350	—	350	—
	LVDS_E_1R	—	—	500	—	500	—
TCCS	Dedicated LVDS	—	—	100	—	—	200
	LVDS_E_3R/ LVDS_E_1R	—	—	250	—	—	250
Receiver							
$f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10	150	—	1250	150	—	840
DPA Mode							
DPA run length	—	—	—	10000	—	—	10000
Soft CDR mode							
Soft-CDR PPM tolerance	—	—	—	300	—	—	
Non DPA Mode							
Sampling Window	All differential I/O standards	—	—	300	—	—	400

Notes to Table 1-32:

- (1) Numbers are preliminary pending characterization.
- (2) When J = 3 to 10, the SERDES block is used.
- (3) When J = 1 or 2, the SERDES block is bypassed.
- (4) Clock boost factor (Ω) is the ratio between the input data rate to the input clock rate.
- (5) The minimum specification is dependent on the clock source (for example, PLL and clock pin) and the clock routing resource (global, regional, or local) is used.
- (6) Pending silicon characterization.

Table 1-33 lists the DPA lock time specifications for HardCopy IV devices.

Table 1-33. DPA Lock Time Specifications—Preliminary (Note 1), (2), (3)

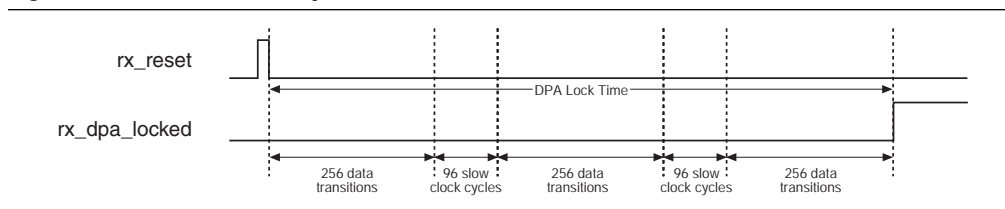
Standard	Training Pattern	Number of Data Transitions in one repetition of training pattern	Number of repetition per 256 data transition (4)	Condition	Min	Typ	Max
SPI-4	00000000001111111111	2	128	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles (5), (6)	—	—
Parallel Rapid I/O	00001111	2	128	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles (5), (6)	—	—
	10010000	4	64	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles (5), (6)	—	—
Misc.	10101010	8	32	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles (5), (6)	—	—
	01010101	8	32	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles (5), (6)	—	—

Notes to Table 1-33:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in the table applies to both commercial and industrial grade.
- (4) This is the number of repetition for the stated training pattern to achieve 256 data transitions.
- (5) Slow clock = data rate (MHz)/deserialization factor.
- (6) The DPA lock time with **DPA PLL Calibration** enabled is preliminary.

Figure 1-4 shows the DPA lock time specifications with DPA PLL calibration enabled.

Figure 1-4. DPA Lock Time Specification with DPA PLL Calibration Enabled



External Memory I/O Timing Specifications

Table 1–34 and Table 1–35 list HardCopy IV device timing uncertainties on the read and write data paths. Use these specifications to determine timing margins for source synchronous paths between a HardCopy IV device and an external memory device.

Refer to “SW (sampling window)” in Table 1–39 on page 1–36.

Table 1–34. Sampling Window (SW) - Read Side—Preliminary (Note 1)

Location (2)	Memory Type	Sampling Window (ps)	
		Setup	Hold
VIO	DDR3 (> 400 MHz) (3)	282	56
	DDR3	344	85
	DDR2	213	162
	DDR1	236	178
	QDRII/II+	218	203
	RLDRAM II (> 333 MHz) (4)	198	183
HIO	DDR3 (> 400 MHz) (3)	282	56
	DDR3	344	85
	DDR2	213	162
	DDR1	236	178
	QDRII/II+	218	203
	RLDRAM II (> 333 MHz) (4)	198	183

Note to Table 1–34:

- (1) Pending silicon Characterization.
- (2) VIO (vertical I/O) refers to I/Os in the top and bottom banks; HIO (horizontal I/O) refers to I/Os in the left and right banks.
- (3) Pending IP support. Actual achievable performance is based on design and system-specific factors. For DDR3 > 400 MHz support, contact Altera.
- (4) Pending IP support. Actual achievable performance is based on design and system-specific factors. For RLDRAM II > 333 MHz support, contact Altera.

Table 1–35. Transmitter Channel-to-Channel Skew (TCCS)—Write Side (Part 1 of 2) (Note 1)

Location (2)	Memory Type	TCCS (ps)	
		Lead	Lag
VIO	DDR3 (> 400 MHz) (3)	234	286
	DDR3	344	347
	DDR2	270	380
	DDR1	275	396
	QDRII/II+	294	408
	RLDRAM II (> 333 MHz) (4)	346	356

Table 1-35. Transmitter Channel-to-Channel Skew (TCCS)—Write Side (Part 2 of 2) (Note 1)

Location (2)	Memory Type	TCCS (ps)	
		Lead	Lag
HIO	DDR3 (> 400 MHz) (3)	282	56
	DDR3	344	347
	DDR2	270	380
	DDR1	275	396
	QDRII/II+	294	408
	RLDRAM II (> 333 MHz) (4)	346	356

Notes to Table 1-35:

- (1) Pending silicon characterization.
- (2) VIO (vertical I/O) refers to I/Os in the top and bottom banks; HIO (horizontal I/O) refers to I/Os in the left and right banks.
- (3) Pending IP support. Actual achievable performance is based on design and system-specific factors. For DDR3 > 400 MHz support, contact Altera.
- (4) Pending IP support. Actual achievable performance is based on design and system-specific factors. For RLDRAM II > 333 MHz support, contact Altera.

DLL and DQS Logic Block Specifications

Table 1-36 describes the delay-locked loop (DLL) frequency range specifications for HardCopy IV devices.

Table 1-36. HardCopy IV DLL Frequency Range Specifications—Preliminary (Note 1)

Frequency Mode	Frequency Range (MHz)	Available Phase Shift	DQS Delay Buffer Mode (2)	Number of Delay Chains
0	90 to 140	45°, 90°, 135°, 180°	Low	16
1	120 to 190	30°, 60, 90°, 120°	Low	12
2	150 to 230	36°, 72°, 108°, 144°	Low	10
3	180 to 290	45°, 90°, 135°, 180°	Low	8
4	240 to 350	30°, 60, 90°, 120°	High	12
5	290 to 420	36°, 72°, 108°, 144°	High	10
6	360 to 540 (3)	45°, 90°, 135°, 180°	High	8

Note to Table 1-36:

- (1) Pending silicon characterization
- (2) Low indicates 6-bit DQS delay setting, high indicates 5-bit DQS delay setting.
- (3) Frequency > 530 MHz on Mode 6 is to for 533 MHz DDR3 support. Pending IP support. Actual achievable performance is based on design and system-specific factors. For DDR3 > 400 MHz, contact Altera.

OCT Calibration Block Specifications

Table 1-37 describes the OCT calibration block specifications for HardCopy IV devices.

Table 1-37. OCT Calibration Block Specifications—Preliminary

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R _S /R _T calibration	—	1000	—	Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	28	—	Cycles
T _{RS_RT}	Time required to dynamically switch from R _S to R _T	—	2.5	—	ns

Duty Cycle Distortion (DCD) Specifications

Table 1-38 lists the worst case DCD for HardCopy IV devices.

Table 1-38. DCD on HardCopy IV I/O Pins—Preliminary

Symbol	Min	Max	Unit
Output Duty Cycle	45	55	%

I/O Timing

Altera offers the Excel-based I/O Timing spreadsheet and the Quartus II TimeQuest Timing Analyzer to determine I/O timing.

Excel-based I/O Timing spreadsheet provides pin timing performance for each device density and speed grade. Use the data before designing the HardCopy device to get an estimate of the timing budget as part of the link timing analysis. The TimeQuest analyzer provides a more accurate and precise I/O timing data based on the specifics of your design after completing placement and routing.



You can download the Excel-based I/O Timing spreadsheet from the [HardCopy IV Devices Literature](#) web page.

Glossary

Table 1-39 shows the glossary for this chapter.

Table 1-39. Glossary Table (Part 1 of 5)

Letter	Subject	Definitions
A	—	—
B	—	—
C	—	—

Table 1-39. Glossary Table (Part 2 of 5)

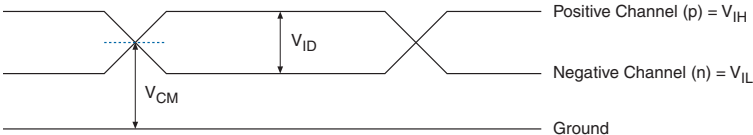
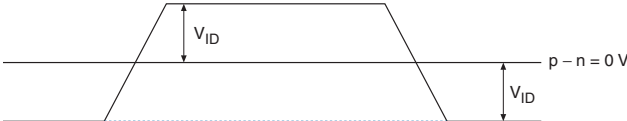
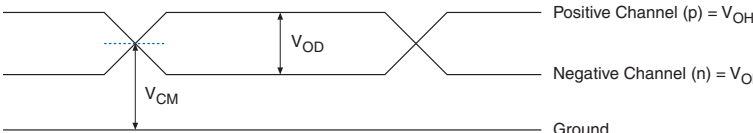
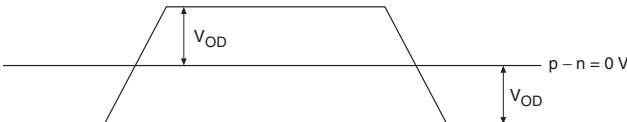
Letter	Subject	Definitions
D	Differential I/O Standards	<p>Figure 1-5. Receiver Input Waveforms</p> <p>Single-Ended Waveform</p>  <p>Differential Waveform</p>  <p>Figure 1-6. Transmitter Output Waveforms</p> <p>Single-Ended Waveform</p>  <p>Differential Waveform</p> 
		E
F	f_{HSCLK}	Left/Right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{\text{HSDR}} = 1/\text{TUI}$), non-DPA.
	$f_{\text{HS DRDPA}}$	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{\text{HS DRDPA}} = 1/\text{TUI}$), DPA.
G	—	—
H	—	—
I	—	—

Table 1-39. Glossary Table (Part 3 of 5)

Letter	Subject	Definitions
J	JTAG Timing Specifications	<p>High-speed I/O block: Deserialization factor (width of parallel data bus).</p> <p>Figure 1-7. JTAG Timing Specifications</p>
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Specifications	<p>Figure 1-8 shows the PLL specification parameters:</p> <p>Figure 1-8. Diagram of PLL Specifications (1)</p> <p>Note to Figure 1-8: (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p>
Q	—	—
R	R _L	Receiver differential input discrete resistor (external to HardCopy IV device).

Table 1-39. Glossary Table (Part 4 of 5)

Letter	Subject	Definitions
S	SW (sampling window)	<p>The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown in Figure 1-9:</p> <p>Figure 1-9. Timing Diagram</p>
	Single-ended voltage referenced I/O standard	<p>The JEDEC standard for SSTI and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown in Figure 1-10:</p> <p>Figure 1-10. Single-Ended Voltage Referenced I/O Standard</p>
T	t_c	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{co} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under S in this table).
	t_{DUTY}	High-speed I/O block: Duty cycle on high-speed transmitter output clock. Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_c/w$)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on PLL clock input
	t_{OUTPJ_IO}	Period jitter on general purpose I/O driven by a PLL
	t_{OUTPJ_DC}	Period jitter on dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20-80%)	
U	—	—

Table 1-39. Glossary Table (Part 5 of 5)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage: Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
V_{OX}	Output differential cross point voltage	
W	W	High-speed I/O block: Clock boost factor
X	—	—
Y	—	—
Z	—	—

Document Revision History

Table 1-40 shows the revision history for this chapter.

Table 1-40. Document Revision History

Date	Version	Changes
January, 2011	2.0	<ul style="list-style-type: none"> ■ Updated Table 1-5, Table 1-20, Table 1-21, Table 1-22, Table 1-23, Table 1-28, Table 1-30, and Table 1-32. ■ Added Table 1-24. ■ Removed “External Memory Interface Specifications” section. ■ Updated “I/O Timing” section. ■ Made general formatting update.
March, 2010	1.0	Metadata corrected. No changes made to document.
June, 2009	1.0	Initial release.