

### Introduction

HardCopy® APEX™ devices enable high-density APEX 20KE device technology to be used in high-volume applications where significant cost reduction is desired. HardCopy APEX devices are physically and functionally compatible with APEX 20KC and APEX 20KE devices. They combine the time-to-market advantage, performance, and flexibility of APEX 20KE devices with the ability to move to high-volume, low-cost devices for production. The migration process from an APEX 20KE device to a HardCopy APEX device is fully automated, with designer involvement limited to providing a few Quartus® II software-generated output files.

### Features...

HardCopy APEX devices are manufactured using an 0.18- $\mu\text{m}$  CMOS six-layer-metal process technology:

- Preserves functionality of a configured APEX 20KC or APEX 20KE device
- Pin-compatible with APEX 20KC or APEX 20KE devices
- Meets or exceeds timing of configured APEX 20KE and APEX 20KC devices
- Optional emulation of original programmable logic device (PLD) programming sequence
- High-performance, low-power device
- MultiCore architecture integrating embedded memory and look-up table (LUT) logic used for register-intensive functions
- Embedded system blocks (ESBs) used to implement memory functions, including first-in first-out (FIFO) buffers, dual-port RAM, and content-addressable memory (CAM)
- Customization performed through metallization layers

High-density architecture:

- 400,000 to 1.5 million typical gates (Table 7-1)
- Up to 51,840 logic elements (LEs)
- Up to 442,368 RAM bits that can be used without reducing available logic

**Table 7-1. HardCopy APEX Device Features** *Note (1)*

Feature	HC20K400	HC20K600	HC20K1000	HC20K1500
Maximum system gates	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	400,000	600,000	1,000,000	1,500,000
LEs	16,640	24,320	38,400	51,840
ESBs	104	152	160	216
Maximum RAM bits	212,992	311,296	327,680	442,368
Phase-locked loops (PLLs)	4	4	4	4
Maximum macrocells	1,664	2,432	2,560	3,456
Maximum user I/O pins	488	588	708	808

**Note to Table 7-1:**

- (1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

## ...and More Features

Low-power operation:

- 1.8-V supply voltage (Table 7-2)
- MultiVolt I/O support for 1.8-, 2.5-, and 3.3-V interfaces
- ESBs offering power-saving mode

Flexible clock management circuitry with up to four phase-locked loops (PLLs):

- Built-in low-skew clock tree
- Up to eight global clock signals
- ClockLock feature reducing clock delay and skew
- ClockBoost feature providing clock multiplication and division
- ClockShift feature providing clock phase and delay shifting

Powerful I/O features:

- Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits

- Support for high-speed external memories, including double-data rate (DDR), synchronous dynamic RAM (SDRAM), and zero-bus-turnaround (ZBT) static RAM (SRAM)
- 16 input and 16 output LVDS channels
- Fast  $t_{CO}$  and  $t_{SU}$  times for complex logic
- MultiVolt I/O support for 1.8-V, 2.5-V, and 3.3-V interfaces
- Individual tri-state output enable control for each pin
- Output slew-rate control to reduce switching noise
- Support for advanced I/O standards, including LVDS, LVPECL, PCI-X, AGP, CTT, SSTL-3 and SSTL-2, GTL+, and HSTL Class I
- Supports hot-socketing operation

**Table 7-2. HardCopy APEX Device Supply Voltages**

Feature	Voltage
Internal supply voltage ( $V_{CCINT}$ )	1.8 V
MultiVolt I/O interface voltage levels ( $V_{CCIO}$ )	1.8 V, 2.5 V, 3.3 V, 5.0 V (1)

**Note to Table 7-2:**

- (1) HardCopy APEX devices can be 5.0-V tolerant by using an external resistor.

HardCopy APEX device implementation features:

- Customized interconnect for each design
- HardCopy APEX devices preserve APEX 20K device MegaLAB structure, LEs, ESBs, I/O element (IOE), PLLs, and LVDS circuitry
- Up to four metal layers customizable for customer designs
- Completely automated proprietary design migration flow
  - Testability analysis and fix
  - Automatic test pattern generation (ATPG)
  - Automatic place and route
  - Static timing analysis
  - Static functional verification
  - Physical verification

Tables 7-3 through 7-6 show the HardCopy APEX device ball-grid array (BGA) and FineLine BGA package options, I/O counts, and sizes.

**Table 7-3. HardCopy APEX Device BGA Package Options and I/O Count**  
*Note (1)*

Device	652-Pin BGA
HC20K400	488
HC20K600	488
HC20K1000	488
HC20K1500	488

**Table 7-4. HardCopy APEX Device FineLine BGA Package Options and I/O Count**  
*Note (1)*

Device	672-Pin	1,020-Pin
HC20K400	488	–
HC20K600	508	588
HC20K1000	508	708
HC20K1500	–	808

*Note to Tables 7-3 and 7-4:*

- (1) I/O counts include dedicated input and clock pins.

**Table 7-5. HardCopy APEX Device BGA Package Sizes**

Feature	652-Pin BGA
Pitch (mm)	1.27
Area (mm <sup>2</sup> )	2,025
Length × width (mm × mm)	45.0 × 45.0

**Table 7-6. HardCopy APEX Device FineLine BGA Package Sizes**

Feature	672-Pin	1,020-Pin
Pitch (mm)	1.00	1.00
Area (mm <sup>2</sup> )	729	1,089
Length × width (mm × mm)	27 × 27	33 × 33

## Document Revision History

Table 7-7 shows the revision history for this chapter.

<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
September 2008, v2.3	Updated chapter number and metadata.	—
June 2007, v2.2	Minor text edits.	—
December 2006 v2.1	Updated revision history.	—
March 2006	Formerly chapter 9; no content change.	—
January 2005 v2.0	Update device names and other minor textual changes	—
June 2003 v1.0	Initial release of Chapter 9, <i>Introduction to HardCopy APEX Devices</i> , in the <i>HardCopy Device Handbook</i>	—

