6. I/O Assignment Analysis

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Introduction

Today's FPGAs support multiple I/O standards and have high pin counts. You must be able to make pin assignments efficiently for designs in these advanced devices. You also need the ability to easily check the legality of the pin assignments to ensure that the pin-out does not violate any board layout guidelines such as pin spacing and current consumption limitations.

This chapter describes a design flow that includes making and analyzing pin assignments using the **Start I/O Assignment Analysis** command in the Quartus® II software, during and after the development of your HDL design.

The **Start I/O Assignment Analysis** command allows you to check your I/O assignments early in the design process. You can use this command to check the legality of pin assignments before, during, or after compilation of your design. If design files are available, you can use this command to perform more thorough legality checks on your design's I/O pins and surrounding logic. These checks include proper reference voltage pin usage, valid pin location assignments, and acceptable mixed I/O standards.

The **Start I/O Assignment Analysis** command can be used for designs targeting Stratix® II, Stratix, Stratix GX, Cyclone™ II, Cyclone, and MAX® II device families.

I/O Assignment Analysis Design Flows

The I/O assignment analysis design flows depend on whether your project contains design files, for example:

- When the board layout must be complete before starting the FPGA design, use the flow shown in Figure 6–1 on page 6–3. This flow does not require design files and checks the legality of your pin assignments.
- With a complete design, use the flow shown in Figure 6–3 on page 6–5. This flow thoroughly checks the legality of your pin assignments against any design files provided. For more information on creating assignments, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Each flow involves creating pin assignments, running the analysis, and reviewing the report file.

You should run the analysis each time you add or modify a pin-related assignment. You can use the **Start I/O Assignment Analysis** command repeatedly since it completes in a short time.

The analysis checks pin assignments and surrounding logic for illegal assignments and violations of board layout rules. For example, the analysis checks whether your pin location supports the I/O standard assigned, current strength, supported V_{REF} voltages, and whether a PCI diode is permitted.

Along with the pin-related assignments, the **Start I/O Assignment Analysis** command also checks blocks that directly feed or are fed by resources such as a phase-locked loops (PLLs), low-voltage differential signals (LVDS), or gigabit transceiver blocks.

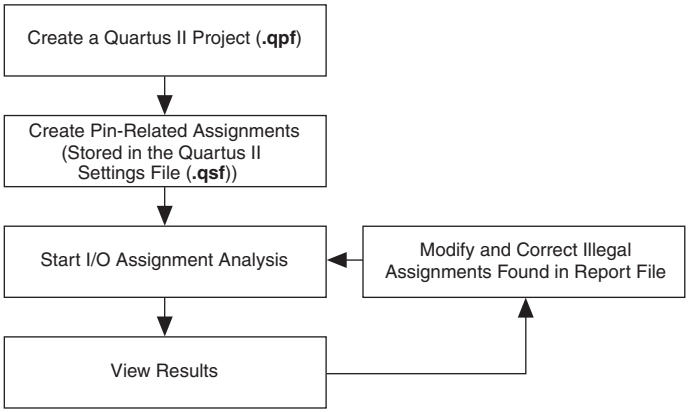
Design Flow Without Design Files

During the early stages of development of an FPGA device, board layout engineers may request preliminary or final pin-outs. It is time consuming to manually check to see whether the pin-outs violate any design rules. Instead, you can use the **Start I/O Assignment Analysis** command to quickly perform basic checks on the legality of your pin assignments.

Without a complete design, the analysis performs limited checks and cannot guarantee that your assignments do not violate design rules.

The I/O assignment analysis command is able to perform limited checks against pin assignments made in a Quartus II project that has a device specified, but may not yet include any HDL design files. For example, you can create a Quartus II project with only a target device specified and create pin-related assignments based on circuit board layout considerations that are already determined. Even though the Quartus II project does not yet contain any design files, you can reserve input and output pins and make pin-related assignments to each pin using the Assignment Editor. After you assign an I/O standard to each reserved pin, you run the I/O assignment analysis to ensure that there are no I/O standard conflicts in each I/O bank.

Figure 6–1. Assigning & Analyzing Pin-Outs Without Design Files



You can assign and analyze pin-outs using the **Start I/O Assignment Analysis** command without design files by following these steps:

1. In the Quartus II software, create a project.
2. Use the **Assignment Editor**, **Pin Planner**, or a Tcl script to create pin locations and related assignments. For the I/O assignment analysis to determine the type of pin, you must reserve your I/O pins. Refer to "Reserving Pins" on page 6–9.
3. Choose **Start > Start I/O Assignment Analysis** (Processing menu) to start the analysis.

For information on using a Tcl script or command prompt to start the analysis, refer to "Scripting Support" on page 6–13.

4. View the messages in the **Compilation Report** window, Fitter report file (<*project name*>.**fit**.**rpt**), or in the **Messages** window.
5. Correct any errors and violations reported by the I/O assignment analysis.

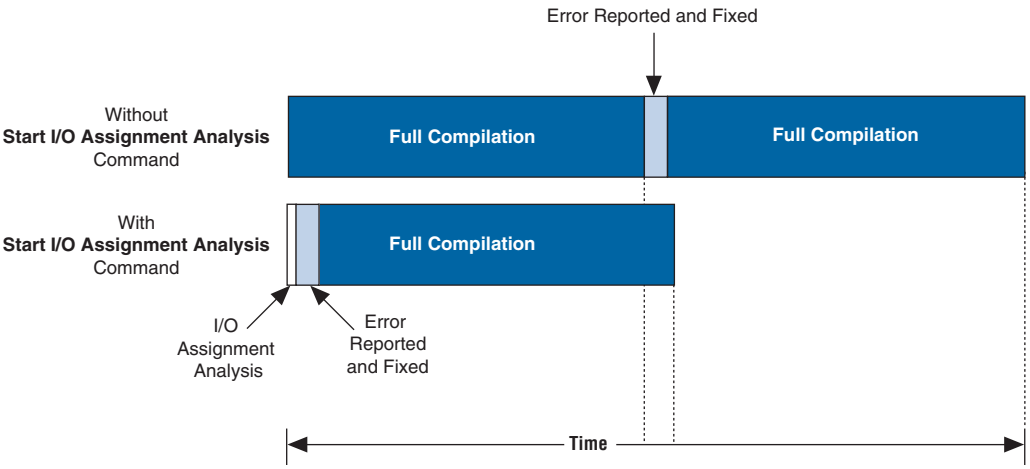
Repeat steps 1 through 5 above until all errors are corrected.

Design Flow with Design Files

During a full compilation, the Quartus II software does not report illegal pin assignments until the fitter stage. To validate pin assignments sooner, you can run the **Start I/O Assignment Analysis** command after

performing analysis and synthesis and before performing a full compilation. Typically, the analysis takes a short time. Figure 6–2 shows the benefits of using the **Start I/O Assignment Analysis** command.

Figure 6–2. Saving Compilation Time with the Start I/O Assignment Analysis Command

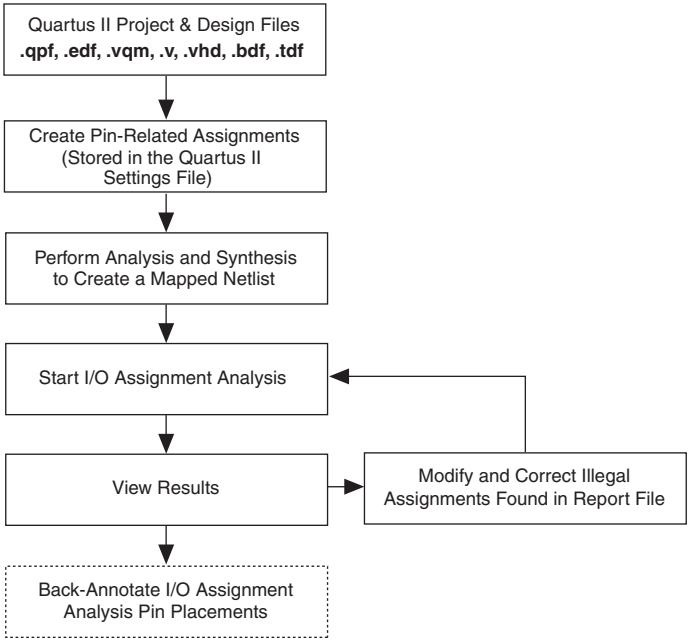


The rules that are checked by the I/O assignment analysis depend on the completeness of the design. With a complete design, the **Start I/O Assignment Analysis** command thoroughly checks the legality of all pin-related assignments. With a partial design, which can just be the top-level wrapper file, the **Start I/O Assignment Analysis** command checks the legality of those pin-related assignments for which it has enough information.

For example, you might assign a clock to a user I/O pin instead of assigning it to a dedicated clock pin, or you design the clock to drive a PLL that has not yet been instantiated in the design. Because the **Start I/O Assignment Analysis** command is unaware of the logic that the pin drives, it is not able to check that only a dedicated clock input pin can drive the clock port of a PLL.

Analyze as much of the design as possible, especially logic that connects to pins, to obtain better coverage. For example, if your design includes PLLs or LVDS blocks, you should include these MegaWizard® Plug-In Manager-generated files in your project for analysis.

Figure 6–3. Assigning & Analyzing Pin-Outs With Design Files



To assign and analyze pin-outs using the **Start I/O Assignment Analysis** command with design files, perform the following steps:

1. In the Quartus II software, create a project including your design files.
2. Create pin-related assignments with the **Assignment Editor**.

   You can also create pin-related assignments by importing them from a comma-separated value file (**.csv**), executing Tcl commands, editing the QSF directly, or by dragging and dropping pins to a location in the timing closure floorplan.

3. Choose **Start > Start Analysis & Synthesis** (Processing menu) to generate an internal mapped netlist.

For information on using a Tcl script or command prompt to start the analysis, refer to "Scripting Support" on page 6–13.

4. Choose **Start > Start I/O Assignment Analysis** (Processing menu) to start the analysis.

5. View the messages in the **Compilation Report** or in the **Messages** window.

6. Use the **Assignment Editor** to correct any errors and violations reported.

7. Use the **Start I/O Assignment Analysis** command until all errors are corrected.

I/O Rules Checked by the I/O Assignment Analysis

The effectiveness of the I/O assignment analysis is relative to the completeness of your pin-related assignments and design. To ensure your design functions correctly, include as many design files as possible and all pin-related assignments in your Quartus II project.

Tables 6–1 and 6–2 list a subset of the I/O rule checks performed when you execute an I/O assignment analysis with and without design files. For more detailed information on each I/O rule, please refer to the *Selectable I/O Standards* chapter in the respective device handbook.

Table 6–1. General I/O Related Rules (Part 1 of 2)

Rule	Description	Device *(1)* Families	HDL Required?
I/O bank capacity	Checks the number of pins assigned to an I/O bank against the number of pins allowed in the I/O bank.	All	No
I/O bank V_{CCIO} voltage compatibility	Checks that no more than one `VCCIO` is required from the pins assigned to the I/O bank.	All	No
I/O bank V_{REF} voltage compatibility	Checks that no more than one `VREF` is required from the pins assigned to the I/O bank.	All	No
I/O standard and location conflicts	Checks if the pin location supports the assigned I/O standard.	All	No
I/O standard and signal direction conflicts	Checks if the pin location supports the I/O standard assigned and the direction. For example, certain I/O standards on a particular pin location can only support output pins.	All	No
Differential I/O standards cannot have open drain turned ON	Checks that open drain is turned off for all pins with a differential I/O standard.	All	No
I/O standard and drive strength conflicts	Checks to see if the drive strength assignments is within the specifications of the I/O standard.	All	No
Drive strength and location conflicts	Checks to see if the pin location supports the assigned drive strength.	All	No

Table 6–1. General I/O Related Rules (Part 2 of 2)

Rule	Description	Device (1) Families	HDL Required?
BUSHOLD and location conflicts	Checks if the pin location supports BUSHOLD (e.g., dedicated clock pins do not support BUSHOLD).	All	No
WEAK_PULLUP and location conflicts	Checks if the pin location supports WEAK_PULLUP (for example, dedicated clock pins do not support WEAK_PULLUP)	All	No
Electromigration check	Checks if the combined drive strength of consecutive pads does not exceed a certain limit. For example, the total current drive for 10 consecutive pads on a Stratix II device cannot exceed 200 mA.	All	No
PCI_IO clamp diode, location, and I/O standard conflicts	Checks if the pin location along with the I/O standard assigned supports PCI_IO clamp diode.	All	No
SERDES and I/O pin location compatibility check	Checks that all pins connected to a SERDES in your design are assigned to dedicated SERDES pin locations.	All	Yes
PLL and I/O pin location compatibility check	Checks if pins connected to PLL are assigned to the dedicated PLL pin locations.	All	Yes

Note to Table 6–1:
(1) "All" includes the following device families: Stratix II, Stratix GX, Stratix, Cyclone II, Cyclone, MAX II, and HardCopy® devices.

Table 6–2. SSN Related Rules (Part 1 of 2)

Rule	Description	Device (1) Families	HDL Required?
I/O bank can not have single-ended I/O when DPA exists	Checks that no single-ended I/O pin exists in the same I/O bank as a DPA.	Stratix II, Stratix GX	No
A PLL I/O bank does not support both a single-ended I/O and a differential signal simultaneously	Checks that there are no single-ended I/O pins present in the PLL I/O Bank when a differential signal exists.	Stratix II	No
Single-ended output is required to be a certain distance away from a differential I/O pin	Checks if single-ended output pins are a certain distance away from a differential I/O pin.	All	No
Single-ended output has to be a certain distance away from a VREF pad	Checks if single-ended output pins are a certain distance away from a VREF pad.	Cyclone II, Cyclone	No
Single-ended input is required to be a certain distance away from a differential I/O pin	Checks if single-ended input pins are a certain distance away from a differential I/O pin.	Cyclone II, Cyclone	No

Table 6–2. SSN Related Rules (Part 2 of 2)

Rule	Description	Device (1) Families	HDL Required?
Too many outputs or bidirectional pins in a VREFGROUP when a VREF is used	Checks that there are no more than a certain number of outputs or bidirectional pins in a VREFGROUP when a VREF is used.	All	No
Too many outputs in a VREFGROUP	Checks if too many outputs are in a VREFGROUP.	All	No

Note to Table 6–2:
(1) "All" includes the following device families: Stratix II, Stratix GX, Stratix, Cyclone II, Cyclone, MAX II, and HardCopy devices.

Inputs for I/O Assignment Analysis

The **Start I/O Assignment Analysis** command reads the following inputs:

- Internal mapped netlist
- QSF

The internal mapped netlist is used when you have a partial or complete design. The QSF is always used to read in all pin-related assignments for analysis.

Generating a Mapped Netlist

The **Start I/O Assignment Analysis** command uses a mapped netlist, if available, to identify the pin type and the surrounding logic. The mapped netlist is stored internally in the Quartus II software database.

To generate a mapped netlist, choose **Start > Start Analysis & Synthesis** (Processing menu). You can also use the **quartus_map** executable to run analysis and synthesis.

Type the following at a system command prompt:

```
quartus_map <project name>↵
```

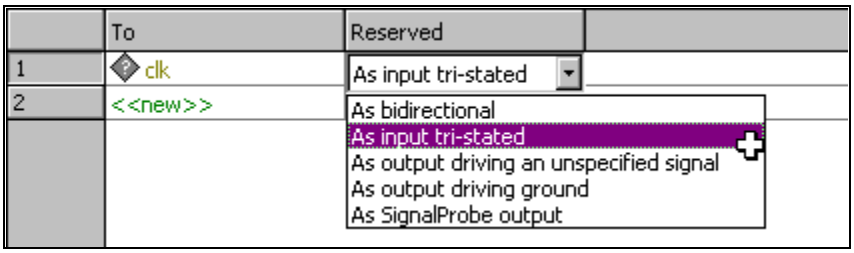
Creating Pin-Related Assignments

The **I/O Assignment Analysis** command reads in a QSF containing all your pin-related assignments. These pin-related assignments include pin settings such as I/O standards, drive strength, and location assignments. The following sections highlight some of the location assignments you can make.

Reserving Pins

If you do not have any design files, you can still reserve pin locations and create pin-related assignments. Reserving pins is necessary so that the **Start I/O Assignment Analysis** command has information about the pin and the pin type (input, output, or bidirectional) and correctly analyzes the pins. You can reserve a pin by choosing **Assignment Editor** (Assignments menu) and selecting **Reserved Pin** from the **Category** list. In the spreadsheet, type in the pin name and select from the **Reserved** list (Figure 6–4).

Figure 6–4. Reserving an Input Pin With the Assignment Editor



For more information on using the Assignment Editor, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

You can also reserve pins using the Pin Planner. For more information on the Pin Planner, refer to the *I/O Planning* chapter in volume 2 of the *Quartus II Handbook*.

Location Assignments

You can create the following types of location assignments for your design and its reserved pins:

- Pin number
- I/O bank
- VREF group
- Edge

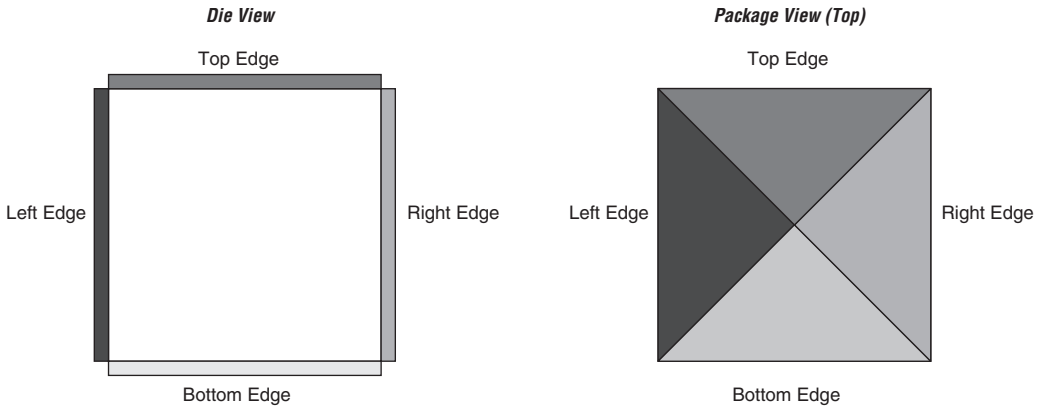
I/O bank, VREF group, and edge location assignments are supported only for Stratix and Cyclone series device families.

You can assign a location to your pins using the Pin Planner or the Assignment Editor. To make a pin location assignment using the Assignment Editor, choose **Assignment Editor** (Assignments menu) and select the **Pin** category from the **Category** list. Type the pin name and select a location from the **Location** list.

It is common to place a group of pins (or bus) with compatible I/O standards in the I/O same bank or VREF group. For example, two buses with two I/O standards 2.5 V and SSTL-II can be placed in the same I/O bank.

An easy way to place large buses that exceed the pins available in a particular I/O bank is to use edge location assignments. You can also use edge location assignments to improve circuit board routing ability of large buses, since they are close together near an edge. Figure 6–5 shows the Altera device package edges.

Figure 6–5. Die View and Package View of the Four Edges on an Altera Device



For more information on using the **Assignment Editor** to create pin-related assignments, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

For more information on using the **Pin Planner** to create pin location assignments, refer to the *I/O Planning* chapter in volume 2 of the *Quartus II Handbook*.

Suggested & Partial Placement

The **Start I/O Assignment Analysis** command automatically assigns suggested pin locations to unassigned pins in your design so it can perform pin legality checks. For example, if you assign an edge location to a group of LVDS pins, the **I/O Assignment Analysis** command assigns pin locations for each LVDS pin in the specified edge location and then performs legality checks.

To accept these suggested pin locations, choose **Back-Annotate Assignments** (Assignments menu), select **Pin & device** assignments, and click **OK**. Back-annotation saves your pin and device assignments in the QSF.

Understanding the I/O Assignment Analysis Report & Messages

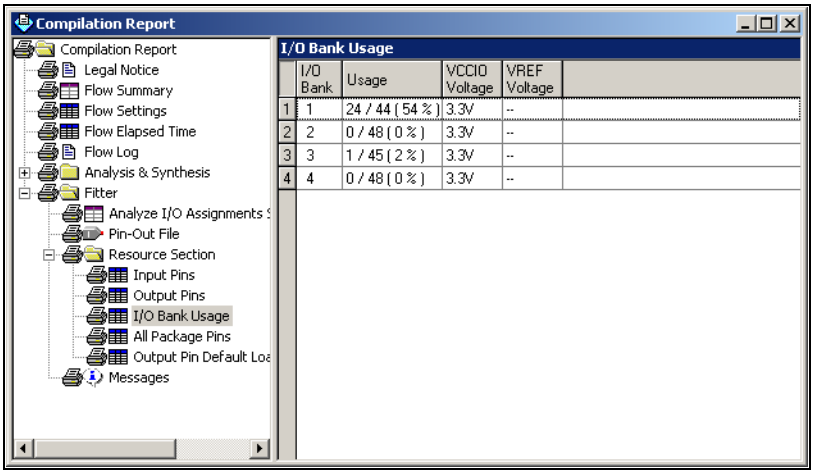
The **Start I/O Assignment Analysis** command generates a detailed analysis report (Figure 6–6) and a Pin-out file (**.pin**). The detailed messages in the report help you quickly understand and resolve pin assignment errors. Each detailed message includes a related node name and a description of the problem.

You can view the report file by choosing **Compilation Report** (Project menu). The **Fitter** section of the **Compilation Report** contains the following four sections:

- Analyze I/O Assignment Summary
- Resource Section
- Pin-Out File
- Fitter Messages

The Resource Section categorizes the pins as **Input Pins**, **Output Pins**, and **Bidir Pins**. View the utilization of each I/O bank in your device in the **I/O Bank Usage** section.

Figure 6–6. Summary of the I/O Bank Usage in the I/O Assignment Analysis Report



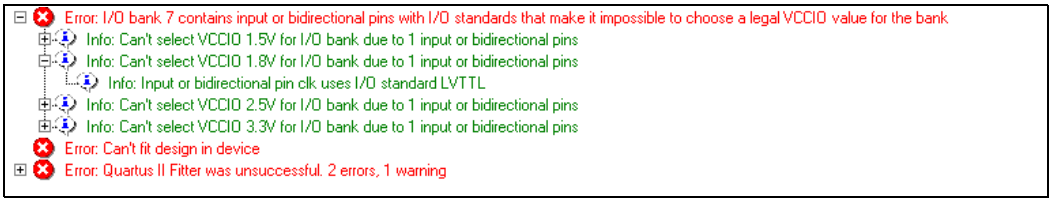
The **Fitter Messages** page stores all messages including errors, warnings, and information messages.

You can view the detailed messages in the **Fitter Messages** page in the compilation report and in the **Processing** tab in the **Messages** window. Choose **Utility Windows** > **Messages** (View menu) to open the **Messages** window.

Use the **Location** box to help resolve the error messages. Select from the **Location** list and click **Locate**.

Figure 6–7 shows an example of error messages reported by I/O assignment analysis.

Figure 6–7. Error Message Report by I/O Assignment Analysis



Scripting Support

A Tcl script allows you to run procedures and make settings described in this chapter. You can also run some of these procedures at a command prompt.

For detailed information about specific scripting command options and Tcl API packages, type `quartus_sh --qhelp` at a system command prompt to run the Quartus II Command-Line and Tcl API Help browser.

For more information on Quartus II scripting support, including examples, refer to the *Tcl Scripting* and *Command-Line Scripting* chapters in volume 2 of the *Quartus II Handbook*.

Running the I/O Assignment Analysis

You can run the I/O assignment analysis with a Tcl command or with a command run at a command prompt. For more information about running the I/O assignment analysis, refer to "Understanding the I/O Assignment Analysis Report & Messages" on page 6–11.

Tcl Command

Enter the following in a Tcl console or script:

```
execute_flow -check_ios
```

Command Prompt

Type the following at a (non-Tcl) system command prompt:

`quartus_fit` <*project-name*> `--check_ios` ↵

Generating a Mapped Netlist

You can generate a mapped netlist with a Tcl command or with a command-line command. For more information about generating a mapped netlist, refer to "Generating a Mapped Netlist" on page 6–8.

Tcl Command

Enter the following in the Tcl console or in a script:

```
execute_module -tool map
```

The `execute_module` command is in the flow package.

Command Prompt

Type the following at a system command prompt:

```
quartus_map <project name>↵
```

Reserving Pins

Use the following Tcl command to reserve a pin. For more information about reserving pins, refer to "Reserving Pins" on page 6–9.

```
set_instance_assignment -name RESERVE_PIN <value> -to <signal name>
```

Valid values are `"AS BIDIRECTIONAL"`, `"AS INPUT TRI-STATED"`,`"AS OUTPUT DRIVING AN UNSPECIFIED SIGNAL"`, `"AS OUTPUT DRIVING GROUND"` and `"AS SIGNAL PROBE OUTPUT"`. Include the quotes when specifying the value.

Location Assignments

Use the following Tcl command to assign a signal to a pin or device location. For more information about location assignments, refer to "Location Assignments" on page 6–9.

```
set_location_assignment <location> -to <signal name>
```

Valid locations are pin location names, such as `Pin_A3`. The Stratix series and Cyclone device families also support edge and I/O bank locations. Edge locations are `EDGE_BOTTOM`, `EDGE_LEFT`, `EDGE_TOP`, and `EDGE_RIGHT`. I/O bank locations include `IOBANK_1` up to `IOBANK_n`, where *n* is the number of I/O banks in a particular device.

Conclusion

The **Start I/O Assignment Analysis** command quickly and thoroughly validates the legality of your pin-related assignments. This helps reduce development time by catching illegal pin assignments early in the design cycle without wasting long design compilations.

By providing the designer with more confidence in the device pin-outs at an early stage, board layout engineers can work in parallel with FPGA designers to achieve a time-to-market advantage.