

This chapter provides the recommended transceiver initialization and reset sequence for Stratix[®] V devices. The recommended reset sequence ensures that the physical coding sublayer (PCS) and physical medium attachment (PMA) in each transceiver channel are initialized and functioning correctly.

Transceiver Reset Sequence

There are two methods of performing the reset sequence in Stratix V transceivers:

- **“Embedded Reset Controller”**
 - The embedded reset controller is enabled by default.
 - One embedded reset controller controls one PHY IP instance (a PHY IP instance could be one channel or multiple channels). Individual channels within a PHY IP instance cannot have separate resets. Resetting one channel in the PHY IP instance resets all the other channels as well.
 - The embedded reset controller is positive-edge triggered.
 - The embedded reset controller cannot be held in reset.
- **“User-Controlled Reset Controller”**
 - If you disable the embedded reset controller, you must implement your own reset logic.
 - The user-controlled reset controller can be designed to reset a single channel or multiple channels simultaneously.
 - The user-controlled reset controller can be level triggered.
 - The user-controlled reset controller can be held in reset.

Embedded Reset Controller

Figure 3-1 shows a block diagram of the transceiver PHY instance and the Transceiver Reconfiguration Controller interacting with the embedded reset controller.

Figure 3-1. Interaction Between the Transceiver PHY Instance, Transceiver Reconfiguration Controller, and the Embedded Reset Controller

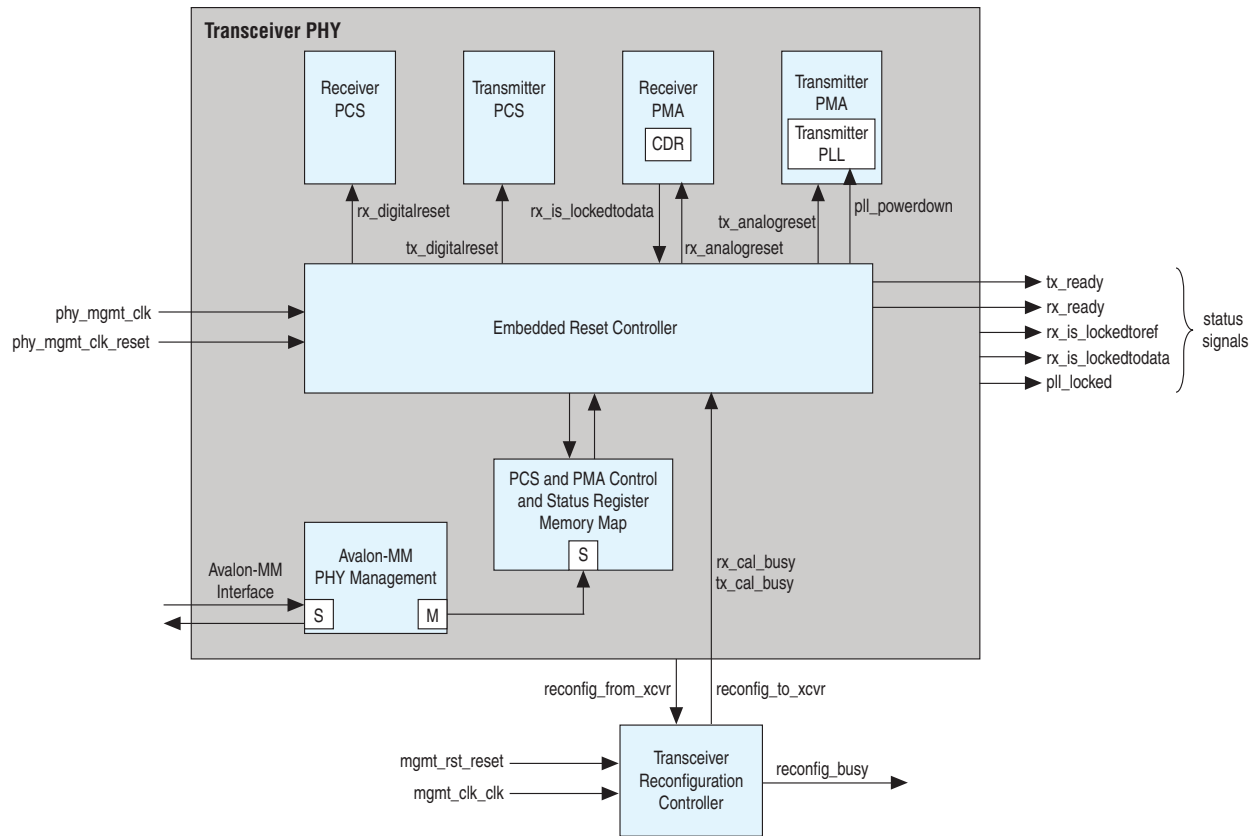


Table 3-1 lists the signals used by the transceiver PHY instance, Transceiver Reconfiguration Controller, and embedded reset controller.

Table 3-1. Signals Used by the Transceiver PHY instance, Transceiver Reconfiguration Controller, and Embedded Reset Controller ⁽¹⁾ (Part 1 of 2)

Signal Name	Signal Type	Description
phy_mgmt_clk	Clock	Clock for the transceiver PHY IP
mgmt_clk_clk	Clock	Clock for the Transceiver Reconfiguration Controller
phy_mgmt_clk_reset	Reset	Edge-triggered reset for the embedded reset controller. Low-to-high transition initiates the transceiver reset sequence.
mgmt_rst_reset	Reset	Reset for the Transceiver Reconfiguration Controller
pll_powerdown	Internal	A high on this signal indicates that the transmitter (TX) phase-locked loop (PLL) is held in reset
tx_analogreset	Internal	A high on this signal indicates the TX PMA is held in reset
tx_digitalreset	Internal	A high on this signal indicates the TX PCS is held in reset
rx_analogreset	Internal	A high on this signal indicates the receiver (RX) PMA is held in reset

Table 3-1. Signals Used by the Transceiver PHY instance, Transceiver Reconfiguration Controller, and Embedded Reset Controller ⁽¹⁾ (Part 2 of 2)

Signal Name	Signal Type	Description
rx_digitalreset	Internal	A high on this signal indicates the RX PCS is held in reset
tx_cal_busy	Internal	A high on this signal indicates that TX calibration is active
rx_cal_busy	Internal	A high on this signal indicates that RX calibration is active
reconfig_busy	Status	A high on this signal indicates that reconfiguration is active
pll_locked	Status	A high on this signal indicates that the TX PLL is locked
rx_is_lockedtoref	Status	A high on this signal indicates that the RX clock data recovery (CDR) is in the lock-to-reference (LTR) mode
rx_is_lockedtodata	Status	A high on this signal indicates that the RX CDR is in the lock-to-data (LTD) mode
tx_ready	Status	A low on this signal indicates that the TX datapath is in reset. A high indicates that the TX datapath is out of reset and ready for data transmission.
rx_ready	Status	A low on this signal indicates that the RX datapath is in reset. A high indicates that the RX datapath is out of reset and ready for data reception.

Note to Table 3-1:

(1) Some of the signal names may be slightly different from the register or port names in the Quartus® II software.

The embedded reset controller is positive-edge triggered. After device power-up, the reset controller initiates the reset sequence when it receives a positive edge on the `phy_mgmt_clk_reset` input signal.

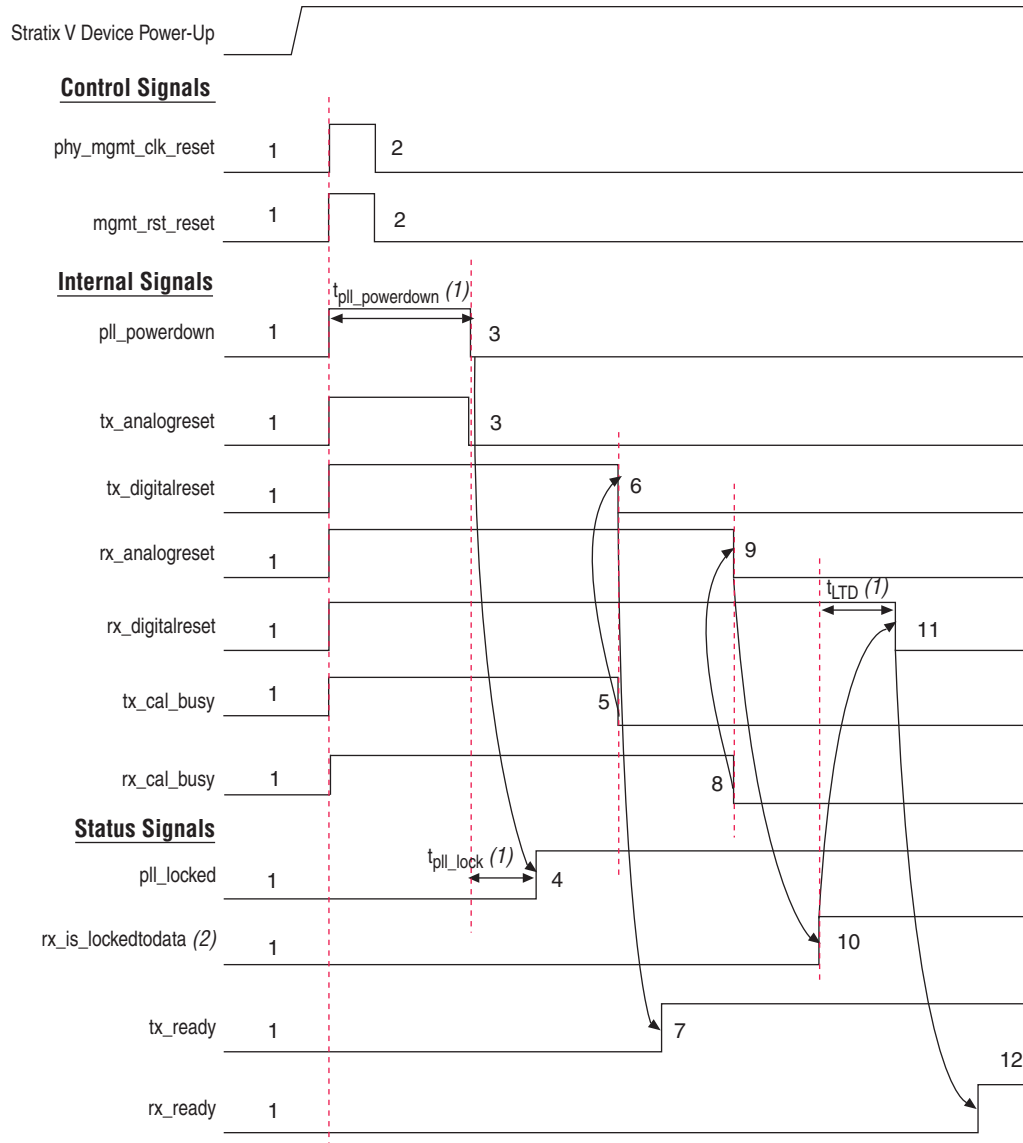
The embedded reset controller handles all the internal signals and the entire reset sequence. In case of loss-of-link or loss-of-data, the embedded reset controller asserts the appropriate reset signals.

You must monitor only the status signals. The `tx_ready` and `rx_ready` status signals indicate the transceiver is out of reset and ready for data transmission and reception.

At Power-Up

Figure 3-2 shows the numbered reset sequence of the embedded reset controller at power-up.

Figure 3-2. Timing Diagram for the Embedded Reset Controller at Power-Up



Notes to Figure 3-2:

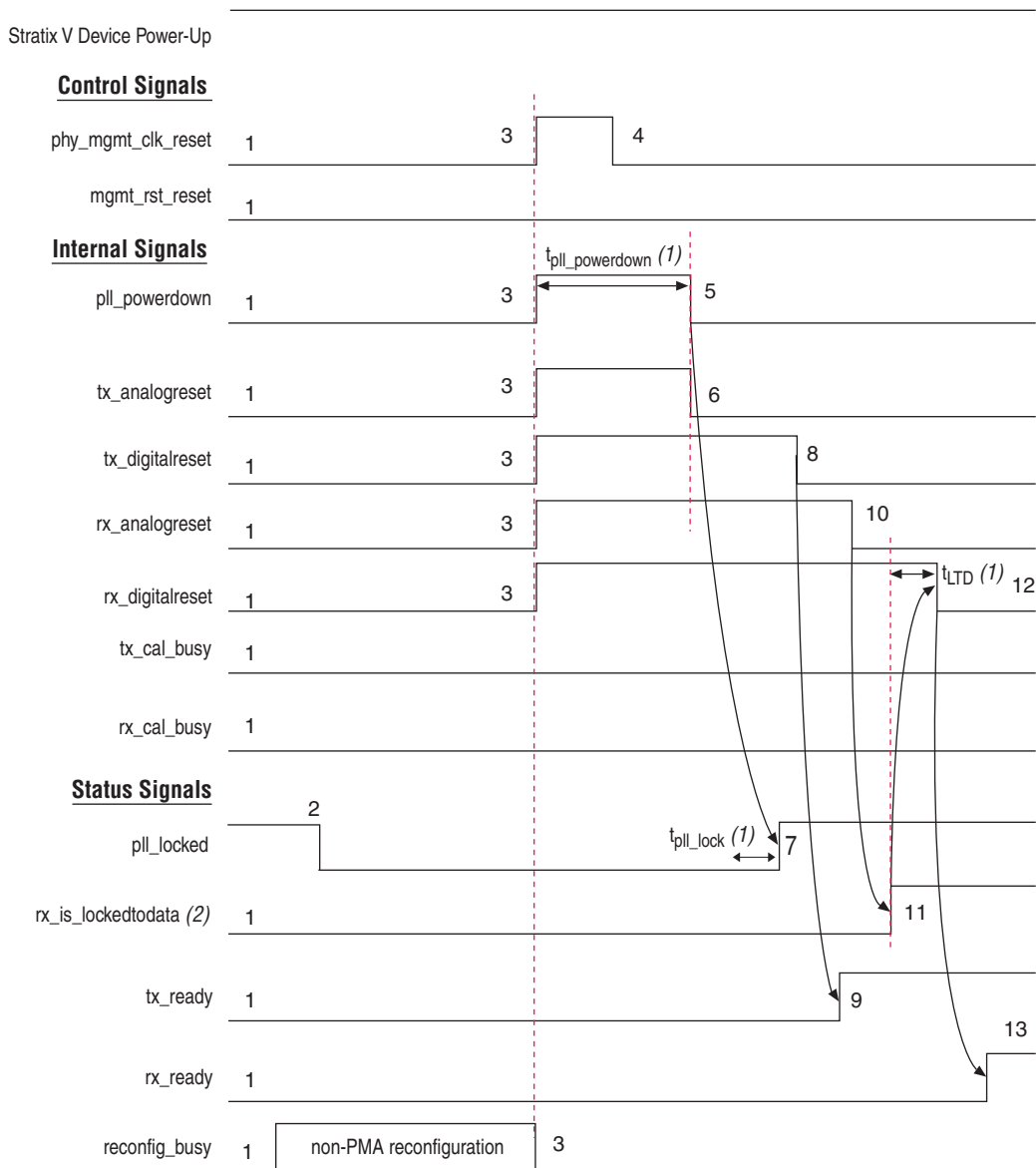
- (1) $t_{pll_powerdown}$, t_{pll_lock} , and t_{LTD} are pending characterization. For more information, refer to the *DC and Switching Characteristics for Stratix V Devices* chapter.
- (2) The `rx_is_lockedtodata` signal shown in this figure is the logical AND of the `rx_is_lockedtodata` signals from all channels in a transceiver PHY instance. If one RX channel loses lock, all channels in the transceiver PHY instance are reset.

During and After Reconfiguration

Altera recommends re-initiating the entire reset sequence after channel or PLL reconfiguration. You do not have to re-initiate the reset sequence after reconfiguring any PMA analog features such as PMA controls, on-chip signal quality monitoring (EyeQ), adaptive equalization (AEQ), decision feedback equalization (DFE), and loopback modes.

Figure 3-3 shows the numbered reset sequence of the embedded reset controller during and after reconfiguration.

Figure 3-3. Timing Diagram for the Embedded Reset Controller During and After Reconfiguration



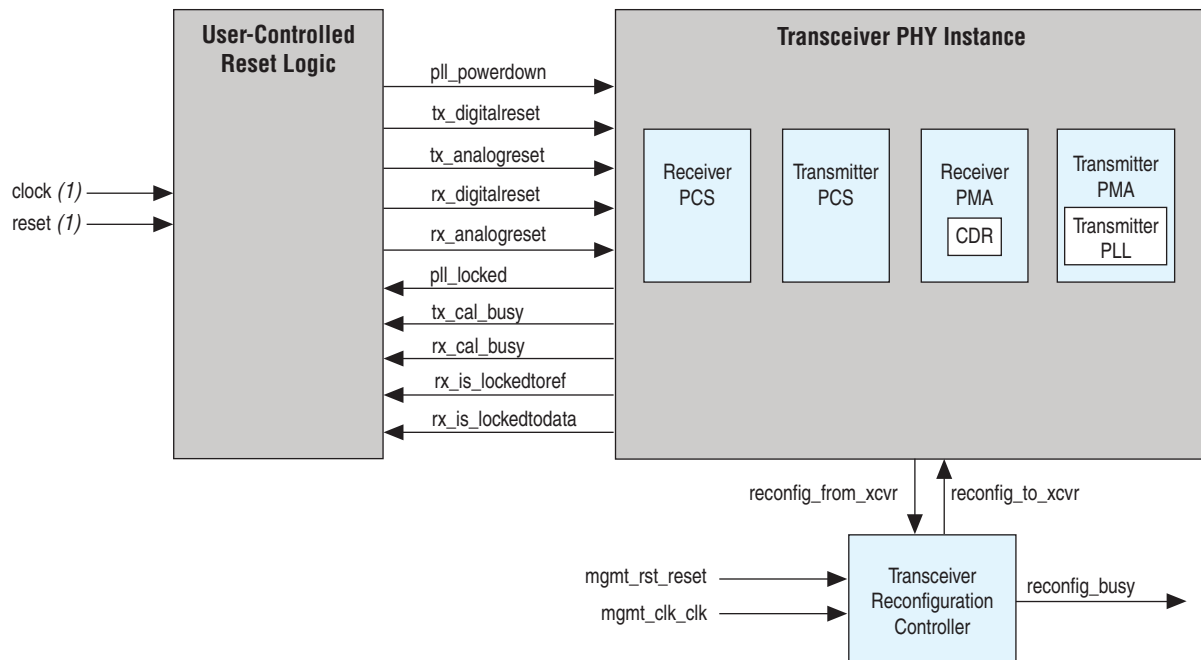
Notes to Figure 3-3:

- (1) $t_{pll_powerdown}$, t_{pll_lock} , and t_{LTD} are pending characterization. For more information, refer to the *DC and Switching Characteristics for Stratix V Devices* chapter.
- (2) The `rx_is_lockedtodata` signal shown in this figure is the logical AND of the `rx_is_lockedtodata` signals from all channels in a transceiver PHY instance. If one RX channel loses lock, all channels in the transceiver PHY instance are reset.

User-Controlled Reset Controller

Figure 3-4 shows a block diagram of the transceiver PHY instance and the Transceiver Reconfiguration Controller interacting with the user-controlled reset controller.

Figure 3-4. Interaction Between the Transceiver PHY Instance, Transceiver Reconfiguration Controller, and the User-Controlled Reset Controller



Note to Figure 3-4:

(1) You can use `phy_mgmt_clk` and `phy_mgmt_clk_reset` as the clock and reset to the user-controlled reset logic.

Table 3-2 lists the signals used by the transceiver PHY instance, Transceiver Reconfiguration Controller, and user-controlled reset controller.

Table 3-2. Signals Used by the Transceiver PHY instance, Transceiver Reconfiguration Controller, and User-Controlled Reset Controller ⁽¹⁾ (Part 1 of 2)

Signal Name	Signal Type	Description
<code>mgmt_clk_clk</code>	Clock	Clock for the Transceiver Reconfiguration Controller
<code>mgmt_rst_reset</code>	Reset	Reset for the Transceiver Reconfiguration Controller
<code>pll_powerdown</code>	Control	Resets the TX PLL when asserted high
<code>tx_analogreset</code>	Control	Resets the TX PMA when asserted high
<code>tx_digitalreset</code>	Control	Resets the TX PCS when asserted high
<code>rx_analogreset</code>	Control	Resets the RX PMA when asserted high
<code>rx_digitalreset</code>	Control	Resets the RX PCS when asserted high
<code>reconfig_busy</code>	Status	A high on this signal indicates that reconfiguration is active
<code>tx_cal_busy</code>	Status	A high on this signal indicates that TX calibration is active
<code>rx_cal_busy</code>	Status	A high on this signal indicates that RX calibration is active
<code>pll_locked</code>	Status	A high on this signal indicates that the TX PLL is locked
<code>rx_is_lockedtoref</code>	Status	A high on this signal indicates that the RX CDR is in the LTR mode

Table 3-2. Signals Used by the Transceiver PHY instance, Transceiver Reconfiguration Controller, and User-Controlled Reset Controller ⁽¹⁾ (Part 2 of 2)

Signal Name	Signal Type	Description
rx_is_lockedtoata	Status	A high on this signal indicates that the RX CDR is in the LTD mode

Note to Table 3-2:

(1) Some of the signal names may be slightly different from the register or port names in the Quartus II software.

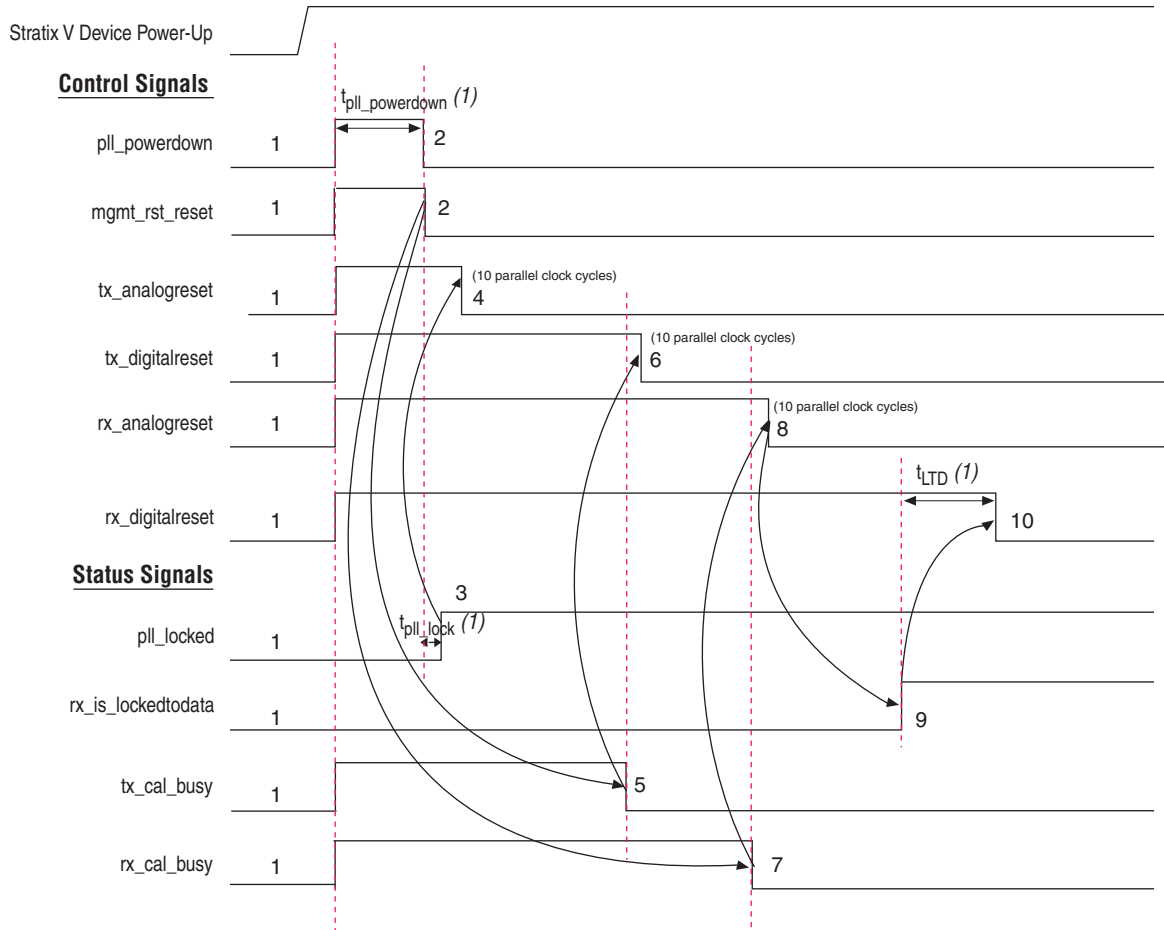
If you disable the embedded reset controller, you must implement your own reset controller logic. You must take the following factors into account:

- The user-controlled reset controller can be level sensitive
- The user-controlled reset controller does not depend on `phy_mgmt_clk_reset`
- You are responsible for providing a clock and reset to the reset controller logic
- Some of the internal signals are now exposed as control signals
- You can hold the transceiver channels in reset by asserting the appropriate reset control signals
- You can create a reset controller to reset individual channels separately
- The `tx_ready` and `rx_ready` status signals are not available in the user-controlled reset controller mode

At Power-Up

Figure 3-5 shows reset sequence of the user-controlled reset controller at power-up. Follow the numbered reset sequence.

Figure 3-5. Timing Diagram for the User-Controlled Reset Controller at Power-Up



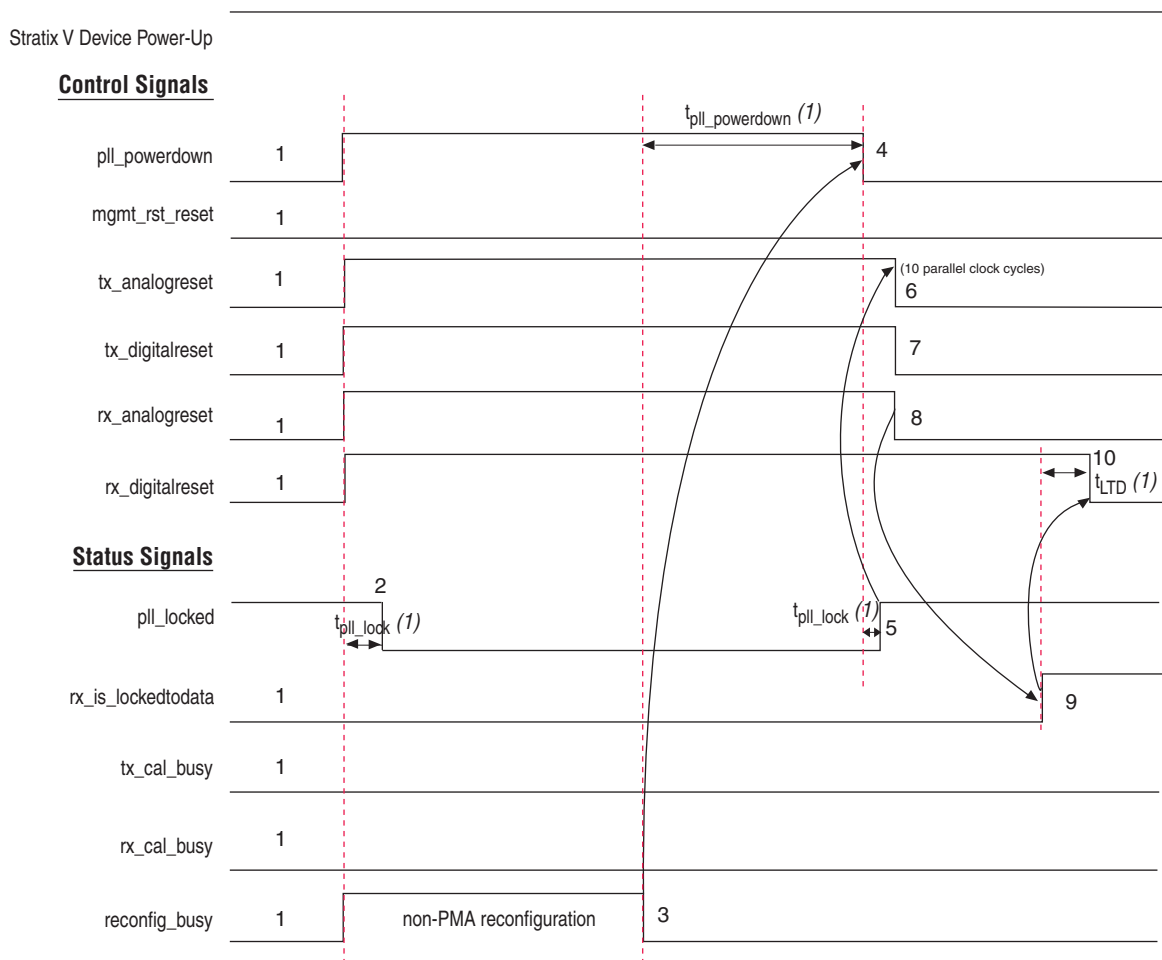
Note to Figure 3-5:

(1) $t_{pll_powerdown}$, t_{pll_lock} , and t_{LTD} are pending characterization. For more information, refer to the *DC and Switching Characteristics for Stratix V Devices* chapter.

During and After Reconfiguration

Figure 3-6 shows the reset sequence of the user-controlled reset controller during and after reconfiguration. Follow the numbered reset sequence. Altera recommends holding the transceiver channels in reset during channel or PLL reconfiguration. Holding the transceiver channels in reset during channel or PLL reconfiguration is not required while reconfiguring any PMA analog features such as PMA controls, EyeQ, AEQ, DFE, and loopback modes.

Figure 3-6. Timing Diagram for the User-Controlled Reset Controller During and After Reconfiguration



Note to Figure 3-6:

(1) $t_{pll_powerdown}$, t_{pll_lock} , and t_{LTD} are pending characterization. For more information, refer to the *DC and Switching Characteristics for Stratix V Devices* chapter.

CDR Modes During the Reset Sequence

Whether you are using the embedded reset controller or the user-controlled reset controller, the RX CDR can be in either automatic lock mode or manual lock mode.

Reset Sequence for CDR in Automatic Lock Mode

The CDR is in automatic lock mode by default for both the embedded reset controller and the user-controlled reset controller. For timing diagrams, refer to [Figure 3-2 on page 3-4](#) through [Figure 3-6 on page 3-9](#).

Reset Sequence for CDR in Manual Lock Mode

The CDR in manual lock mode is also available for both the embedded reset controller and the user-controlled reset controller. The two control signals to enable the CDR in manual lock mode are `rx_set_locktoref` and `rx_set_locktodata`.

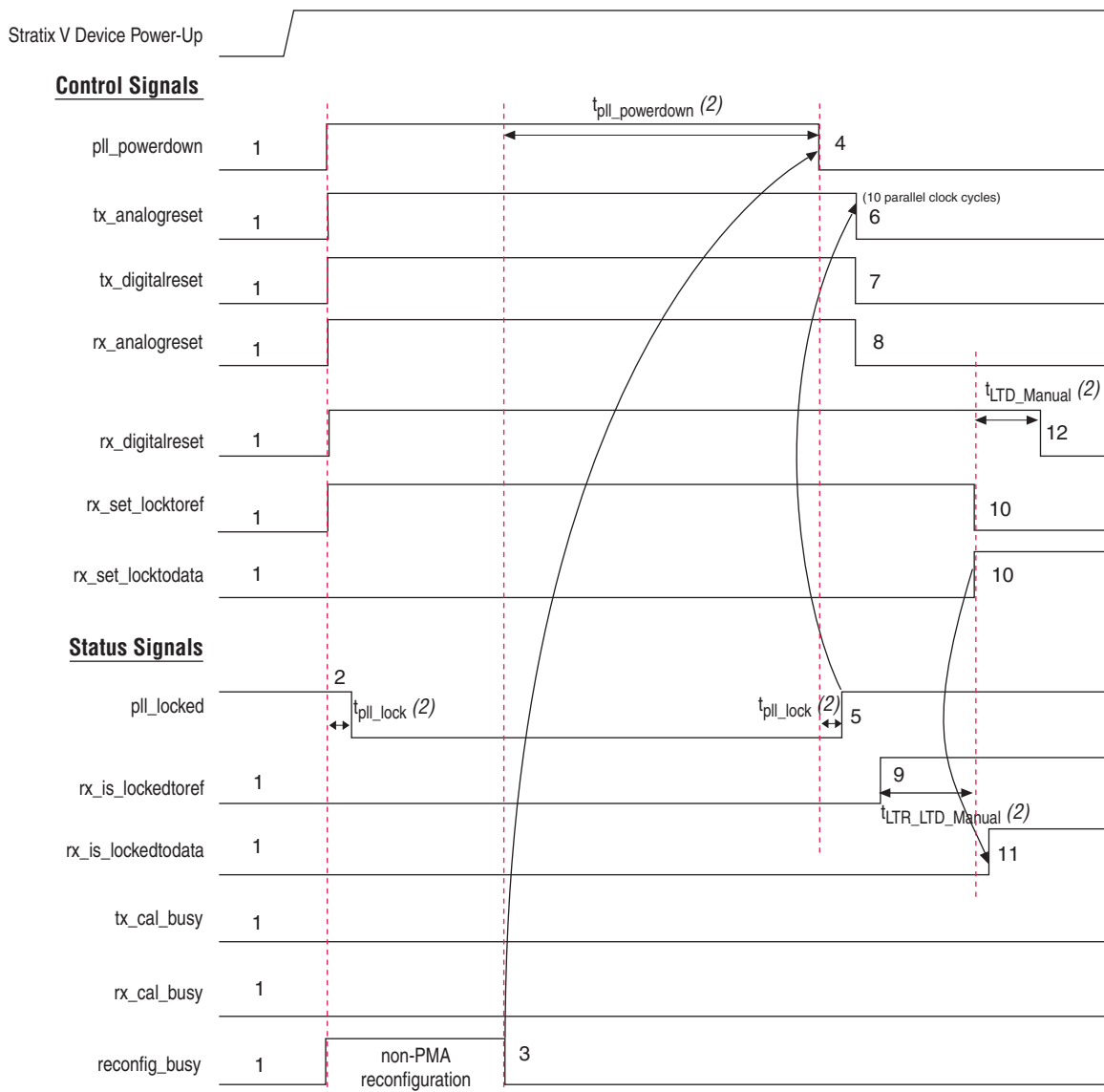
[Table 3-3](#) lists the control settings for the CDR in manual lock mode.

Table 3-3. Control Settings for the CDR in Manual Lock Mode

<code>rx_set_locktoref</code>	<code>rx_set_locktodata</code>	CDR Lock Mode
0	0	Automatic
1	0	Manual—RX CDR LTR
X	1	Manual—RX CDR LTD

Figure 3-7 shows one of the timing diagrams of the transceiver reset sequence for the CDR in manual lock mode. Follow the numbered reset sequence. Manual lock mode can also be implemented in all the other configurations described previously.

Figure 3-7. Timing Diagram for the Transceiver Reset Sequence for CDR in Manual Lock Mode ⁽¹⁾



Notes to Figure 3-7:

- (1) This timing diagram is just one configuration in which manual lock mode can be implemented.
- (2) $t_{pll_powerdown}$, t_{LTD_Manual} , t_{pll_lock} , and $t_{LTR_LTD_Manual}$ are pending characterization. For more information, refer to the *DC and Switching Characteristics for Stratix V Devices* chapter.

Document Revision History

Table 3-4 lists the revision history for this chapter.

Table 3-4. Document Revision History

Date	Version	Changes
November 2011	3.0	<ul style="list-style-type: none"> ■ Added “Embedded Reset Controller” and “User-Controlled Reset Controller” sections. ■ Updated Figure 3-2, Figure 3-3, Figure 3-5, Figure 3-6, and Figure 3-7. ■ Added the tx_analogreset signal. ■ Minor text edits.
May 2011	2.0	<ul style="list-style-type: none"> ■ Added sections for CDR reset sequence in automatic and manual lock mode. ■ Removed sections for PCIe and non-PCIe reset sequences. ■ Chapter moved to Volume 3.
December 2010	1.1	No changes to the content of this chapter for the Quartus II software 10.1.
July 2010	1.0	Initial release.