

This document lists the Stratix<sup>®</sup> V device family features that were not enabled in the Quartus<sup>®</sup> II software version 10.1. However, these features will be supported in a future release of the Quartus II software.

Table 1 lists the current available device support.

**Table 1. Device Support for Stratix V Devices**

Device Variant	Support
Stratix V E	The Stratix V E FPGAs will be supported in a future release of the Quartus II software.
Stratix V GS	Select Stratix V GS devices are currently supported in the Quartus II software.
Stratix V GT	The Stratix V GT FPGAs will be supported in a future release of the Quartus II software.
Stratix V GX	Select Stratix V devices are currently supported in the Quartus II software.

## Features of the Stratix V Device Family

Table 1 lists the configuration features that will be supported in a future version of the Quartus II software.

**Table 2. Configuration Support for Stratix V Devices**

Feature	Future Support
Partial reconfiguration	You will be able to partially reconfigure Stratix V devices while the rest of the device is still operating.
Configuration via PCI Express <sup>®</sup> (PCIe)	Configuration via PCIe will allow you to configure the FPGA fabric using one of the transceiver channels configured in PCIe mode.
DCLK pin as the initialization clock source	You will be able to use a DCLK pin as the clock source during initialization for fast passive parallel (FPP) and passive serial (PS) configuration schemes.

Table 2 lists the FPGA fabric features that will be supported in a future version of the Quartus II software.

**Table 3. FPGA Fabric Support for Stratix V Devices**

Feature	Future Support
Single event upset (SEU) mitigation	The following SEU features will be supported in a future version of the Quartus II software: <ul style="list-style-type: none"> <li>■ Error classification</li> <li>■ Scrubbing</li> <li>■ Fault injection</li> </ul>
Anti-tamper	Advanced encryption standard (AES) encryption and additional anti-tamper features will be supported closer to silicon availability.

Table 4 lists the external memory features that are currently supported and features that will be supported in a future version of the Quartus II software.

**Table 4. External Memory Support for Stratix V Devices**

Feature	Current Support	Future Support
DDR3	DDR3 up to 533 MHz with preliminary IP	Final IP that enables DDR3 functionality up to 800 MHz.
RLDRAM II PHY/Controller IP	Supported in the Quartus II software version 10.1 and beyond	—
QDR II/II+ PHY/Controller IP	Supported in the Quartus II software version 10.1 and beyond	—
DDR2/3 RDIMM UniPHY-based controller	Supported in the Quartus II software version 10.1 and beyond	—

Table 5 lists the transceiver standard physical coding sublayer (PCS) features that are currently supported and features that will be supported in a future version of the Quartus II software.

**Table 5. Transceiver Standard PCS Support for Stratix V Devices**

Feature	Current Support	Future Support
Protocols supported using standard PCS	<ul style="list-style-type: none"> <li>■ PCIe Gen1/Gen2 ×1, ×4, and ×8 modes</li> <li>■ XAUI using soft PCS</li> <li>■ Select custom configurations</li> <li>■ SerialLite and SerialLite II</li> <li>■ Fiber Channel 1G, 2G, 4G and 8G</li> <li>■ SONET OC12, OC48</li> <li>■ Low latency configurations</li> </ul> <p>NOTE: For details regarding configurations supported, refer to the specific handbook.</p>	<p>The following transceiver protocol modes will be supported in a future release of the Quartus II software:</p> <ul style="list-style-type: none"> <li>■ PCIe Gen3 ×1, ×4, and ×8 modes</li> <li>■ PCIe Gen1/Gen2/Gen3 ×2 mode</li> <li>■ Serial RapidIO (SRIO) v1.2 and v2.1</li> <li>■ Gigabit Ethernet (GbE)</li> <li>■ HiGig, HiGig+, and HiGig2</li> <li>■ XAUI using Hard PCS</li> <li>■ QPI</li> <li>■ HyperTransport 3.1</li> <li>■ Serial digital interface (SDI)</li> <li>■ Deterministic Latency (CPRI/OBSAI)</li> <li>■ SATA/SAS</li> <li>■ All custom configurations</li> </ul>
PCIe	<ul style="list-style-type: none"> <li>■ PCIe Gen1/Gen2 ×1, ×4, and ×8 modes</li> <li>■ PCIe low latency synchronous mode</li> </ul>	<p>The following PCIe features will be supported in a future release of the Quartus II software:</p> <ul style="list-style-type: none"> <li>■ PCIe Gen1/Gen2 ×2 mode</li> <li>■ PCIe Gen3 ×1, ×2, ×4, and ×8 modes</li> <li>■ Dynamic rate switch between Gen1, Gen2, and Gen3 modes</li> <li>■ Reverse parallel loopback</li> </ul>
XAUI	XAUI links are currently implemented using the physical media attachment (PMA) of the transceiver and soft PCS in the FPGA fabric. The hard PCS available in Stratix V devices does not currently support XAUI in the Quartus II software.	You will have the option to use the hard PCS available in the transceiver to implement XAUI links.
SRIO	Not supported	<ul style="list-style-type: none"> <li>■ Hard PCS will be enabled to support SRIO 1.2 and 2.1 protocols.</li> <li>■ ×2 and ×4 bonding will be available in addition to independent ×1 channels.</li> </ul>
Deterministic latency mode	Not supported	Deterministic latency mode will be supported in the future for protocols such as Common Public Radio Interface (CPRI) and OBSAI.

Table 6 lists the transceiver 10G PCS features that are currently supported and features that will be supported in a future version of the Quartus II software.

**Table 6. Transceiver 10G PCS Support for Stratix V Devices**

Feature	Current Support	Future Support
Protocols supported using 10G PCS	<ul style="list-style-type: none"> <li>■ Interlaken</li> <li>■ 10G Base-R</li> <li>■ SFI-S</li> <li>■ SDI 10G</li> <li>■ 10GPON</li> <li>■ 10G EPON</li> <li>■ Low latency configurations</li> <li>■ Select custom configurations</li> </ul>	<p>The following transceiver protocol modes using the transceiver 10G PCS will be supported in a future release of the Quartus II software:</p> <ul style="list-style-type: none"> <li>■ 10G Base-KR</li> <li>■ 40G/100G Ethernet</li> <li>■ SONET OC192</li> <li>■ Low latency configurations</li> </ul>

Table 7 lists the transceiver clocking features that are currently supported and features that will be supported in a future version of the Quartus II software.

**Table 7. Transceiver Clocking Support for Stratix V Devices (Part 1 of 2)**

Feature	Current Support	Future Support
Input reference clock sources	Dedicated <code>refclk</code> pins	<p>In addition to dedicated <code>refclk</code> pins, the following input reference clock sources will be enabled:</p> <ul style="list-style-type: none"> <li>■ Dual-purpose receiver/<code>refclk</code> pins—receiver pins of <b>Transmit-only</b> or unused transceiver channels can be used for sourcing input reference clocks. They will support fewer I/O standards when compared with dedicated <code>refclk</code> pins.</li> <li>■ Fractional phase-locked loops (PLLs) outputs.</li> <li>■ Global clock networks.</li> </ul>
ATX PLL	LC-tank based ATX PLLs can be enabled as transmit PLLs for superior performance for high data rates.	Support for new configurations as the configurations become available.
Fractional PLL	Supported for use in the FPGA fabric as general purpose PLLs	<p>The following fractional PLL features will be supported:</p> <ul style="list-style-type: none"> <li>■ Ability to use fractional PLLs as transmit PLLs for transceivers</li> <li>■ Cascading output counters to create counters larger than 512</li> <li>■ Fractional support</li> <li>■ Dynamic reconfiguration</li> <li>■ Dynamic clock switchover</li> <li>■ Dynamic phase shift</li> </ul>

**Table 7. Transceiver Clocking Support for Stratix V Devices (Part 2 of 2)**

Feature	Current Support	Future Support
PLL cascading	Not supported	The following transceiver PLL cascading will be supported in the future: <ul style="list-style-type: none"> <li>Fractional PLL to transmit PLL cascade—using fractional PLLs to generate multiple input reference clocks for transmit PLLs using a single input clock to the fractional PLL.</li> <li>Clock divider to fractional PLL cascade—to save clock sources in systems by using clocks generated by a transmit PLL in the FPGA fabric.</li> <li>Recovered <code>clk</code> to fractional PLL cascade—for repeater-type applications that require clock clean-up.</li> </ul>
Transmit PLL feedback compensation mode	Not supported	Transmit PLL feedback compensation mode will be enabled to support: <ul style="list-style-type: none"> <li>Deterministic latency by compensating for uncertainty introduced by clock dividers for protocols such as CPRI and OBSAI.</li> <li>Multi-channel bonding for data rates beyond 6 Gbps.</li> </ul>
Multi-Channel Bonding	The following are supported: <ul style="list-style-type: none"> <li>Bonding up to five channels for configurations using standard PCS</li> <li>Bonding up to 8 channels for PCIe Gen1/Gen2 configurations</li> </ul>	The following will be supported: <ul style="list-style-type: none"> <li>Side-wide bonding for configurations using standard PCS. Data rates will vary based on the number of channels bonded. The data rates will be determined after characterization.</li> <li>Side-wide bonding for configurations using 10G PCS. Data rates will vary based on the number of channels bonded. The data rates will be determined after characterization.</li> </ul>
Flexible master/slave configuration	In bonded configurations, a master channel provides control signals and clocks all the remaining slave channels. Currently, you cannot choose which channel is master.	You will be able to choose which channel will be the master.

Table 8 lists the transceiver PMA features that are currently supported and features that will be supported in a future version of the Quartus II software.

**Table 8. Transceiver PMA Support for Stratix V Devices**

Feature	Current Support	Future Support
Signal detect and electrical idle	<ul style="list-style-type: none"> <li>Electrical idle for PCIe Gen1</li> <li>Electrical idle inference for PCIe Gen2</li> </ul>	<ul style="list-style-type: none"> <li>Electrical idle inference for PCIe Gen3</li> <li>Signal detect for SATA and HyperTransport</li> </ul>
Loopback	<ul style="list-style-type: none"> <li>Serial loopback for all protocols except PCIe</li> <li>Reverse parallel loopback for PCIe</li> </ul>	<ul style="list-style-type: none"> <li>Reverse serial loopback</li> <li>Pre-clock data recovery (CDR) reverse serial loopback</li> </ul>

Table 9 lists the signal conditioning features that will be supported in a future version of the Quartus II software.

**Table 9. Signal Conditioning Features Support for Stratix V Devices**

Feature	Future Support
EyeQ	EyeQ hardware allows you to analyze and debug the receiver data recovery path (receiver gain, clock jitter, and noise level). You can use it to monitor the eye and assess the quality of the incoming signal. In Stratix V devices, you can observe the complete eye opening by measuring both the eye width and height. You can use this data to adjust the data sampling point to an optimal location with the largest eye opening and least bit error ratio (BER).
Adaptive Equalization (AEQ)	The AEQ feature will enable the Stratix V transceivers to adapt to changing data rates and backplane characteristics by dynamically tuning the equalization settings of the receiver without user intervention. It will also support a standby mode for lower power consumption. In standby mode, the AEQ block locks in the selected equalization settings instead of continuously tuning the equalization settings for the receiver.
Decision feedback equalization (DFE)	High-speed signals transmitted across a backplane experience signal attenuation due to skin effect, dielectric losses, and crosstalk. Stratix V devices will provide multi-tap DFE to primarily compensate the backplane attenuation due to crosstalk. DFE is effective in canceling post cursor inter-symbol interference (ISI) by boosting only the high frequency components of a signal without noise amplification. You can use DFE feature in conjunction with pre-emphasis, linear equalization (manual equalization), and AEQ.

Table 10 lists the transceiver dynamic reconfiguration features that are currently supported and features that will be supported in a future version of the Quartus II software.

**Table 10. Transceiver Dynamic Reconfiguration Support for Stratix V Devices**

Feature	Current Support	Future Support
Dynamic reconfiguration	The Quartus II software supports dynamic reconfiguration in the following analog parameters of a transceiver PMA: <ul style="list-style-type: none"> <li>■ differential output voltage (<math>V_{OD}</math>)</li> <li>■ Pre Emphasis</li> <li>■ Equalization</li> <li>■ DC Gain</li> </ul>	Future versions of the Quartus II software will support dynamic reconfiguration of the following transceiver features: <ul style="list-style-type: none"> <li>■ Transmitter and receiver termination values</li> <li>■ Common mode voltage for QPI</li> <li>■ Channel reconfiguration</li> <li>■ Transmit PLL reconfiguration</li> <li>■ Transmit PLL selection</li> <li>■ Channel and transmit PLL reconfiguration</li> <li>■ AEQ</li> <li>■ DFE</li> <li>■ EyeQ</li> </ul>
PCIe hard IP reconfiguration	Not supported	Stratix V devices will support dynamic reconfiguration of the following in the PCIe hard IP: <ul style="list-style-type: none"> <li>■ Endpoint modes in PCIe Gen1/Gen2</li> <li>■ Rootport modes in PCIe Gen1/Gen2</li> <li>■ Runtime reconfiguration of PCIe read only registers</li> <li>■ Runtime switching between endpoint and rootport modes</li> </ul>

Table 11 lists a transceiver feature that will be supported in a future version of the Quartus II software.

**Table 11. Other Transceiver Feature Support for Stratix V Devices**

Feature	Future Support
Offset Cancellation	Offset cancellation compensates for on-die process variations between channels. It will be enabled for the following blocks in every channel: <ul style="list-style-type: none"> <li>■ Receiver buffer</li> <li>■ Transmitter buffer</li> <li>■ CDR</li> <li>■ AEQ</li> <li>■ DFE</li> <li>■ EyeQ</li> <li>■ Clock delay buffers</li> <li>■ On-die voltage regulators</li> </ul>

## Document Revision History

Table 12 shows the revision history for this document.

**Table 12. Document Revision History**

Date	Version	Changes
December 2010	1.3	Updated document for the Quartus II software 10.1 release.
July 2010	1.2	Updated document for Quartus II software 10.0 release.
April 2010	1.1	Updated item 22 and 23 in Table 1.
April 2010	1.0	Initial release.

