



Section VI. PCB Layout Guidelines

This section provides information for board layout designers to successfully layout their boards for Stratix® II devices. These chapters contain the required PCB layout guidelines and package specifications.

This section contains the following chapters:

- [Chapter 10, Package Information for Stratix II & Stratix II GX Devices](#)
- [Chapter 11, High-Speed Board Layout Guidelines](#)

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.



10. Package Information for Stratix II & Stratix II GX Devices

SI152010-4.3

Introduction

This chapter provides package information for Altera® Stratix® II and Stratix II GX devices, including:

- Device and package cross reference
- Thermal resistance values
- Package outlines

Tables 10–1 and 10–2 show which Altera Stratix II and Stratix II GX devices, respectively, are available in FineLine BGA® (FBGA) packages.

Device	Package	Pins
EP2S15	Flip-chip FBGA	484
	Flip-chip FBGA	672
EP2S30	Flip-chip FBGA	484
	Flip-chip FBGA	672
EP2S60	Flip-chip FBGA	484
	Flip-chip FBGA	672
	Flip-chip FBGA	1,020
EP2S90	Flip-chip FBGA	484
	Flip-chip FBGA	780
	Flip-chip FBGA	1,020
	Flip-chip FBGA	1,508
EP2S130	Flip-chip FBGA	780
	Flip-chip FBGA	1,020
	Flip-chip FBGA	1,508
EP2S180	Flip-chip FBGA	1,020
	Flip-chip FBGA	1,508

Table 10–2. Stratix II GX Devices in FBGA Packages

Device	Package	Pins
EP2SGX30	Flip-chip FBGA	780
EP2SGX60	Flip-chip FBGA	780
	Flip-chip FBGA	1,152
EP2SGX90	Flip-chip FBGA	1,152
	Flip-chip FBGA	1,508
EP2SGX130	Flip-chip FBGA	1,508

Thermal Resistance

Thermal resistance values for Stratix II devices are provided for a board that meets JEDEC specifications and for a typical board. The following values are provided:

- θ_{JA} (°C/W) still air—Junction-to-ambient thermal resistance with no air flow when a heat sink is not used.
- θ_{JA} (°C/W) 100 ft./min.—Junction-to-ambient thermal resistance with 100 ft./min. airflow when a heat sink is not used.
- θ_{JA} (°C/W) 200 ft./min.—Junction-to-ambient thermal resistance with 200 ft./min. airflow when a heat sink is not used.
- θ_{JA} (°C/W) 400 ft./min.—Junction-to-ambient thermal resistance with 400 ft./min. airflow when a heat sink is not used.
- θ_{JC} —Junction-to-case thermal resistance for device.
- θ_{JB} —Junction-to-board thermal resistance for device.

Tables 10–3 provides θ_{JA} (junction-to-ambient thermal resistance), θ_{JC} (junction-to-case thermal resistance), and θ_{JB} (junction-to-board thermal resistance) values for Stratix II devices on a board meeting JEDEC specifications for thermal resistance calculation. The JEDEC board specifications require two signal and two power/ground planes and are available at www.jedec.org.

Table 10–3. Stratix II Device Thermal Resistance for Boards Meeting JEDEC Specifications (Part 1 of 2)

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)	θ_{JB} (° C/W)
EP2S15	484	FBGA	13.1	11.1	9.6	8.3	0.36	4.19
	672	FBGA	12.2	10.2	8.8	7.6	0.36	4.09
EP2S30	484	FBGA	12.6	10.6	9.1	7.9	0.21	3.72
	672	FBGA	11.7	9.7	8.3	7.1	0.21	3.35

Table 10–3. Stratix II Device Thermal Resistance for Boards Meeting JEDEC Specifications (Part 2 of 2)

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)	θ_{JB} (° C/W)
EP2S60	484	FBGA	12.3	10.3	8.8	7.5	0.13	3.38
	672	FBGA	11.4	9.4	7.8	6.7	0.13	2.95
	1,020	FBGA	10.4	8.4	7.0	5.9	0.13	2.67
EP2S90	484	Hybrid FBGA	12.0	9.9	8.3	7.1	0.07	3.73
	780	FBGA	10.8	8.8	7.3	6.1	0.09	2.59
	1,020	FBGA	9.2	8.2	6.8	5.7	0.10	2.41
	1,508	FBGA	9.3	7.4	6.1	5.0	0.10	2.24
EP2S130	780	FBGA	10.1	8.7	7.2	6.0	0.07	2.44
	1,020	FBGA	9.5	8.1	6.7	5.5	0.07	2.24
	1,508	FBGA	8.6	7.3	6.0	4.8	0.07	2.08
EP2S180	1,020	FBGA	9.0	7.9	6.5	5.4	0.05	2.10
	1,508	FBGA	8.1	7.1	5.8	4.7	0.05	1.94

Table 10–4 provides θ_{JA} (junction-to-ambient thermal resistance), θ_{JC} (junction-to-case thermal resistance), and θ_{JB} (junction-to-board thermal resistance) values for Stratix II devices on a board with the information shown in Table 10–5.

Table 10–4. Stratix II Device Thermal Resistance for Typical Board (Part 1 of 2)

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)	θ_{JB} (° C/W)
EP2S15	484	FBGA	12.6	9.9	8.1	6.7	0.36	2.48
	672	FBGA	11.4	8.8	7.2	5.9	0.36	2.41
EP2S30	484	FBGA	12.3	9.6	7.8	6.4	0.21	2.02
	672	FBGA	11.1	8.5	6.9	5.6	0.21	1.95
EP2S60	484	FBGA	12.1	9.4	7.6	6.3	0.13	1.74
	672	FBGA	10.9	8.3	6.6	5.4	0.13	1.56
	1,020	FBGA	9.6	7.1	5.6	4.5	0.13	1.33
EP2S90	484	Hybrid FBGA	11.2	8.9	7.2	5.9	0.07	2.48
	780	FBGA	10.0	7.6	6.1	4.9	0.09	1.22
	1,020	FBGA	9.2	6.9	5.5	4.4	0.10	1.16
	1,508	FBGA	8.2	6.0	4.7	3.7	0.10	1.15

Table 10–4. Stratix II Device Thermal Resistance for Typical Board (Part 2 of 2)

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)	θ_{JB} (° C/W)
EP2S130	780	FBGA	9.3	7.5	6.0	4.8	0.07	1.12
	1,020	FBGA	8.5	6.8	5.3	4.2	0.07	1.03
	1,508	FBGA	7.5	5.8	4.6	3.6	0.07	1.02
EP2S180	1,020	FBGA	8.0	6.7	5.3	4.2	0.05	0.93
	1,508	FBGA	7.1	5.7	4.5	3.5	0.05	0.91

Table 10–5. Board Specifications Notes (1), (2)

Pin Count	Package	Signal Layers	Power/Ground Layers	Size (mm)
1,508	FBGA	12	12	100 × 100
1,020	FBGA	10	10	93 × 93
780	FBGA	9	9	89 × 89
672	FBGA	8	8	87 × 87
484	FBGA	7	7	83 × 83

Notes to Table 10–5:

- (1) Power layer Cu thickness 35 μ m, Cu 90%.
- (2) Signal layer Cu thickness 17 μ m, Cu 15%.

Table 10–6 provides θ_{JA} (junction-to-ambient thermal resistance) and θ_{JC} (junction-to-case thermal resistance) values for Stratix II devices.

Table 10–6. Stratix II GX Device Thermal Resistance

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)
EP2SGX30	780	FBGA	11.1	8.6	7.2	6.0	0.24
EP2SGX60	780	FBGA	10.9	8.4	6.9	5.8	0.15
	1,152	FBGA	9.9	7.5	6.1	5.0	0.15
EP2SGX90	1,152	FBGA	9.6	7.3	5.9	4.9	0.11
	1,508	FBGA	9.0	6.7	5.4	4.4	0.11
EP2SGX130	1,508	FBGA	8.3	6.6	5.3	4.3	0.10

Package Outlines

The package outlines are listed in order of ascending pin count. Altera package outlines meet the requirements of *JEDEC Publication No. 95*.

484-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

Tables 10–7 and 10–8 show the package information and package outline figure references, respectively, for the 484-pin FBGA packaging.

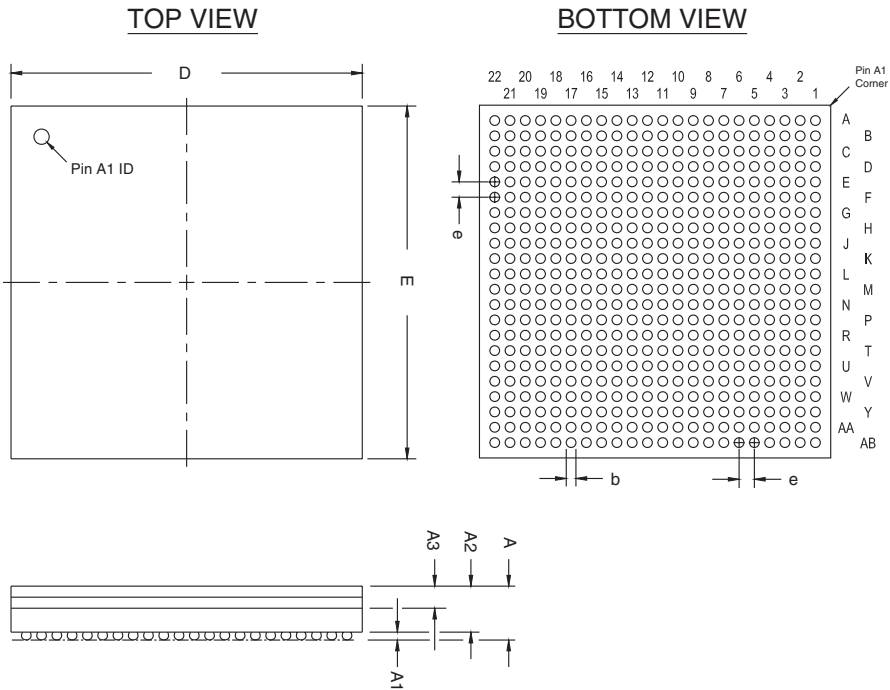
Table 10–7. 484-Pin FBGA Package Information	
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAJ-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	5.8 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 10–8. 484-Pin FBGA Package Outline Dimensions (Part 1 of 2)			
Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	23.00 BSC		
E	23.00 BSC		

Table 10–8. 484-Pin FBGA Package Outline Dimensions (Part 2 of 2)			
Symbol	Millimeter		
	Min.	Nom.	Max.
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 10–1 shows a package outline for the 484-pin FineLine BGA packaging.

Figure 10–1. 484-Pin FBGA Package Outline



672-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

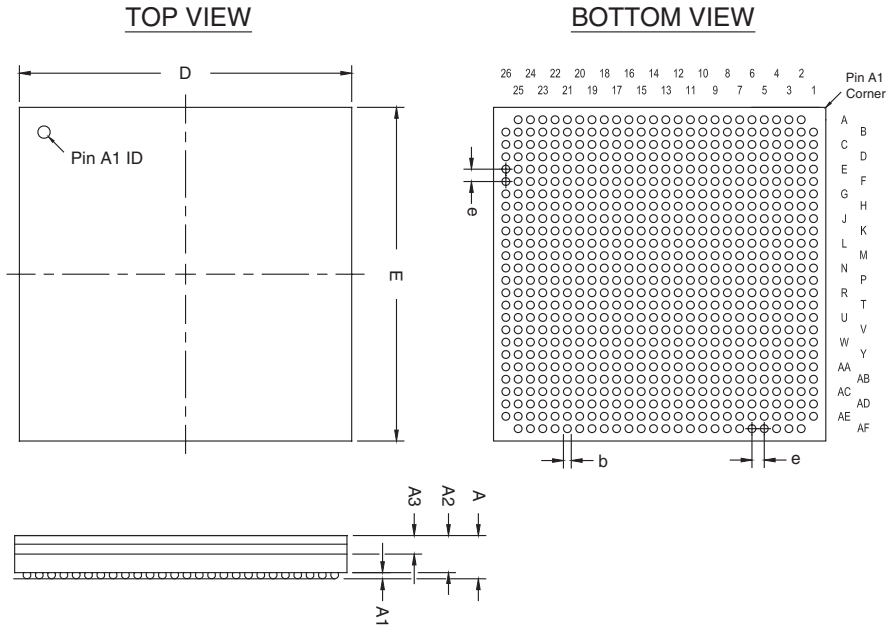
Tables 10–9 and 10–10 show the package information and package outline figure references, respectively, for the 672-pin FBGA packaging.

Table 10–9. 672-Pin FBGA Package Information	
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAL-1
Maximum Lead coplanarity	0.008 inches (0.20 mm)
Weight	7.7 g
Moisture Sensitivity level	Printed on moisture barrier bag

Table 10–10. 672-Pin FBGA Package Outline Dimensions			
Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	27.00 BSC		
E	27.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 10–2 shows a package outline for the 672-pin FineLine BGA packaging.

Figure 10–2. 672-Pin FBGA Package Outline



780-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

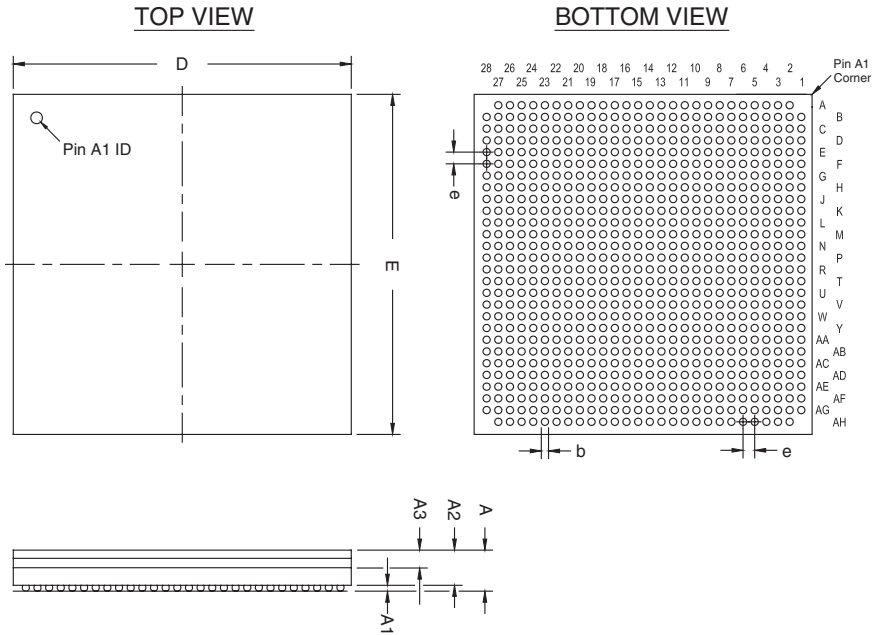
Tables 10–11 and 10–12 show the package information and package outline figure references, respectively, for the 780-pin FBGA packaging.

Table 10–11. 780-Pin FBGA Package Information	
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAM-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	8.9 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Table 10–12. 780-Pin FBGA Package Outline Dimensions			
Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	29.00 BSC		
E	29.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 10–3 shows a package outline for the 780-pin FineLine BGA packaging.

Figure 10–3. 780-Pin FBGA Package Outline



1,020-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

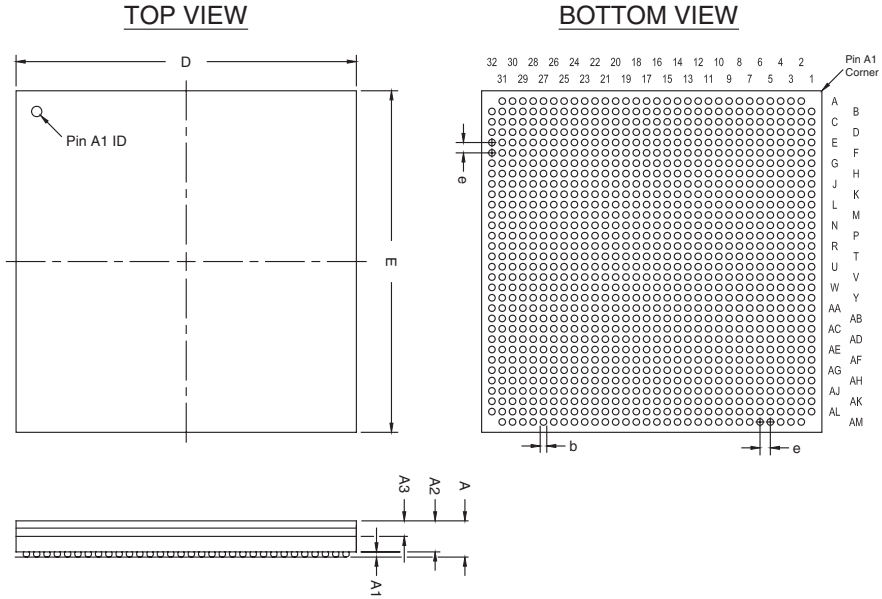
Tables 10–13 and 10–14 show the package information and package outline figure references, respectively, for the 1,020-pin FBGA packaging.

Table 10–13. 1,020-Pin FBGA Package Information	
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAP-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	11.5 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 10–14. 1,020-Pin FBGA Package Outline Dimensions			
Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	33.00 BSC		
E	33.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 10–4 shows a package outline for the 1,020-pin FineLine BGA packaging.

Figure 10–4. 1,020-Pin FBGA Package Outline



1,152-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

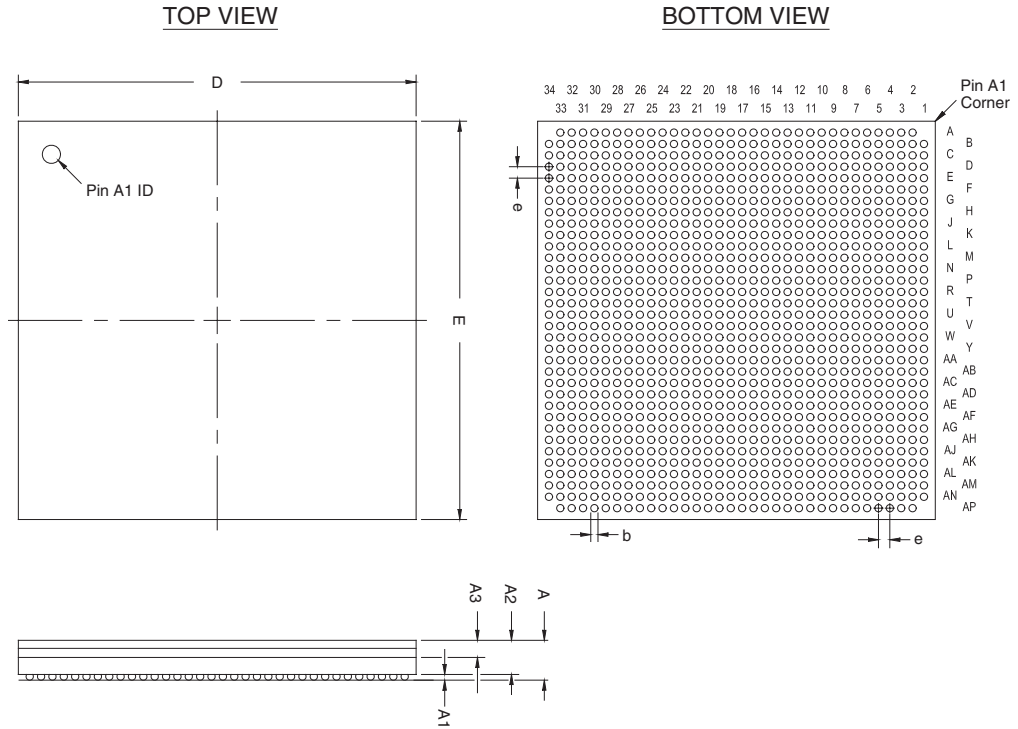
Tables 10–15 and 10–16 show the package information and package outline figure references, respectively, for the 1,152-pin FBGA packaging.

Table 10–15. 1,152-Pin FBGA Package Information	
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 variation: AAR-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	12.0 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 10–16. 1,152-Pin FBGA Package Outline Dimensions			
Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	35.00 BSC		
E	35.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 10–5 shows a package outline for the 1,152-pin FineLine BGA packaging.

Figure 10–5. 1,152-Pin FBGA Package Outline



1,508-Pin FBGA - Flip Chip

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

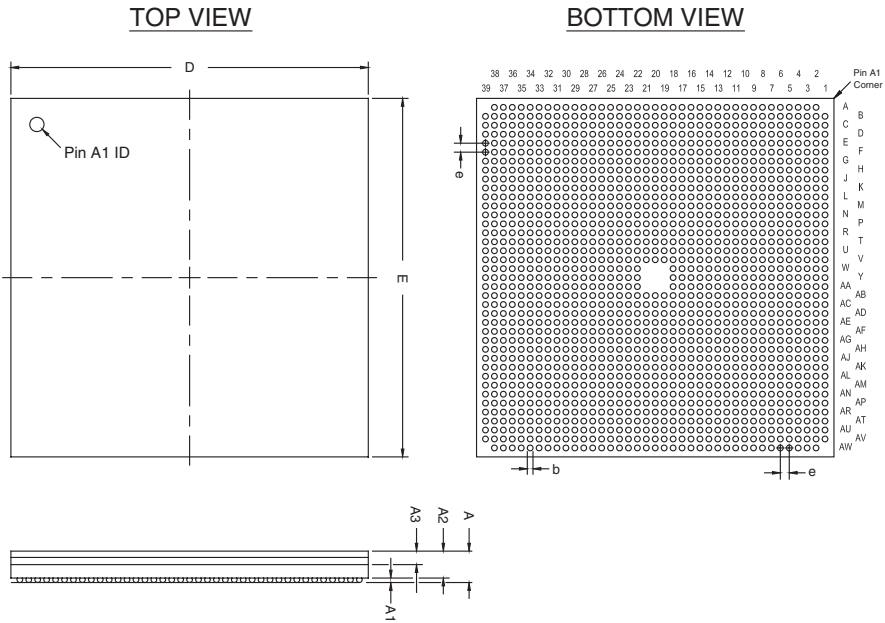
Tables 10–17 and 10–18 show the package information and package outline figure references, respectively, for the 1,508-pin FBGA packaging.

Table 10–17. 1,508-Pin FBGA Package Information	
Description	Specification
Ordering code reference	F
Package acronym	FBGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC outline reference	MS-034 Variation: AAU-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	14.6 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 10–18. 1,508-Pin FBGA Package Outline Dimensions			
Symbol	Millimeters		
	Min.	Nom.	Max.
A	–	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
A3	–	–	2.50
D	40.00 BSC		
E	40.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Figure 10–6 shows a package outline for the 1,508-pin FineLine BGA packaging.

Figure 10–6. 1,508-Pin FBGA Package Outline



Document Revision History

Table 10–19 shows the revision history for this chapter.

Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.3	Minor change to Table 10–3 .	—
February 2007 v4.2	Added the “ Document Revision History ” section to this chapter.	—
No change	Formerly chapter 14. Chapter number change only due to chapter addition to Section I in February 2006; no content change.	—
December 2005, v4.1	Chapter updated as part of the <i>Stratix II Device Handbook</i> update.	—
October 2005 v4.0	Added chapter to the <i>Stratix II GX Device Handbook</i> .	—

Introduction

Printed circuit board (PCB) layout becomes more complex as device pin density and system frequency increase. A successful high-speed board must effectively integrate devices and other elements while avoiding signal transmission problems associated with high-speed I/O standards. Because Altera® devices include a variety of high-speed features, including fast I/O pins and edge rates less than one hundred picoseconds, it is imperative that an effective design successfully:

- Reduces system noise by filtering and evenly distributing power to all devices
- Matches impedance and terminates the signal line to diminish signal reflection
- Minimizes crosstalk between parallel traces
- Reduces the effects of ground bounce

This chapter provides guidelines for effective high-speed board design using Altera devices and discusses the following issues:

- PCB material selection
- Transmission line layouts
- Routing schemes for minimizing crosstalk and maintaining signal integrity
- Termination schemes
- Simultaneous switching noise (SSN)
- Electromagnetic interference (EMI)
- Additional FPGA-specific board design/signal integrity information

PCB Material Selection

Fast edge rates contribute to noise and crosstalk, depending on the PCB dielectric construction material. Dielectric material can be assigned a dielectric constant (ϵ_r) that is related to the force of attraction between two opposite charges separated by a distance in a uniform medium as follows:

$$F = \frac{Q_1 Q_2}{4\pi\epsilon r^2}$$

where:

Q_1, Q_2 = charges

r = distance between the charges (m)

F = force (N)

ϵ = permittivity of dielectric (F/m).

Each PCB substrate has a different relative dielectric constant. The dielectric constant is the ratio of the permittivity of a substance to that of free space, as follows:

$$\epsilon_r = \frac{\epsilon}{\epsilon_0}$$

where:

ϵ_r = dielectric constant

ϵ_0 = permittivity of empty space (F/m)

ϵ = permittivity (F/m)

The dielectric constant compares the effect of an insulator on the capacitance of a conductor pair, with the capacitance of the conductor pair in a vacuum. The dielectric constant affects the impedance of a transmission line. Signals can propagate faster in materials that have a lower dielectric constant.

A high-frequency signal that propagates through a long line on the PCB from driver to receiver is severely affected by the loss tangent of the dielectric material. A large loss tangent means higher dielectric absorption.

The most widely used dielectric material for PCBs is FR-4, a glass laminate with epoxy resin that meets a wide variety of processing conditions. The dielectric constant for FR-4 is between 4.1 and 4.5. GETEK is another material that can be used in high-speed boards. GETEK is composed of epoxy and resin (polyphenylene oxide) and has a dielectric constant between 3.6 and 4.2.

Table 11-1 shows the loss tangent value for FR-4 and GETEK materials.

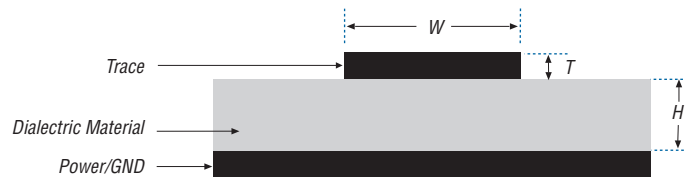
Manufacturer	Material	Loss Tangent Value
GE Electromaterials	GETEK	0.010 @ 1 MHz
Isola Laminate Systems	FR-4	0.019 @ 1 MHz

Transmission Line Layout

The transmission line is a trace and has a distributed mixture of resistance (R), inductance (L), and capacitance (C). There are two types of transmission line layouts, microstrip and stripline.

Figure 11-1 shows a microstrip transmission line layout, which refers to a trace routed as the top or bottom layer of a PCB and has one voltage-reference plane (power or ground). Figure 11-2 shows a stripline transmission line layout, which uses a trace routed on the inside layer of a PCB and has two voltage-reference planes (power and/or ground).

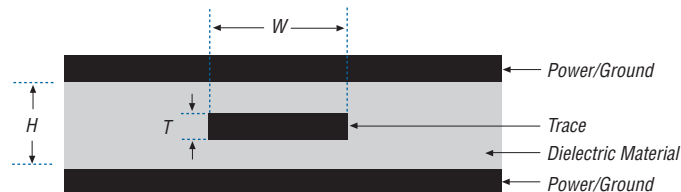
Figure 11-1. Microstrip Transmission Line Layout Note (1)



Note to Figure 11-1:

- (1) W = width of trace, T = thickness of trace, and H = height between trace and reference plane.

Figure 11-2. Stripline Transmission Line Layout Note (1)



Note to Figure 11-2:

- (1) W = width of trace, T = thickness of trace, and H = height between trace and two reference planes.

Impedance Calculation

Any circuit trace on the PCB has characteristic impedance associated with it. This impedance is dependent on the width (W) of the trace, the thickness (T) of the trace, the dielectric constant of the material used, and the height (H) between the trace and reference plane.

Microstrip Impedance

A circuit trace routed on an outside layer of the PCB with a reference plane (GND or V_{CC}) below it, constitutes a microstrip layout. Use the following microstrip impedance equation to calculate the impedance of a microstrip trace layout:

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left(\frac{5.98 \times H}{0.8W + T} \right) \Omega$$

Using typical values of $W = 8$ mil, $H = 5$ mil, $T = 1.4$ mil, the dielectric constant, and (FR-4) = 4.1, with the microstrip impedance equation, solving for microstrip impedance (Z_0) yields:

$$Z_0 = \frac{87}{\sqrt{4.1 + 1.41}} \ln \left(\frac{5.98 \times (5)}{0.8(8) + 1.4} \right) \Omega$$

$$Z_0 \sim 50 \Omega$$



The measurement unit in the microstrip impedance equation is mils (i.e., 1 mil = 0.001 inches). Also, copper (Cu) trace thickness is usually measured in ounces for example, 1 oz = 1.4 mil).

Figure 11-3 shows microstrip trace impedance with changing trace width (W), using the values in the microstrip impedance equation, keeping dielectric height and trace thickness constant.

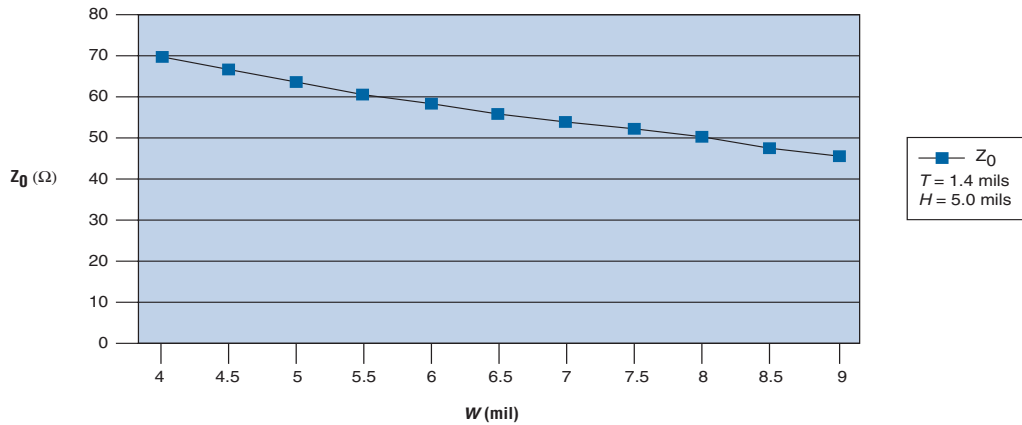
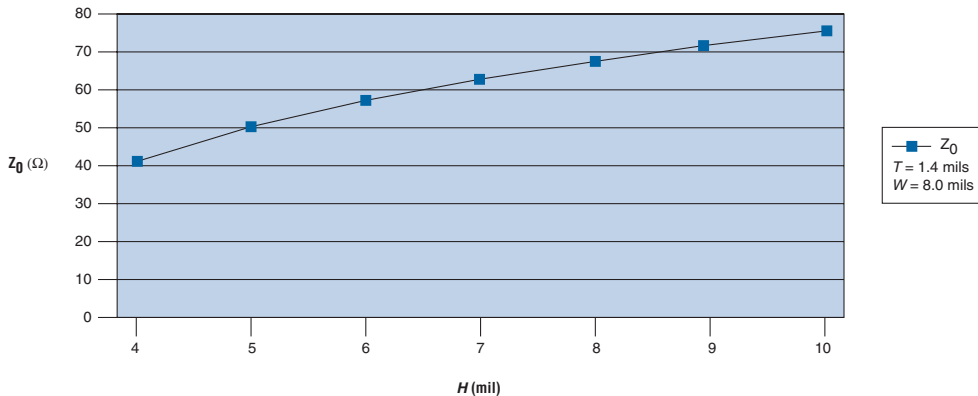
Figure 11–3. Microstrip Trace Impedance with Changing Trace Width

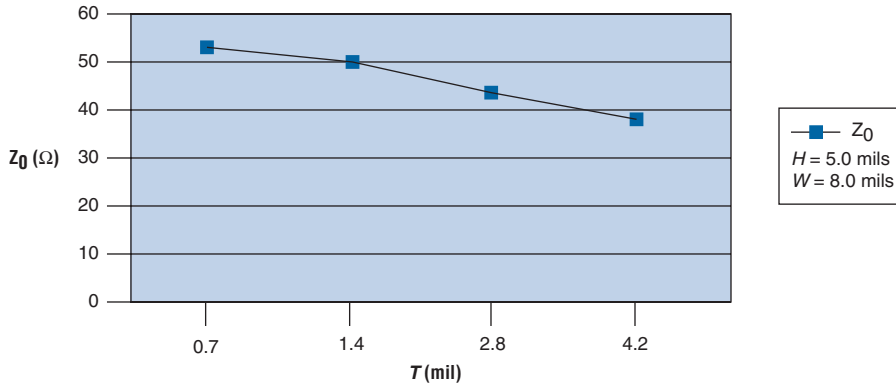
Figure 11–4 shows microstrip trace impedance with changing height, using the values in the microstrip impedance equation, keeping trace width and trace thickness constant.

Figure 11–4. Microstrip Trace Impedance with Changing Height

The impedance graphs show that the change in impedance is inversely proportional to trace width and directly proportional to trace height above the ground plane.

Figure 11–5 plots microstrip trace impedance with changing trace thickness using the values in the microstrip impedance equation, keeping trace width and dielectric height constant. Figure 11–5 shows that as trace thickness increases, trace impedance decreases.

Figure 11–5. Microstrip Trace Impedance with Changing Trace Thickness



Stripline Impedance

A circuit trace routed on the inside layer of the PCB with two low-voltage reference planes (power and/or GND) constitutes a stripline layout. You can use the following stripline impedance equation to calculate the impedance of a stripline trace layout:

$$Z_o = \frac{60}{\sqrt{\epsilon_r}} \ln \left(\frac{4H}{0.67\pi(T + 0.8W)} \right) \Omega$$

Using typical values of $W = 9$ mil, $H = 24$ mil, $T = 1.4$ mil, dielectric constant and (FR-4) = 4.1 with the stripline impedance equation and solving for stripline impedance (Z_o) yields:

$$Z_o = \frac{60}{\sqrt{4.1}} \ln \left(\frac{4(24)}{0.67\pi(1.4) + 0.8(9)} \right) \Omega$$

$$Z_o \sim 50 \Omega$$

Figure 11–6 shows impedance with changing trace width using the stripline impedance equation, keeping height and thickness constant for stripline trace.

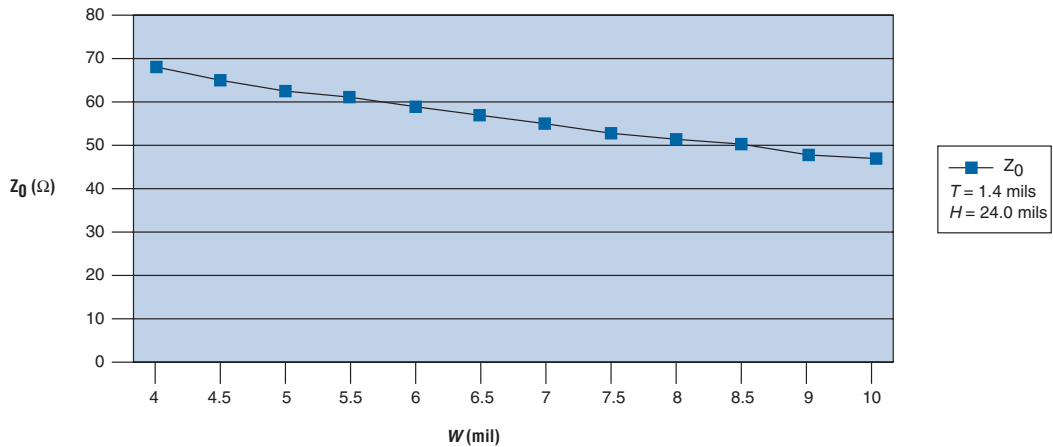
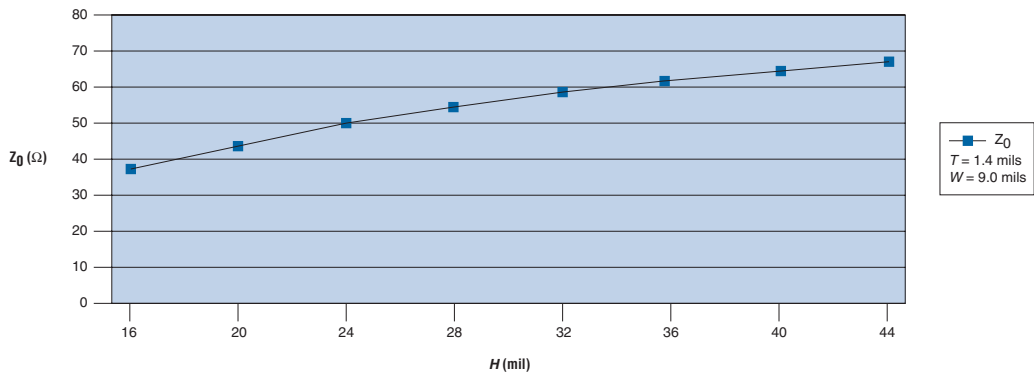
Figure 11–6. Stripline Trace Impedance with Changing Trace Width

Figure 11–7 shows stripline trace impedance with changing dielectric height using the stripline impedance equation, keeping trace width and trace thickness constant.

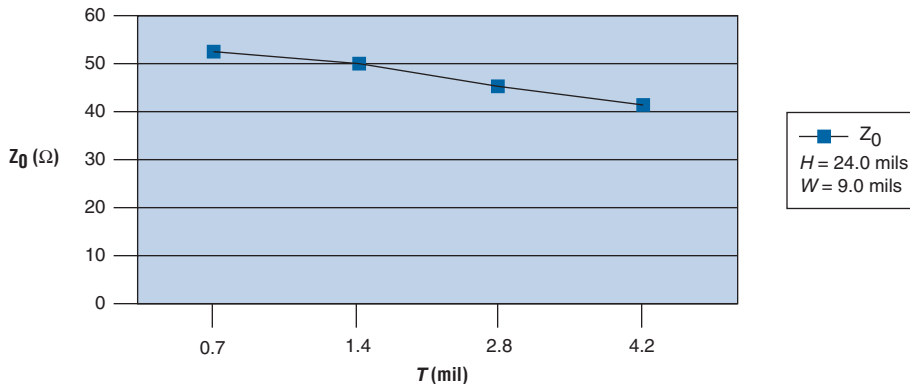
Figure 11–7. Stripline Trace Impedance with Changing Dielectric Height

As with the microstrip layout, the stripline layout impedance also changes inversely proportional to line width and directly proportional to height. However, the rate of change with trace height above GND is much slower in a stripline layout compared with a microstrip layout. A stripline layout has a signal sandwiched by FR-4 material, whereas a microstrip layout has one conductor open to air. This exposure causes a higher effective dielectric constant in stripline layouts compared with microstrip

layouts. Thus, to achieve the same impedance, the dielectric span must be greater in stripline layouts compared with microstrip layouts. Therefore, stripline-layout PCBs with controlled impedance lines are thicker than microstrip-layout PCBs.

Figure 11–8 shows stripline trace impedance with changing trace thickness, using the stripline impedance equation, keeping trace width and dielectric height constant. Figure 11–8 shows that the characteristic impedance decreases as the trace thickness increases.

Figure 11–8. Stripline Trace Impedance with Changing Trace Thickness



Propagation Delay

Propagation delay (t_{PD}) is the time required for a signal to travel from one point to another. Transmission line propagation delay is a function of the dielectric constant of the material.

Microstrip Layout Propagation Delay

You can use the following equation to calculate the microstrip trace layout propagation delay:

$$t_{PD} (\text{microstrip}) = 85 \sqrt{0.475\epsilon_r + 0.67}$$

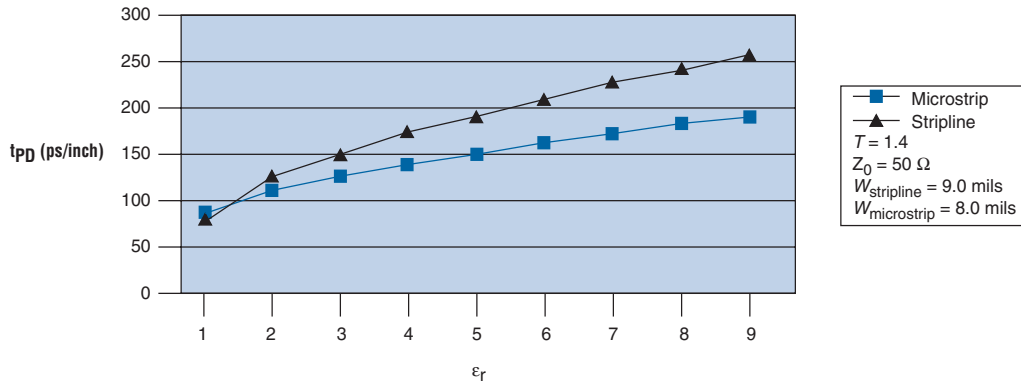
Stripline Layout Propagation Delay

You can use the following equation to calculate the stripline trace layout propagation delay.

$$t_{PD} (\text{stripline}) = 85 \sqrt{\epsilon_r}$$

Figure 11–9 shows the propagation delay versus the dielectric constant for microstrip and stripline traces. As the dielectric constant increases, the propagation delay also increases.

Figure 11–9. Propagation Delay Versus Dielectric Constant for Microstrip & Stripline Traces



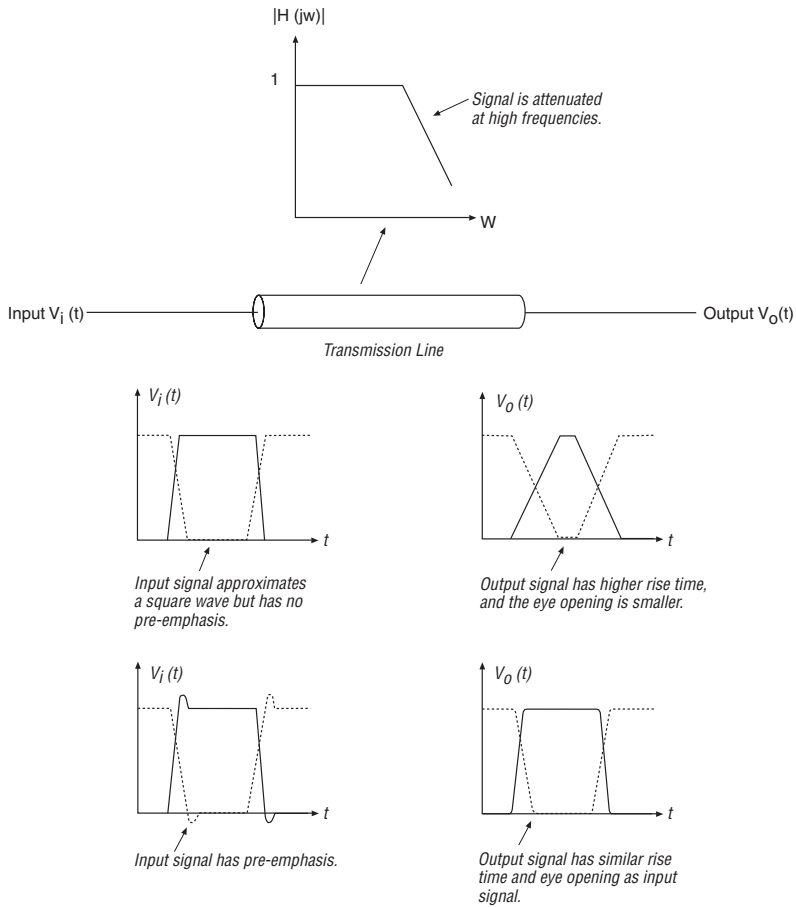
Pre-Emphasis

Typical transmission media like copper trace and coaxial cable have low-pass characteristics, so they attenuate higher frequencies more than lower frequencies. A typical digital signal that approximates a square wave contains high frequencies near the switching region and low frequencies in the constant region. When this signal travels through low-pass media, its higher frequencies are attenuated more than the lower frequencies, resulting in increased signal rise times. Consequently, the eye opening narrows and the probability of error increases.

The high-frequency content of a signal is also degraded by what is called the “skin effect.” The cause of skin effect is the high-frequency current that flows primarily on the surface (skin) of a conductor. The changing current distribution causes the resistance to increase as a function of frequency.

You can use pre-emphasis to compensate for the skin effect. By Fourier analysis, a square wave signal contains an infinite number of frequencies. The high frequencies are located in the low-to-high and high-to-low transition regions and the low frequencies are located in the flat (constant) regions. Increasing the signal’s amplitude near the transition region emphasizes higher frequencies more than the lower frequencies. When this pre-emphasized signal passes through low-pass media, it will come out with minimal distortion, if you apply the correct amount of pre-emphasis (see Figure 11–10).

Figure 11–10. Input & Output Signals with & without Pre-Emphasis



Stratix® II and Stratix GX devices provide programmable pre-emphasis to compensate for variable lengths of transmission media. You can set the pre-emphasis to between 5 and 25%, depending on the value of the output differential voltage (V_{OD}) in the Stratix GX device. [Table 11-2](#) shows the available Stratix GX programmable pre-emphasis settings.

Table 11-2. Programmable Pre-Emphasis with Stratix GX Devices

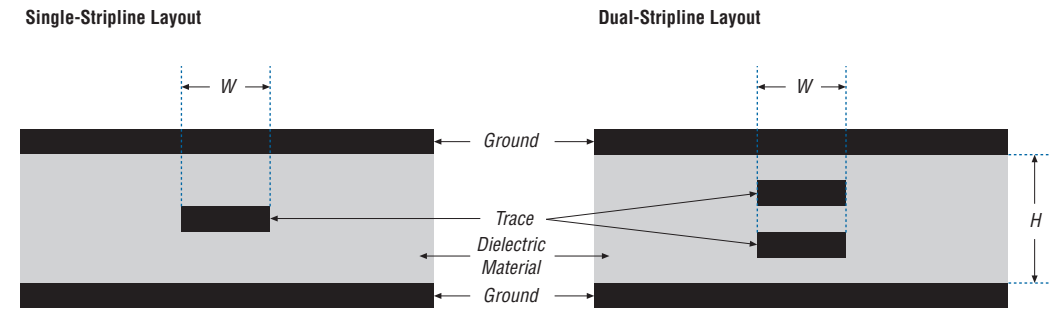
V_{OD}	Pre-emphasis Setting (%)				
	5	10	15	20	25
400	420	440	460	480	500
480	504	528	552	576	600
600	630	660	690	720	750
800	840	880	920	960	1,000
960	1,008	1,056	1,104	1,152	1,200
1,000	1,050	1,100	1,150	1,200	1,250
1,200	1,260	1,320	1,380	1,440	1,500
1,400	1,470	1,540	-	-	-
1,440	1,512	1,584	-	-	-
1,500	1,575	-	-	-	-
1,600	-	-	-	-	-

Routing Schemes for Minimizing Crosstalk & Maintaining Signal Integrity

Crosstalk is the unwanted coupling of signals between parallel traces. Proper routing and layer stack-up through microstrip and stripline layouts can minimize crosstalk.

To reduce crosstalk in dual-stripline layouts that have two signal layers next to each other, route all traces perpendicular, increase the distance between the two signal layers, and minimize the distance between the signal layer and the adjacent reference plane (see [Figure 11-11](#)).

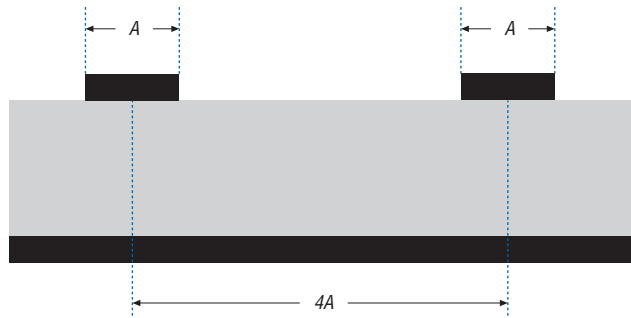
Figure 11–11. Dual- and Single-Stripline Layouts



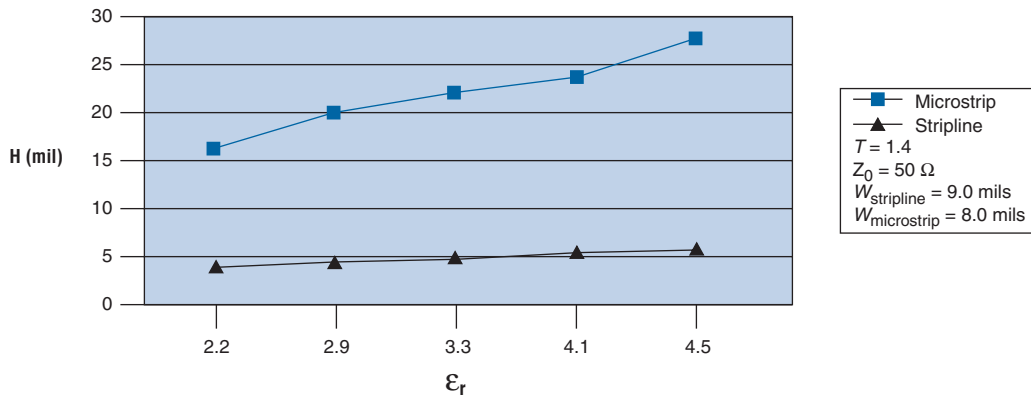
Take the following actions to reduce crosstalk in either microstrip or stripline layouts:

- Widen spacing between signal lines as much as routing restrictions will allow. Try not to bring traces closer than three times the dielectric height.
- Design the transmission line so that the conductor is as close to the ground plane as possible. This technique will couple the transmission line tightly to the ground plane and help decouple it from adjacent signals.
- Use differential routing techniques where possible, especially for critical nets (i.e., match the lengths as well as the turns that each trace goes through).
- If there is significant coupling, route single-ended signals on different layers orthogonal to each other.
- Minimize parallel run lengths between single-ended signals. Route with short parallel sections and minimize long, coupled sections between nets.

Crosstalk also increases when two or more single-ended traces run parallel and are not spaced far enough apart. The distance between the centers of two adjacent traces should be at least four times the trace width, as shown in [Figure 11–12](#). To improve design performance, lower the distance between the trace and the ground plane to under 10 mils without changing the separation between the two traces.

Figure 11–12. Separating Traces for Crosstalk

Compared with high dielectric materials, low dielectric materials help reduce the thickness between the trace and ground plane while maintaining signal integrity. Figure 11–13 plots the relationship of height versus dielectric constant using the microstrip impedance and stripline impedance equations, keeping impedance, width, and thickness constant.

Figure 11–13. Height Versus Dielectric Constant

Signal Trace Routing

Proper routing helps to maintain signal integrity. To route a clean trace, you should perform simulation with good signal integrity tools. The following section describes the two different types of signal traces available for routing, single-ended traces, and differential pair traces.

Single-Ended Trace Routing

A single-ended trace connects the source and the load/receiver. Single-ended traces are used in general point-to-point routing, clock routing, low-speed, and non-critical I/O routing. This section discusses different routing schemes for clock signals. You can use the following types of routing to drive multiple devices with the same clock:

- Daisy chain routing
 - With stub
 - Without stub
- Star routing
- Serpentine routing

Use the following guidelines to improve the clock transmission line's signal integrity:

- Keep clock traces as straight as possible. Use arc-shaped traces instead of right-angle bends.
- Do not use multiple signal layers for clock signals.
- Do not use vias in clock transmission lines. Vias can cause impedance change and reflection.
- Place a ground plane next to the outer layer to minimize noise. If you use an inner layer to route the clock trace, sandwich the layer between reference planes.
- Terminate clock signals to minimize reflection.
- Use point-to-point clock traces as much as possible.

Daisy Chain Routing With Stubs

Daisy chain routing is a common practice in designing PCBs. One disadvantage of daisy chain routing is that stubs, or short traces, are usually necessary to connect devices to the main bus (see [Figure 11-14](#)). If a stub is too long, it will induce transmission line reflections and degrade signal quality. Therefore, the stub length should not exceed the following conditions:

$$TD_{\text{stub}} < (T_{10\% \text{ to } 90\%})/3$$

where TD_{stub} = Electrical delay of the stub

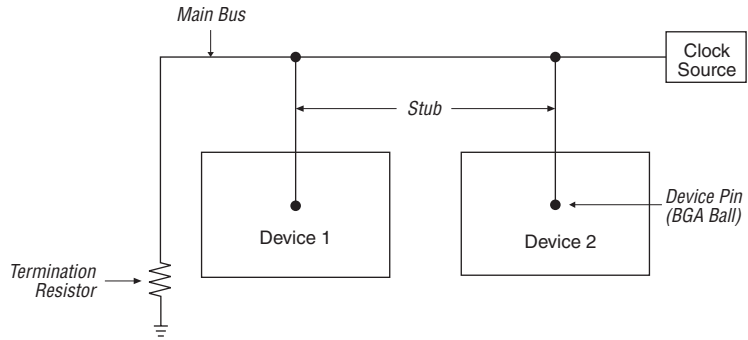
$$T_{10\% \text{ to } 90\%} = \text{Rise or fall time of signal edge}$$

For a 1-ns rise-time edge, the stub length should be less than 0.5 inches (see the “References” section). If your design uses multiple devices, all stub lengths should be equal to minimize clock skew.



If possible, you should avoid using stubs in your PCB design. For high-speed designs, even very short stubs can create signal integrity problems.

Figure 11-14. Daisy Chain Routing with Stubs



Figures 11-15 through 11-17 show the SPICE simulation with different stub length. As the stub length decreases, there is less reflection noise, which causes the eye opening to increase.

Figure 11-15. Stub Length = 0.5 Inch

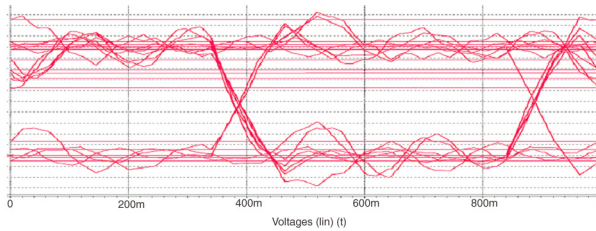


Figure 11-16. Stub Length = 0.25 Inch

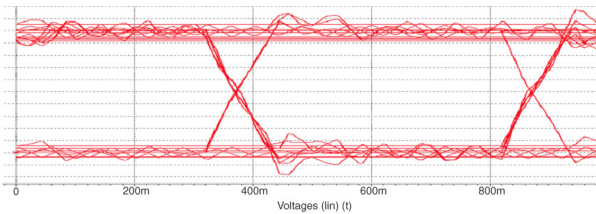
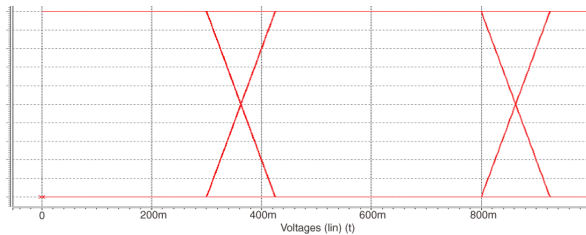


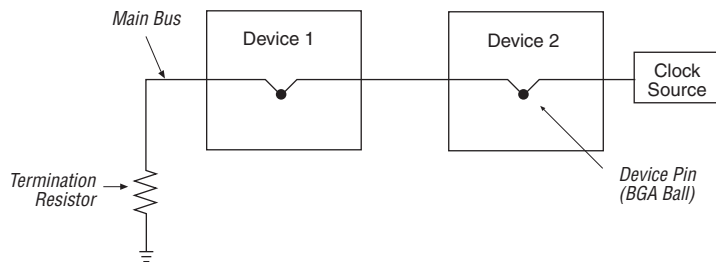
Figure 11-17. Stub Length = Zero Inches



Daisy Chain Routing without Stubs

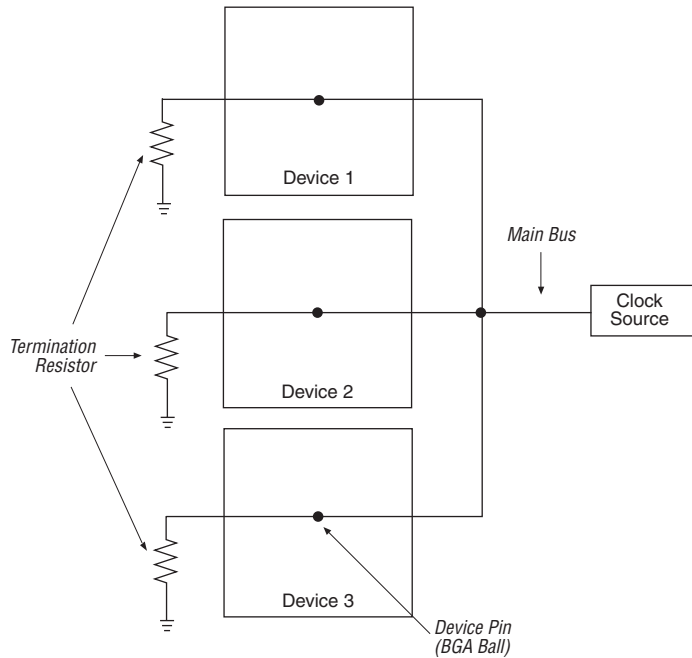
Figure 11-18 shows daisy chain routing with the main bus running through the device pins, eliminating stubs. This layout removes the risk of impedance mismatch between the main bus and the stubs, minimizing signal integrity problems.

Figure 11-18. Daisy Chain Routing without Stubs



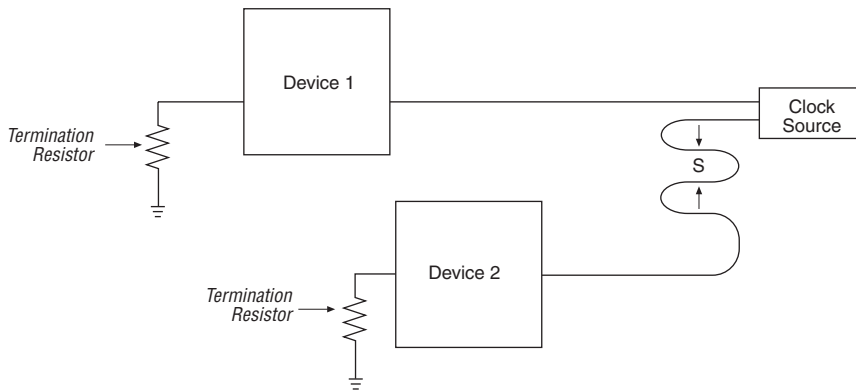
Star Routing

In star routing, the clock signal travels to all the devices at the same time (see Figure 11-19). Therefore, all trace lengths between the clock source and devices must be matched to minimize the clock skew. Each load should be identical to minimize signal integrity problems. In star routing, you must match the impedance of the main bus with the impedance of the long trace that connects to multiple devices.

Figure 11–19. Star Routing**Serpentine Routing**

When a design requires equal-length traces between the source and multiple loads, you can bend some traces to match trace lengths (see [Figure 11–20](#)). However, improper trace bending affects signal integrity and propagation delay. To minimize crosstalk, ensure that $S \geq 3 \times H$, where S is the spacing between the parallel sections and H is the height of the signal trace above the reference ground plane (see [Figure 11–21](#)).

Figure 11–20. Serpentine Routing

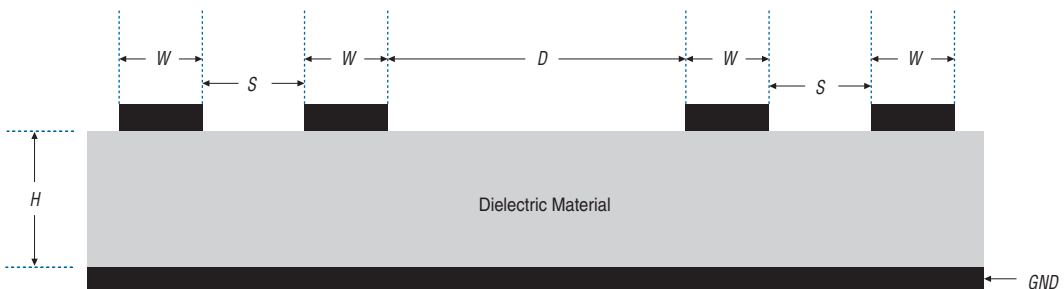


Altera recommends avoiding serpentine routing, if possible. Instead, use arcs to create equal-length traces.

Differential Trace Routing

To maximize signal integrity, proper routing techniques for differential signals are important for high-speed designs. Figure 11–21 shows two differential pairs using the microstrip layout.

Figure 11–21. Differential Trace Routing Note (1)



Note to Figure 11–21:

- (1) D = distance between two differential pair signals; W = width of a trace in a differential pair; S = distance between the trace in a differential pair; and H = dielectric height above the group plane.

Use the following guidelines when using two differential pairs:

- Keep the distance between the differential traces (S) constant over the entire trace length.

- Ensure that $D > 2S$ to minimize the crosstalk between the two differential pairs.
- Place the differential traces $S = 3H$ as they leave the device to minimize reflection noise.
- Keep the length of the two differential traces the same to minimize the skew and phase difference.
- Avoid using multiple vias because they can cause impedance mismatch and inductance.

Termination Schemes

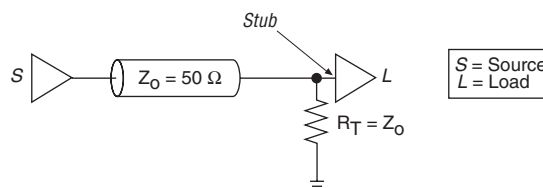
Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing at the load receiver. The ringing reduces the dynamic range of the receiver and can cause false triggering. To eliminate reflections, the impedance of the source (Z_S) must equal the impedance of the trace (Z_0), as well as the impedance of the load (Z_L). This section discusses the following signal termination schemes:

- Simple parallel termination
- Thevenin parallel termination
- Active parallel termination
- Series-RC parallel termination
- Series termination
- Differential pair termination

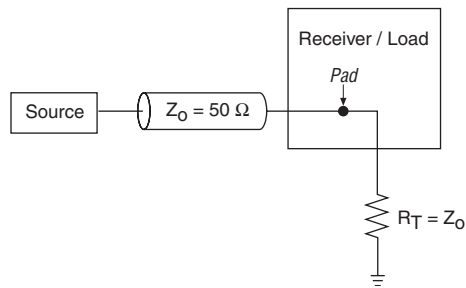
Simple Parallel Termination

In a simple parallel termination scheme, the termination resistor (R_T) is equal to the line impedance. Place the R_T as close to the load as possible to be efficient (see [Figure 11-22](#)).

Figure 11-22. Simple Parallel Termination

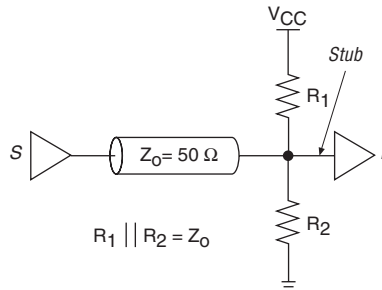


The stub length from the R_T to the receiver pin and pads should be as small as possible. A long stub length causes reflections from the receiver pads, resulting in signal degradation. If your design requires a long termination line between the terminator and receiver, the placement of the resistor becomes important. For long termination line lengths, use fly-by termination (see [Figure 11-23](#)).

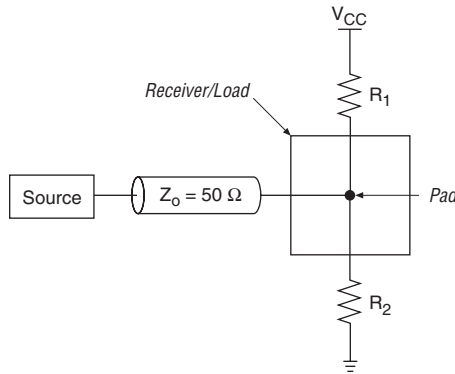
Figure 11–23. Simple Parallel Fly-By Termination

Thevenin Parallel Termination

An alternative parallel termination scheme uses a Thevenin voltage divider (see [Figure 11–24](#)). The R_T is split between R_1 and R_2 , which equals the line impedance when combined.

Figure 11–24. Thevenin Parallel Termination

As noted in the previous section, stub length is dependent on signal rise and fall time and should be kept to a minimum. If your design requires a long termination line between the terminator and receiver, use fly-by termination or Thevenin fly-by termination (see [Figures 11–23](#) and [11–25](#)).

Figure 11–25. Thevenin Parallel Fly-By Termination

Active Parallel Termination

Figure 11–26 shows an active parallel termination scheme, where the terminating resistor ($R_T = Z_0$) is tied to a bias voltage (V_{BIAS}). In this scheme, the voltage is selected so that the output drivers can draw current from the high- and low-level signals. However, this scheme requires a separate voltage source that can sink and source currents to match the output transfer rates.

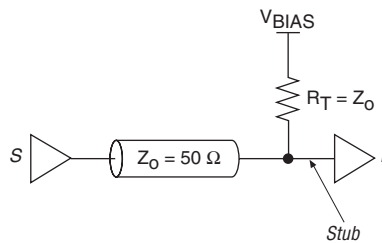
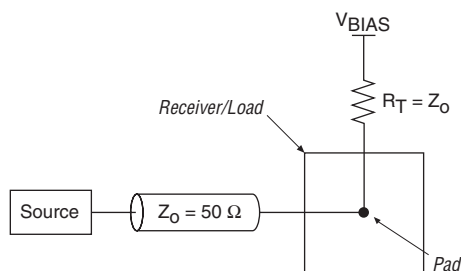
Figure 11–26. Active Parallel Termination

Figure 11-27 shows the active parallel fly-by termination scheme.

Figure 11-27. Active Parallel Fly-By Termination



Series-RC Parallel Termination

A series-RC parallel termination scheme uses a resistor and capacitor (series-RC) network as the terminating impedance. R_T is equal to Z_0 . The capacitor must be large enough to filter the constant flow of DC current. For data patterns with long strings of 1 or 0, this termination scheme may delay the signal beyond the design thresholds, depending on the size of the capacitor.

Capacitors smaller than 100 pF diminish the effectiveness of termination. The capacitor blocks low-frequency signals while passing high-frequency signals. Therefore, the DC loading effect of R_T does not have an impact on the driver, as there is no DC path to ground. The series-RC termination scheme requires balanced DC signaling, the signals spend half the time on and half the time off. AC termination is typically used if there is more than one load (see Figure 11-28).

Figure 11-28. Series-RC Parallel Termination

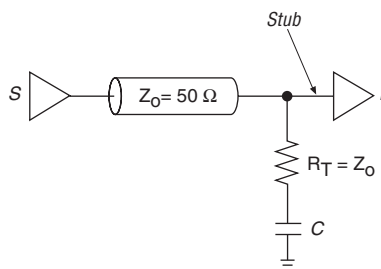
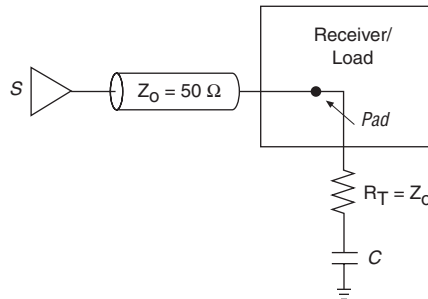


Figure 11–29 shows series-RC parallel fly-by termination.

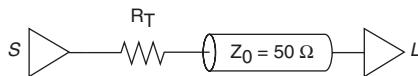
Figure 11–29. Series-RC Parallel Fly-By Termination



Series Termination

In a series termination scheme, the resistor matches the impedance at the signal source instead of matching the impedance at each load (see Figure 11–30). Stratix II devices have programmable output impedance. You can choose output impedance to match the line impedance without adding an external series resistor. The sum of R_T and the impedance of the output driver should be equal to Z_0 . Because Altera device output impedance is low, you should add a series resistor to match the signal source to the line impedance. The advantage of series termination is that it consumes little power. However, the disadvantage is that the rise time degrades because of the increased RC time constant. Therefore, for high-speed designs, you should perform the pre-layout signal integrity simulation with Altera I/O buffer information specification (IBIS) models before using the series termination scheme.

Figure 11–30. Series Termination



Differential Pair Termination

Differential signal I/O standards require an R_T between the signals at the receiving device (see Figure 11–31). For the low-voltage differential signal (LVDS) and low-voltage positive emitter-coupled logic (LVPECL) standard, the R_T should match the differential load impedance of the bus (typically 100 Ω).

Figure 11–31. Differential Pair (LVDS & LVPECL) Termination

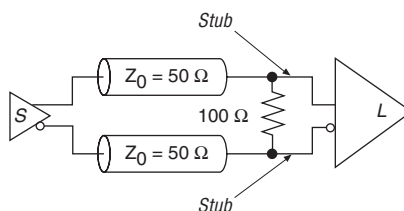
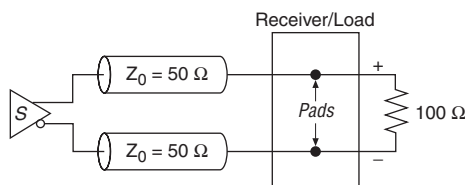


Figure 11–32 shows the differential pair fly-by termination scheme for the LVDS and LVPECL standard.

Figure 11–32. Differential Pair (LVDS & LVPECL) Fly-By Termination



See the *Board Design Guidelines for LVDS Systems* White Paper for more information on terminating differential signals.

Simultaneous Switching Noise

As digital devices become faster, their output switching times decrease. This causes higher transient currents in outputs as the devices discharge load capacitances. These higher transient currents result in a board-level phenomenon known as ground bounce.

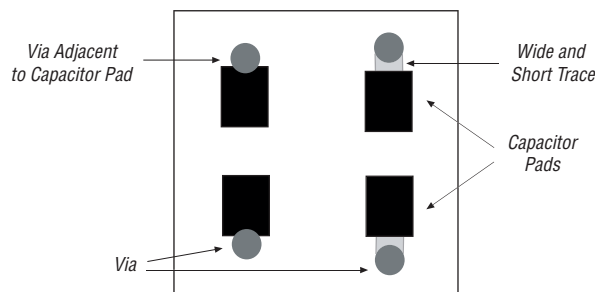
Because many factors contribute to ground bounce, you cannot use a standard test method to predict its magnitude for all possible PCB environments. You can only test the device under a given set of conditions to determine the relative contributions of each condition and of the device itself. Load capacitance, socket inductance, and the number of switching outputs are the predominant factors that influence the magnitude of ground bounce in FPGAs.

Altera requires 0.01- to 0.1- μF surface-mount capacitors in parallel to reduce ground bounce. Add an additional 0.001- μF capacitor in parallel to these capacitors to filter high-frequency noise (>100 MHz). You can also add 0.0047- μF and 0.047- μF capacitors.

Altera recommends that you take the following action to reduce ground bounce and V_{CC} sag:

- Configure unused I/O pins as output pins, and drive the output low to reduce ground bounce. This configuration will act as a virtual ground. Connect the output pin to GND on your board.
- Configure the unused I/O pins as output, and drive high to prevent V_{CC} sag. Connect the output pin to V_{CCIO} of that I/O bank.
- Create a programmable ground or V_{CC} next to switching pins.
- Reduce the number of outputs that can switch simultaneously and distribute them evenly throughout the device.
- Manually assign ground pins in between I/O pins. (Separating I/O pins with ground pins prevents ground bounce.)
- Set the programmable drive strength feature with a weaker drive strength setting to slow down the edge rate.
- Eliminate sockets whenever possible. Sockets have inductance associated with them.
- Depending on the problem, move switching outputs close to either a package ground or V_{CC} pin. Eliminate pull-up resistors, or use pull-down resistors.
- Use multi-layer PCBs that provide separate V_{CC} and ground planes to utilize the intrinsic capacitance of the V_{CC} /GND plane.
- Create synchronous designs that are not affected by momentarily switching pins.
- Add the recommended decoupling capacitors to V_{CC} /GND pairs.
- Place the decoupling capacitors as close as possible to the power and ground pins of the device.
- Connect the capacitor pad to the power and ground plane with larger vias to minimize the inductance in decoupling capacitors and allow for maximum current flow.
- Use wide, short traces between the vias and capacitor pads, or place the via adjacent to the capacitor pad (see [Figure 11–33](#)).

Figure 11–33. Suggested Via Location that Connects to Capacitor Pad



- Traces stretching from power pins to a power plane (or island, or a decoupling capacitor) should be as wide and as short as possible. This reduces series inductance, thereby reducing transient voltage drops from the power plane to the power pin which, in turn, decreases the possibility of ground bounce.
- Use surface-mount low effective series resistance (ESR) capacitors to minimize the lead inductance. The capacitors should have an ESR value as small as possible.
- Connect each ground pin or via to the ground plane individually. A daisy chain connection to the ground pins shares the ground path, which increases the return current loop and thus inductance.

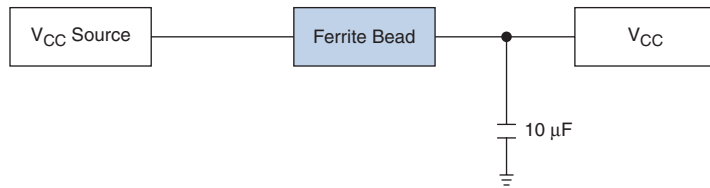
Power Filtering & Distribution

You can reduce system noise by providing clean, evenly distributed power to V_{CC} on all boards and devices. This section describes techniques for distributing and filtering power.

Filtering Noise

To decrease the low-frequency (< 1 kHz) noise caused by the power supply, filter the noise on power lines at the point where the power connects to the PCB and to each device. Place a 100- μ F electrolytic capacitor where the power supply lines enter the PCB. If you use a voltage regulator, place the capacitor immediately after the pin that provides the V_{CC} signal to the device(s). Capacitors not only filter low-frequency noise from the power supply, but also supply extra current when many outputs switch simultaneously in a circuit.

To filter power supply noise, use a non-resonant, surface-mount ferrite bead large enough to handle the current in series with the power supply. Place a 10- to 100- μ F bypass capacitor next to the ferrite bead (see [Figure 11–34](#)). (If proper termination, layout, and filtering eliminate enough noise, you do not need to use a ferrite bead.) The ferrite bead acts as a short for high-frequency noise coming from the V_{CC} source. Any low-frequency noise is filtered by a large 10- μ F capacitor after the ferrite bead.

Figure 11–34. Filtering Noise with a Ferrite Bead

Usually, elements on the PCB add high-frequency noise to the power plane. To filter the high-frequency noise at the device, place decoupling capacitors as close as possible to each V_{CC} and GND pair.



See the *Operating Requirements for Altera Devices* Data Sheet for more information on bypass capacitors.

Power Distribution

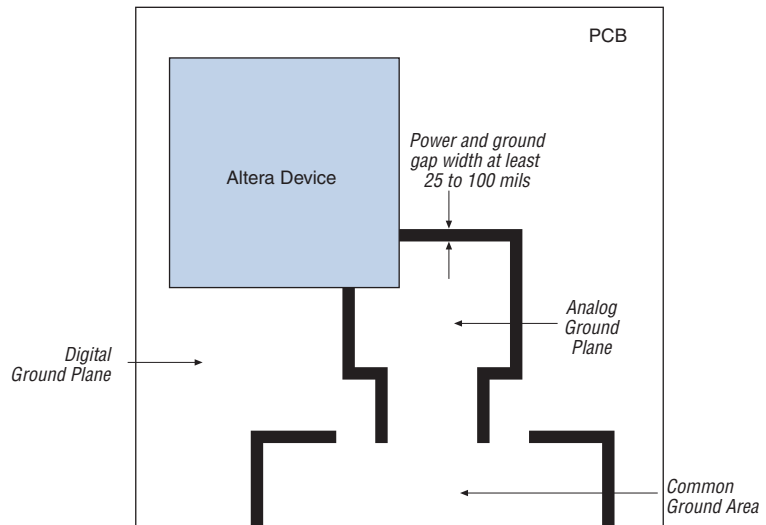
A system can distribute power throughout the PCB with either power planes or a power bus network.

You can use power planes on multi-layer PCBs that consist of two or more metal layers that carry V_{CC} and GND to the devices. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains V_{CC} and distributes it equally to all devices while providing very high current-sink capability, noise protection, and shielding for the logic signals on the PCB. Altera recommends using power planes to distribute power.

The power bus network—which consists of two or more wide-metal traces that carry V_{CC} and GND to devices—is often used on two-layer PCBs and is less expensive than power planes. When designing with power bus networks, be sure to keep the trace widths as wide as possible. The main drawback to using power bus networks is significant DC resistance.

Altera recommends using separate analog and digital power planes. For fully digital systems that do not already have a separate analog power plane, it can be expensive to add new power planes. However, you can create partitioned islands (split planes). [Figure 11–35](#) shows an example board layout with phase-locked loop (PLL) ground islands.

Figure 11–35. Board Layout for General-Purpose PLL Ground Islands



If your system shares the same plane between analog and digital power supplies, there may be unwanted interaction between the two circuit types. The following suggestions will reduce noise:

- For equal power distribution, use separate power planes for the analog (PLL) power supply. Avoid using trace or multiple signal layers to route the PLL power supply.
- Use a ground plane next to the PLL power supply plane to reduce power-generated noise.
- Place analog and digital components only over their respective ground planes.
- Use ferrite beads to isolate the PLL power supply from digital power supply.

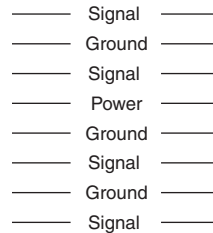
Electromagnetic Interference (EMI)

Electromagnetic interference (EMI) is directly proportional to the change in current or voltage with respect to time. EMI is also directly proportional to the series inductance of the circuit. Every PCB generates EMI. Precautions such as minimizing crosstalk, proper grounding, and proper layer stack-up significantly reduce EMI problems.

Place each signal layer in between the ground plane and power (or ground) plane. Inductance is directly proportional to the distance an electric charge has to cover from the source of an electric charge to ground. As the distance gets shorter, the inductance becomes smaller.

Therefore, placing ground planes close to a signal source reduces inductance and helps contain EMI. Figure 11–36 shows an example of an eight-layer stack-up. In the stack-up, the stripline signal layers are the quietest because they are centered by power and GND planes. A solid ground plane next to the power plane creates a set of low ESR capacitors. With integrated circuit edge rates becoming faster and faster, these techniques help to contain EMI.

Figure 11–36. Example Eight-Layer Stack-Up



Component selection and proper placement on the board is important to controlling EMI.

The following guidelines can reduce EMI:

- Select low-inductance components, such as surface mount capacitors with low ESR, and effective series inductance.
- Use proper grounding for the shortest current return path.
- Use solid ground planes next to power planes.
- In unavoidable circumstances, use respective ground planes next to each segmented power plane for analog and digital circuits.

Additional FPGA-Specific Information

This section provides the following additional information recommended by Altera for board design and signal integrity: FPGA-specific configuration, Joint Test Action Group (JTAG) testing, and permanent test points.

Configuration

The DCLK signal is used in configuration devices and passive serial (PS) and passive parallel synchronous (PPS) configuration schemes. This signal drives edge-triggered pins in Altera devices. Therefore, any overshoot, undershoot, ringing, crosstalk, or other noise can affect configuration. Use the same guidelines for designing clock signals to

route the DCLK trace (see the “[Signal Trace Routing](#)” section). If your design uses more than five configuration devices, Altera recommends using buffers to split the fan-out on the DCLK signal.

JTAG

As PCBs become more complex, testing becomes increasingly important. Advances in surface mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods such as external test probes and “bed-of-nails” test fixtures harder to implement. As a result, cost savings from PCB space reductions can be offset by cost increases in traditional testing methods.

In addition to boundary scan testing (BST), you can use the IEEE Std. 1149.1 controller for in-system programming. JTAG consists of four required pins, test data input (TDI), test data output (TDO), test mode select (TMS), and test clock input (TCK) as well as an optional test reset input (TRST) pin.

Use the same guidelines for laying out clock signals to route TCK traces. Use multiple devices for long JTAG scan chains. Minimize the JTAG scan chain trace length that connects one device’s TDO pins to another device’s TDI pins to reduce delay.



See *Application Note 39: IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices* for additional details on BST.

Test Point

As device package pin density increases, it becomes more difficult to attach an oscilloscope or a logic analyzer probe on the device pin. Using a physical probe directly on to the device pin can damage the device. If the ball grid array (BGA) or FineLine BGA® package is mounted on top of the board, it is difficult to probe the other side of the board. Therefore, the PCB must have a permanent test point to probe. The test point can be a via that connects to the signal under test with a very short stub. However, placing a via on a trace for a signal under test can cause reflection and poor signal integrity.

Summary

You must carefully plan out a successful high-speed PCB. Factors such as noise generation, signal reflection, crosstalk, and ground bounce can interfere with a signal, especially with the high speeds that Altera devices transmit and receive. The signal routing, termination schemes, and power distribution techniques discussed in this chapter contribute to a more effectively designed PCB using high-speed Altera devices.

References

Johnson, H. W., and Graham, M., *“High-Speed Digital Design.”* Prentice Hall, 1993.

Hall, S. H., Hall, G. W., and McCall J. A., *“High-Speed Digital System Design.”* John Wiley & Sons, Inc. 2000.

Document Revision History

Table 11–3 shows the revision history for this chapter.

<i>Table 11–3. Document Revision History</i>		
Date and Document Version	Changes Made	Summary of Changes
May 2007, v1.4	Updated “ Simultaneous Switching Noise ” section.	—
	Moved the Document Revision History section to the end of the chapter.	—
December 2005, v1.3	Minor content update.	—
March 2005, v1.2	Minor content updates.	—
January 2005, v1.1	This chapter was formally chapter 12.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

