

Introduction

Stratix® II and Stratix II GX devices support a broad range of external memory interfaces such as double data rate (DDR) SDRAM, DDR2 SDRAM, RLDRAM II, QDR II SRAM, and single data rate (SDR) SDRAM. Its dedicated phase-shift circuitry allows the Stratix II or Stratix II GX device to interface with an external memory at twice the system clock speed (up to 300 MHz/600 megabits per second (Mbps) with RLDRAM II). In addition to external memory interfaces, you can also use the dedicated phase-shift circuitry for other applications that require a shifted input signal.

Typical I/O architectures transmit a single data word on each positive clock edge and are limited to the associated clock speed. To achieve a 400-Mbps transfer rate, a SDR system requires a 400-MHz clock. Many new applications have introduced a DDR I/O architecture as an alternative to SDR architectures. While SDR architectures capture data on one edge of a clock, the DDR architectures captures data on both the rising and falling edges of the clock, doubling the throughput for a given clock frequency and accelerating performance. For example, a 200-MHz clock can capture a 400-Mbps data stream, enhancing system performance and simplifying board design.

Most new memory architectures use a DDR I/O interface. Although Stratix II and Stratix II GX devices also support the mature and well established SDR external memory, this chapter focuses on DDR memory standards. These DDR memory standards cover a broad range of applications for embedded processor systems, image processing, storage, communications, and networking.

Stratix II devices offer external memory support in every I/O bank. The side I/O banks support the PLL-based interfaces running at up to 200 MHz, while the top and bottom I/O banks support PLL- and DLL-based interfaces. [Figure 9-1](#) shows Stratix II device memory support.

Figure 9–1. External Memory Support

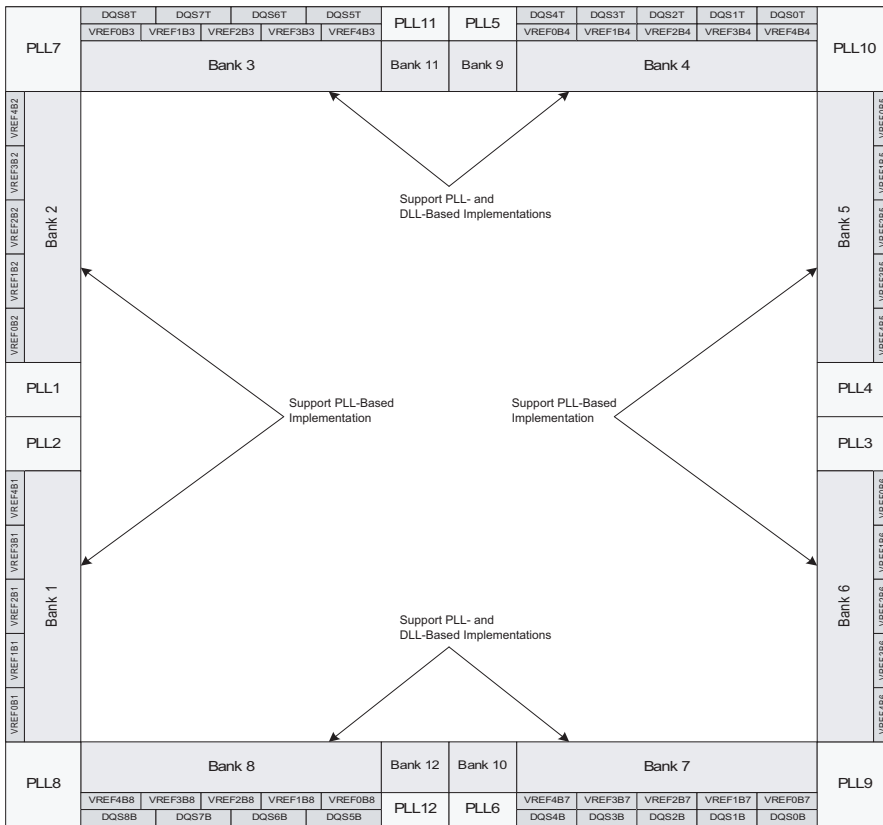


Table 9–1 summarizes the maximum clock rate Stratix II and Stratix II GX devices can support with external memory devices.

Table 9–1. Stratix II and Stratix II GX Maximum Clock Rate Support for External Memory Interfaces
Notes (1), (2)

Memory Standards	–3 Speed Grade (MHz)		–4 Speed Grade (MHz)		–5 Speed Grade (MHz)	
	DLL-Based	PLL-Based	DLL-Based	PLL-Based	DLL-Based	PLL-Based
DDR2 SDRAM (3), (5)	333	200	267	167	233	167
DDR SDRAM (3)	200	150	200	133	200	100
RLDRAM II	300	200	250 (4)	175	200	175
QDR II SRAM	300	200	250	167	250	167
QDR II+ SRAM	300	(6)	250	(6)	250	(6)

Notes to Table 9–1:

- (1) Memory interface timing specifications are dependent on the memory, board, physical interface, and core logic. Refer to each memory interface application note for more details on how each specification was generated.
- (2) The respective Altera MegaCore function and the EP2S60F1020C3 timing information featured in the Quartus® II software version 6.0 was used to define these clock rates.
- (3) This applies for interfaces with both modules and components.
- (4) You must underclock a 300-MHz RLDRAM II device to achieve this clock rate.
- (5) To achieve speeds greater than 267 MHz (533 Mbps) up to 333 MHz (667 Mbps), you must use the Altera DDR2 SDRAM Controller MegaCore function that features a new dynamic auto-calibration circuit in the data path for resynchronization. For more information, see the Altera web site at www.altera.com. For interfaces running at 267 MHz or below, continue to use the static resynchronization data path currently supported by the released version of the MegaCore function.
- (6) The lowest frequency at which a QDR II+ SRAM device can operate is 238 MHz. Therefore, the PLL-based implementation does not support the QDR II+ SRAM interface.

This chapter describes the hardware features in Stratix II and Stratix II GX devices that facilitate the high-speed memory interfacing for each DDR memory standard. This chapter focuses primarily on the DLL-based implementation. The PLL-based implementation is described in application notes. It then lists the Stratix II and Stratix II GX feature enhancements from Stratix devices and briefly explains how each memory standard uses the Stratix II and Stratix II GX features.



You can use this document with the following documents:

- AN 325: Interfacing RLDRAM II with Stratix II & Stratix GX Devices
- AN 326: Interfacing QDR II & QDR II+ SRAM with Stratix II, Stratix, & Stratix GX Devices
- AN 327: Interfacing DDR SDRAM with Stratix II Devices
- AN 328: Interfacing DDR2 SDRAM with Stratix II Devices

External Memory Standards

The following sections briefly describe the external memory standards supported by Stratix II and Stratix II GX devices. Altera offers a complete solution for these memories, including clear-text data path, memory controller, and timing analysis.

DDR and DDR2 SDRAM

DDR SDRAM is a memory architecture that transmits and receives data at twice the clock speed. These devices transfer data on both the rising and falling edge of the clock signal. DDR2 SDRAM is a second generation memory based on the DDR SDRAM architecture and transfers data to Stratix II and Stratix II GX devices at up to 333 MHz/667 Mbps. Stratix II and Stratix II GX devices can support DDR SDRAM at up to 200 MHz/400 Mbps. For PLL-based implementations, Stratix II and Stratix II GX devices support DDR and DDR2 SDRAM up to 150 MHz and 200 MHz, respectively.

Interface Pins

DDR and DDR2 SDRAM devices use interface pins such as data (DQ), data strobe (DQS), clock, command, and address pins. Data is sent and captured at twice the system clock rate by transferring data on the clock's positive and negative edge. The commands and addresses still only use one active (positive) edge of a clock. DDR and DDR2 SDRAM use single-ended data strobes (DQS). DDR2 SDRAM can also use optional differential data strobes (DQS and DQS#). However, Stratix II and Stratix II GX devices do not use the optional differential data strobes for DDR2 SDRAM interfaces since DQS and DQSn pins in Stratix II and Stratix II GX devices are not differential. You can leave the DDR SDRAM memory DQS# pin unconnected. Only the shifted DQS signal from the DQS logic block is used to capture data.

DDR and DDR2 SDRAM $\times 16$ devices use two DQS pins, and each DQS pin is associated with eight DQ pins. However, this is not the same as the $\times 16/\times 18$ mode in Stratix II and Stratix II GX devices (see [“Data and Data Strobe Pins” on page 9–14](#)). To support a $\times 16$ DDR SDRAM device, you need to configure Stratix II and Stratix II GX devices to use two sets of DQ pins in $\times 8/\times 9$ mode. Similarly if your $\times 32$ memory device uses four DQS pins where each DQS pin is associated with eight DQ pins, you need to configure Stratix II and Stratix II GX devices to use four sets of DQS/DQ groups in $\times 8/\times 9$ mode.

Connect the memory device's DQ and DQS pins to Stratix II and Stratix II GX DQ and DQS pins, respectively, as listed in Stratix II and Stratix II GX pin tables. DDR and DDR2 SDRAM also uses active-high data mask, DM, pins for writes. You can connect the memory's DM pins

to any of Stratix II and Stratix II GX I/O pins in the same bank as the DQ pins of the FPGA. There is one DM pin per DQS/DQ group in a DDR or DDR2 SDRAM device.

You can also use I/O pins in banks 1, 2, 5, or 6 to interface with DDR and DDR2 SDRAM devices. These banks do not have dedicated circuitry, though, and can only support DDR SDRAM at speeds up to 150 MHz and DDR2 SDRAM at speeds up to 200 MHz. DDR2 SDRAM interfaces using these banks are supported using the SSTL-18 Class I I/O standard.

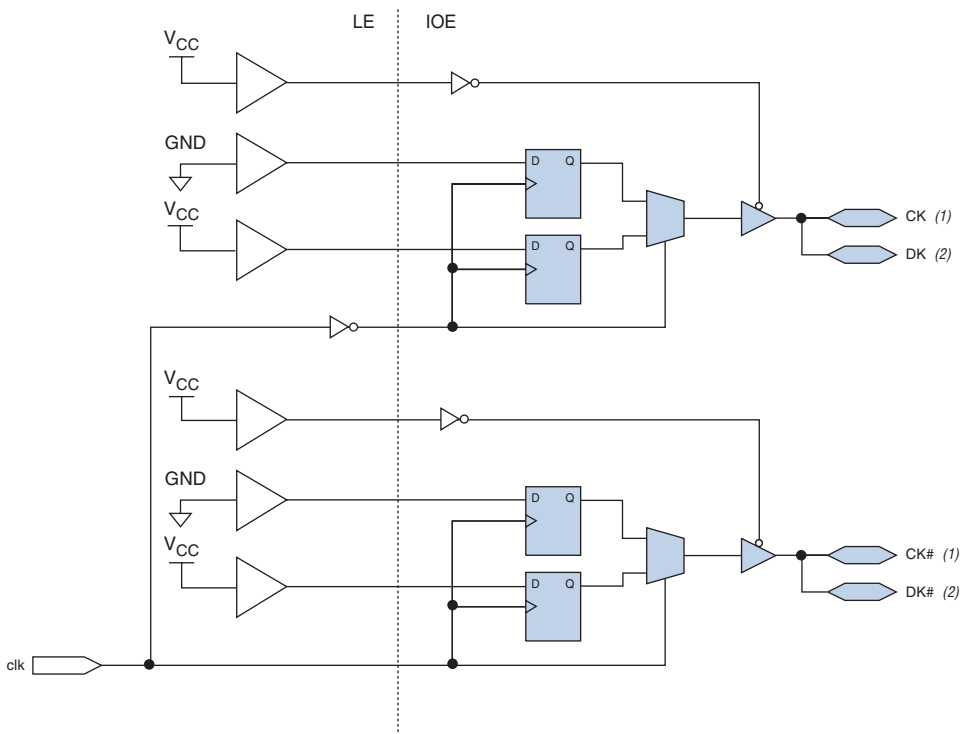


For more information, see [AN 327: Interfacing DDR SDRAM with Stratix II Devices](#) and [AN 328: Interfacing DDR2 SDRAM with Stratix II Devices](#).

If the DDR or DDR2 SDRAM device supports error correction coding (ECC), the design will use an extra DQS/DQ group for the ECC pins.

You can use any of the user I/O pins for commands and addresses to the DDR and DDR2 SDRAM. You may need to generate these signals from the system clock's negative edge.

The clocks to the SDRAM device are called CK and CK# pins. Use any of the user I/O pins via the DDR registers to generate the CK and CK# signals to meet the DDR SDRAM or DDR2 SDRAM device's t_{DQSS} requirement. The memory device's t_{DQSS} specification requires that the write DQS signal's positive edge must be within 25% of the positive edge of the DDR SDRAM or DDR2 SDRAM clock input. Using regular I/O pins for CK and CK# also ensures that any PVT variations on the DQS signals are tracked the same way by these CK and CK# pins. [Figure 9-2](#) shows a diagram that illustrates how to generate these clocks.

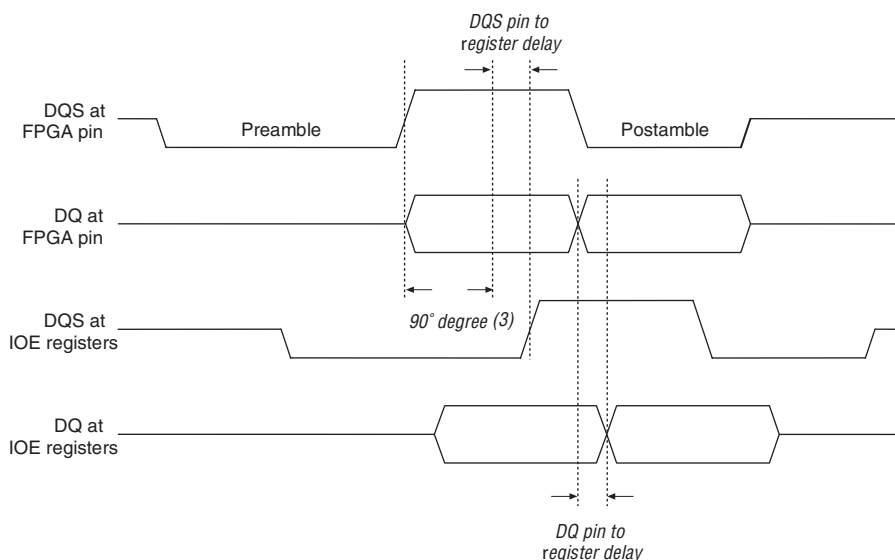
Figure 9–2. Clock Generation for External Memory Interfaces in Stratix II and Stratix II GX Devices

Notes to Figure 9–2:

- (1) CK and CK# are the clocks to the memory devices.
- (2) DK and DK# are for RLD RAM II interfaces. You can generate DK# and DK from separate pins if the difference of the Quartus II software's reported clock-to-out time for these pins meets the RLD RAM II device's t_{CKDK} specification.

Read and Write Operations

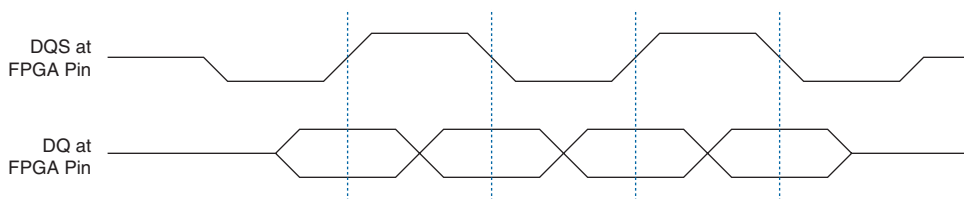
When reading from the memory, DDR and DDR2 SDRAM devices send the data edge-aligned with respect to the data strobe. To properly read the data in, the data strobe needs to be center-aligned with respect to the data inside the FPGA. Stratix II and Stratix II GX devices feature dedicated circuitry to shift this data strobe to the middle of the data window.

Figure 9–3 shows an example of how the memory sends out the data and data strobe for a burst-of-two operation.

Figure 9–3. Example of a 90° Shift on the DQS Signal Notes (1), (2)**Notes to Figure 9–3:**

- (1) RLDRAM II and QDR II SRAM memory interfaces do not have preamble and postamble specifications.
- (2) DDR2 SDRAM does not support a burst length of two.
- (3) The phase shift required for your system should be based on your timing analysis and may not be 90°.

During write operations to a DDR or DDR2 SDRAM device, the FPGA needs to send the data to the memory center-aligned with respect to the data strobe. Stratix II and Stratix II GX devices use a PLL to center-align the data by generating a 0° phase-shifted system clock for the write data strobes and a -90° phase-shifted write clock for the write data pins for DDR and DDR2 SDRAM. Figure 9–4 shows an example of the relationship between the data and data strobe during a burst-of-four write.

Figure 9–4. DQ and DQS Relationship During a DDR and DDR2 SDRAM Write Notes (1), (2)**Notes to Figure 9–4:**

- (1) This example shows a write for a burst length of four. DDR SDRAM also supports burst lengths of two.
- (2) The write clock signals never go to hi-Z state on RLDRAM II and QDR II SRAM memory interfaces because they use free-running clocks. However, the general timing relationship between data and the read clock shown in this figure still applies.



For more information on DDR SDRAM and DDR2 SDRAM specifications, refer to JEDEC standard publications JESD79C and JESD79-2, respectively, from www.jedec.org, or see [AN 327: Interfacing DDR SDRAM with Stratix II Devices](#) and [AN 327: Interfacing DDR SDRAM with Stratix II Devices](#).

RLDRAM II

RLDRAM II provides fast random access as well as high bandwidth and high density, making this memory technology ideal for high-speed network and communication data storage applications. The fast random access speeds in RLDRAM II devices make them a viable alternative to SRAM devices at a lower cost. Additionally, RLDRAM II devices have minimal latency to support designs that require fast response times.

Interface Pins

RLDRAM II devices use interface pins such as data, clock, command, and address pins. There are two types of RLDRAM II memory: common I/O (CIO) and separate I/O (SIO). The data pins in a RLDRAM II CIO device are bidirectional while the data pins in a RLDRAM II SIO device are unidirectional. Instead of bidirectional data strobes, RLDRAM II uses differential free-running read and write clocks to accompany the data. As in DDR or DDR2 SDRAM, data is sent and captured at twice the system clock rate by transferring data on the clock's positive and negative edge. The commands and addresses still only use one active (positive) edge of a clock.

If the data pins are bidirectional, as in RLDRAM II CIO devices, connect them to Stratix II and Stratix II GX DQ pins. If the data pins are unidirectional, as in RLDRAM II SIO devices, connect the RLDRAM II device Q ports to the Stratix II and Stratix II GX device DQ pins and

connect the D ports to any user I/O pins in I/O banks 3, 4, 7, or 8 for optimal performance. RLDRAM II also uses active-high data mask, DM, pins for writes. You can connect DM pins to any of the I/O pins in the same bank as the DQ pins of the FPGA when interfacing with RLDRAM II CIO devices to any of the I/O pins in the same bank as the D pins when interfacing with RLDRAM II SIO devices. There is one DM pin per RLDRAM II device. You can also use I/O pins in banks 1, 2, 5, or 6 to interface with RLDRAM II devices. However, these banks do not have dedicated circuitry and can only support RLDRAM II devices at speeds up to 200 MHz. RLDRAM II interfaces using these banks are supported using the 1.8-V HSTL Class I I/O support.

Connect the RLDRAM II device's read clock pins (QK) to Stratix II or Stratix II GX DQS pins. Because of software requirements, you must configure the DQS signals as bidirectional pins. However, since QK pins are output-only pins from the memory, RLDRAM II memory interfacing in Stratix II and Stratix II GX devices requires that you ground the DQS pin output enables. Stratix II and Stratix II GX devices use the shifted QK signal from the DQS logic block to capture data. You can leave the QK# signal of the RLDRAM II device unconnected, as DQS and DQSn in Stratix II and Stratix II GX devices are not differential pins.

RLDRAM II devices also have input clocks (CK and CK#) and write clocks (DK and DK#).

You can use any of the user I/O pins for commands and addresses. RLDRAM II also offers QVLD pins to indicate the read data availability. Connect the QVLD pins to the Stratix II or Stratix II GX DQVLD pins, listed in the pin table.



Because the Quartus II software treats the DQVLD pins like DQ pins, you should ensure that the DQVLD pin is assigned to the pin table's recommended pin.

Read and Write Operations

When reading from the RLDRAM II device, data is sent edge-aligned with the read clock QK and QK#. When writing to the RLDRAM II device, data must be center-aligned with the write clock (DK and DK#). The RLDRAM II interface uses the same scheme as in DDR or DDR2 SDRAM interfaces, where the dedicated circuitry is used during reads to center-align the data and the read clock inside the FPGA and the PLL center-aligns the data and write clock outputs. The data and clock relationship for reads and writes in RLDRAM II is similar to those in DDR and DDR2 SDRAM as shown in [Figures 9-3 and 9-4](#).



For details on RLD RAM II, see [AN 325: Interfacing RLD RAM II with Stratix II & Stratix GX Devices](#).

QDR II SRAM

QDR II SRAM is the second generation of QDR SRAM devices. Both devices can transfer four words per clock cycle, fulfilling the requirements facing next-generation communications system designers. QDR II SRAM devices provide concurrent reads and writes, zero latency, and increased data throughput, allowing simultaneous access to the same address location. QDR II SRAM is available in burst-of-2 and burst-of-4 devices. Burst-of-2 devices support two-word data transfer on all read and write transactions, and burst-of-4 devices support four-word data transfer

Interface Pins

QDR II SRAM uses two separate, unidirectional data ports for read and write operations, enabling QDR data transfer. QDR II SRAM uses shared address lines for reads and writes. QDR II SRAM burst-of-two devices sample the read address on the rising edge of the clock and sample the write address on the falling edge of the clock while QDR II SRAM burst-of-four devices sample both read and write addresses on the clock's rising edge. Connect the memory device's Q ports (read data) to the Stratix II or Stratix II GX DQ pins. You can use any of the Stratix II or Stratix II GX device user I/O pins in I/O banks 3, 4, 7, or 8 for the D ports (write data), commands, and addresses. The control signals are sampled on the rising edge of the clock. You can also use I/O pins in banks 1, 2, 5, or 6 to interface with QDR II SRAM devices. However, these banks do not have dedicated circuitry and can only support QDR II SRAM devices at speeds up to 200 MHz. QDR II SRAM interfaces using these banks are supported using the 1.8-V HSTL Class I I/O support.

QDR II SRAM uses the following clock signals:

- Input clocks K and K#
- Output clocks C and C#
- Echo clocks CQ and CQ#

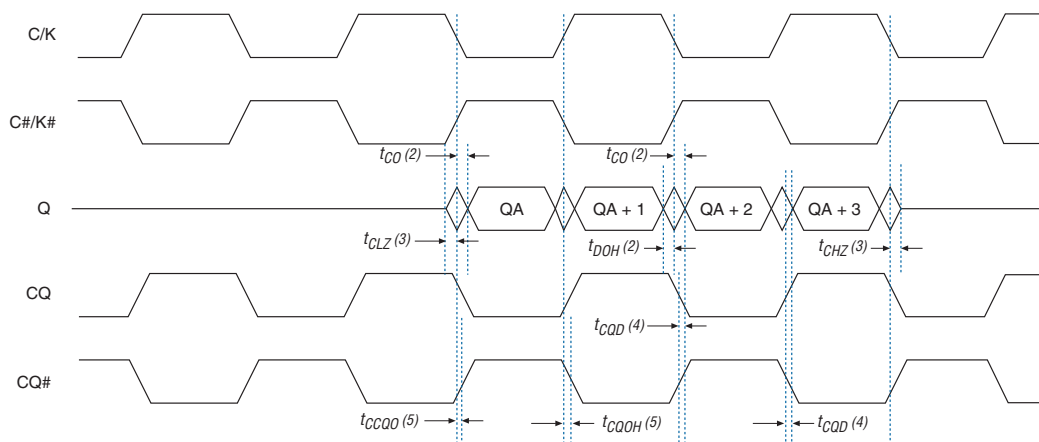
Clocks C#, K#, and CQ# are logical complements of clocks C, K, and CQ, respectively. Clocks C, C#, K, and K# are inputs to the QDR II SRAM while clocks CQ and CQ# are outputs from the QDR II SRAM. Stratix II and Stratix II GX devices use single-clock mode for single-device QDR II SRAM interfacing where the K and K# are used for write operations, and CQ and CQ# are used for read operations. You should use both C or C# and K or K# clocks when interfacing with a bank of multiple QDR II SRAM devices with a single controller.

You can generate C, C#, K, and K# clocks using any of the I/O registers via the DDR registers. Because of strict skew requirements between K and K# signals, use adjacent pins to generate the clock pair.

Connect CQ and CQ# pins to the Stratix II or Stratix II GX DQS and DQSn pins for DLL-based implementations. You must configure DQS and DQSn as bidirectional pins. However, since CQ and CQ# pins are output-only pins from the memory, the Stratix II or Stratix II GX device QDRII SRAM memory interface requires that you ground the DQS and DQSn output enable. To capture data presented by the memory, connect the shifted CQ signal to the input latch and connect the active-high input registers and the shifted CQ# signal is connected to the active-low input register. For PLL-based implementations, connect QK to the input of the read PLL and leave QK# unconnected.

Read and Write Operations

Figure 9-5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. Data is output one-and-a-half clock cycles after a read command is latched into memory. QDRII SRAM devices send data within a t_{CO} time after each rising edge of the read clock C or C# in multi-clock mode, or the input clock K or K# in single clock mode. Data is valid until t_{DOH} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. The CQ and CQ# clocks are edge-aligned with the read data signal. These clocks accompany the read data for data capture in Stratix II and Stratix II GX devices.

Figure 9–5. Data and Clock Relationship During a QDRII SRAM Read *Note (1)***Notes to Figure 9–5:**

- (1) This relationship is at the memory device. The timing parameter nomenclature is based on the Cypress QDRII SRAM data sheet for CY7C1313V18.
- (2) t_{CO} is the data clock-to-out time and t_{DOH} is the data output hold time between burst.
- (3) t_{CLZ} and t_{CHZ} are bus turn-on and turn-off times respectively.
- (4) t_{CQD} is the skew between the rising edge of CQ or CQ# and the data edges.
- (5) t_{CCQO} and t_{CQOH} are skew measurements between the C or C# clocks (or the K or K# clocks in single-clock mode) and the CQ or CQ# clocks.

When reading from the QDRII SRAM, data is sent edge-aligned with the rising edge of the echo clocks CQ and CQ#. Both CQ and CQ# are shifted inside the FPGA using DQS and DQSn logic blocks to capture the data in the DDR IOE registers in DLL-based implementations. In PLL-based implementations, CQ feeds a PLL, which generates the clock to capture the data in the DDR IOE registers.

When writing to QDRII SRAM devices, data is generated by the write clock while the K clock is 90° shifted from the write clock, creating a center-aligned arrangement.

Read and write operations occur during the same clock cycle on independent read and write data paths along with the cycle-shared address bus. Performing concurrent reads and writes does not change the functionality of either transaction. If a read request occurs simultaneously with a write request at the same address, the new data on D is forwarded to Q. Therefore, latency is not required to access valid data.



For more information on QDRII SRAM, go to www.qdrsram.com or see [AN 326: Interfacing QDRII & QDRII+ SRAM with Stratix II, Stratix, & Stratix GX Devices](#).

Stratix II and Stratix II GX DDR Memory Support Overview

This section describes Stratix II and Stratix II GX features that enable high-speed memory interfacing. It first describes Stratix II and Stratix II GX memory pins and then the DQS phase-shift circuitry and the DDR I/O registers. Table 9–2 shows the I/O standard associated with the external memory interfaces.

Table 9–2. External Memory Support in Stratix II and Stratix II GX Devices

Memory Standard	I/O Standard
DDR SDRAM	SSTL-2 Class II
DDR2 SDRAM	SSTL-18 Class II(1)
RLDRAM II (2)	1.8-V HSTL Class I or II (1)
QDRII SRAM (2)	1.8-V HSTL Class I or II (1)

Notes to Table 9–2:

- (1) Stratix II and Stratix II GX devices support 1.8-V HSTL/SSTL-18 Class I and II I/O standards in I/O banks 3, 4, 7, and 8. In I/O banks 1, 2, 5, and 6, Class I is supported for both input and output operations, while Class II is only supported for input operations for these I/O standards.
- (2) For maximum performance, Altera recommends using the 1.8-V HSTL I/O standard. RLDRAM II and QDRII SRAM devices also support the 1.5-V HSTL I/O standard.

Stratix II and Stratix II GX devices support the data strobe or read clock signal (DQS) used in DDR SDRAM, DDR2 SDRAM, RLDRAM II, and QDRII SRAM devices with dedicated circuitry. Stratix II and Stratix II GX devices also support the DQSn signal (the DQS complement signal) for external memory types that require them, for example QDRII SRAM. DQS and DQSn signals are usually associated with a group of data (DQ) pins. However, these are not differential buffers and cannot be used in DDR2 SDRAM or RLDRAM II interfaces.



You can also interface with these external memory devices without the use of dedicated circuitry at a lower performance.



For more information, see the appropriate Stratix II or Stratix II GX memory interfaces application note available at www.altera.com.

Stratix II and Stratix II GX devices contain dedicated circuitry to shift the incoming DQS signals by 0°, 22.5°, 30°, 36°, 45°, 60°, 67.5°, 72°, 90°, 108°, 120°, or 144°, depending on the delay-locked loop (DLL) mode. There are four DLL modes. The DQS phase-shift circuitry uses a frequency reference to dynamically generate control signals for the delay chains in each of the DQS and DQSn pins, allowing it to compensate for process,

voltage, and temperature (PVT) variations. This phase-shift circuitry has been enhanced in Stratix II and Stratix II GX devices to support more phase-shift options with less jitter.

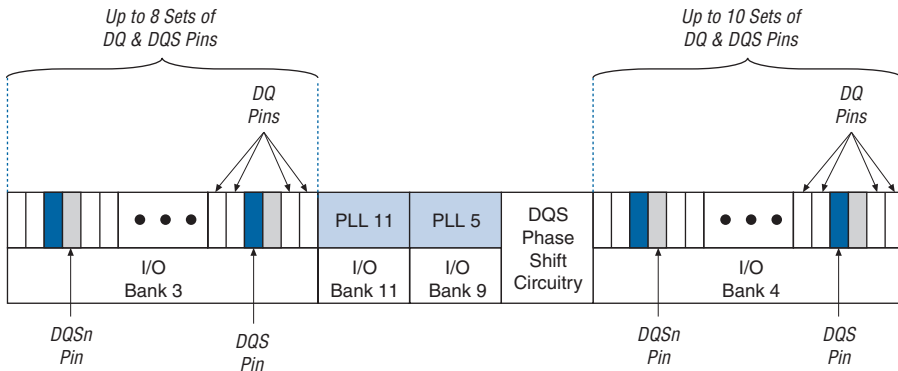
Besides the DQS dedicated phase-shift circuitry, each DQS and DQSn pin has its own DQS logic block that sets the delay for the signal input to the pin. Using the DQS dedicated phase-shift circuitry with the DQS logic block allows for phase-shift fine-tuning. Additionally, every IOE in a Stratix II or Stratix II GX device contains six registers and one latch to achieve DDR operation.

DDR Memory Interface Pins

Stratix II and Stratix II GX devices use data (DQ), data strobe (DQS and DQSn), and clock pins to interface with external memory.

Figure 9–6 shows the DQ, DQS, and DQSn pins in the Stratix II or Stratix II GX I/O banks on the top of the device. A similar arrangement is repeated at the bottom of the device.

Figure 9–6. DQ and DQS Pins Per I/O Bank



Data and Data Strobe Pins

Stratix II and Stratix II GX data pins for the DDR memory interfaces are called DQ pins. Stratix II and Stratix II GX devices can use either bidirectional data strobes or unidirectional read clocks. Depending on the external memory interface, either the memory device’s read data strobes or read clocks feed the Stratix II or Stratix II GX DQS (and DQSn) pins.

Stratix II and Stratix II GX DQS pins connect to the DQS pins in DDR and DDR2 SDRAM interfaces or to the QK pins in RLDRAM II interfaces. The DQSn pins are not used in these interfaces. Connect the Stratix II or Stratix II GX DQS and DQSn pins to the QDRII SRAM CQ and CQ# pins, respectively.

In every Stratix II or Stratix II GX device, the I/O banks at the top (I/O banks 3 and 4) and bottom (I/O banks 7 and 8) of the device support DDR memory up to 300 MHz/600 Mbps (with RLDRAM II). These I/O banks support DQS signals and its complement DQSn signals with DQ bus modes of $\times 4$, $\times 8/\times 9$, $\times 16/\times 18$, or $\times 32/\times 36$.

In $\times 4$ mode, each DQS/DQSn pin drives up to four DQ pins within that group. In $\times 8/\times 9$ mode, each DQS/DQSn pin drives up to nine DQ pins within that group to support one parity bit and the eight data bits. If the parity bit or any data bit is not used, the extra DQ pins can be used as regular user I/O pins. Similarly, with $\times 16/\times 18$ and $\times 32/\times 36$ modes, each DQS/DQSn pin drives up to 18 and 36 DQ pins respectively. There are two parity bits in the $\times 16/\times 18$ mode and four parity bits in the $\times 32/\times 36$ mode. Tables 9–3 through 9–6 show the number of DQS/DQ groups and non-DQS /DQ supported in each Stratix II or Stratix II GX density/package combination, respectively, for DLL-based implementations.

Table 9–3. Stratix II DQS and DQ Bus Mode Support (Part 1 of 2) *Note (1)*

Device	Package	Number of $\times 4$ Groups	Number of $\times 8/\times 9$ Groups	Number of $\times 16/\times 18$ Groups	Number of $\times 32/\times 36$ Groups
EP2S15	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S30	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S60	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4
EP2S90	484-pin Hybrid FineLine BGA	8	4	0	0
	780-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4
EP2S130	780-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4

Table 9–3. Stratix II DQS and DQ Bus Mode Support (Part 2 of 2) *Note (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S180	1,020-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4

Note to Table 9–3:

- (1) Check the pin table for each DQS/DQ group in the different modes.

Table 9–4. Stratix II non-DQS and DQ Bus Mode Support *Note (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S15	484-pin FineLine BGA	13	7	3	1
	672-pin FineLine BGA	24	9	4	2
EP2S30	484-pin FineLine BGA	13	7	3	1
	672-pin FineLine BGA	36	15	7	3
EP2S60	484-pin FineLine BGA	13	7	3	1
	672-pin FineLine BGA	36	15	7	3
	1,020-pin FineLine BGA	51	26	13	6
EP2S90	780-pin FineLine BGA	40	24	12	6
	1,020-pin FineLine BGA	51	25	12	6
	1,508-pin FineLine BGA	51	25	12	6
EP2S130	780-pin FineLine BGA	40	24	12	6
	1,020-pin FineLine BGA	51	25	12	6
	1,508-pin FineLine BGA	51	25	12	6
EP2S180	1,020-pin FineLine BGA	51	25	12	6
	1,508-pin FineLine BGA	51	25	12	6

Note to Table 9–4:

- (1) Check the pin table for each DQS/DQ group in the different modes.

Table 9–5. Stratix II GX DQS and DQ Bus Mode Support *Note (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2SGX30C EP2SGX30D	780-pin FineLine BGA	18	8	4	0
EP2SGX60C EP2SGX60D	780-pin FineLine BGA	18	8	4	0
EP2SGX60E	1,152-pin FineLine BGA	36	18	8	4
EP2SGX90E	1,152-pin FineLine BGA	36	18	8	4
EP2SGX90F	1,508-pin FineLine BGA	36	18	8	4
EP2SGX130G	1,508-pin FineLine BGA	36	18	8	4

Note to Table 9–5:

- (1) Check the pin table for each DQS/DQ group in the different modes.

Table 9–6. Stratix II GX Non-DQS and DQ Bus Mode Support *Note (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2SGX30	780-pin FineLine BGA	18	8	4	2
EP2SGX60	780-pin FineLine BGA	18	8	4	2
	1,152-pin FineLine BGA	25	13	6	3
EP2SGX90	1,152-pin FineLine BGA	25	13	6	3
	1,508-pin FineLine BGA	25	12	6	3
EP2SGX130	1,508-pin FineLine BGA	25	12	6	3

Note to Table 9–6:

- (1) Check the pin table for each DQS/DQ group in the different modes.



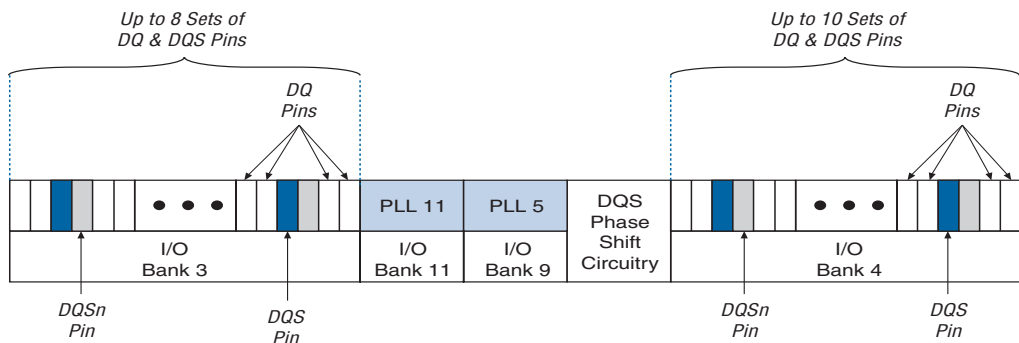
To support the RLDRAM II QVLD pin, some of the unused ×4 DQS pins, whose DQ pins were combined to make the bigger ×8/×9, ×16/×18, or ×32/×36 groups, are listed as DQVLD pins in the Stratix II or Stratix II GX pin table. DQVLD pins are for input-only operations. The signal coming into this pin can be captured by the shifted DQS signal like any of the DQ pins.

The DQS pins are listed in the Stratix II or Stratix II GX pin tables as DQS [17 . . 0] T or DQS [17 . . 0] B. The T denotes pins on the top of the device and the B denotes pins on the bottom of the device. The complement DQSn pins are marked as DQSn [17 . . 0] T or DQSn [17 . . 0] B. The corresponding DQ pins are marked as DQ [17 . . 0] T [3 . . 0], where [17 . . 0] indicates which DQS group the pins belong to. Similarly, the corresponding DQVLD pins are marked as DQVLD [8 . . 0] T, where [8 . . 0] indicates which DQS group the pins belong to. The numbering scheme starts from right to left on the package bottom view. When not used as DQ, DQS, or DQSn pins, these pins are available as regular I/O pins. Figure 9–7 shows the DQS pins in Stratix II or Stratix II GX I/O banks.



The Quartus II software treats DQVLD pins as regular DQ pins. Therefore, you must ensure that the DQVLD pin assigned in your design corresponds to the pin table's recommended DQVLD pins.

Figure 9–7. DQS Pins in Stratix II and Stratix II GX I/O Banks Notes (1), (2), (3)



Notes to Figure 9–7:

- (1) There are up to 18 pairs of DQS and DQSn pins on both the top and bottom of the device. See Table 9–3 for the exact number of DQS and DQSn pin pairs in each device package.
- (2) See Table 9–7 for the available DQS and DQSn pins in each mode and package.
- (3) Each DQS pin has a complement DQSn pin. DQS and DQSn pins are not differential.

The DQ pin numbering is based on $\times 4$ mode. There are up to 8 DQS/DQ groups in $\times 4$ mode in I/O banks 3 and 8 and up to 10 DQS/DQ groups in $\times 4$ mode in I/O banks 4 and 7. In $\times 8/\times 9$ mode, two adjacent $\times 4$ DQS/DQ groups plus one parity pin are combined; one pair of DQS/DQSn pins from the combined groups can drive all the DQ and parity pins. Since there is an even number of DQS/DQ groups in an I/O bank, combining groups is efficient. Similarly, in $\times 16/\times 18$ mode, four adjacent $\times 4$ DQS/DQ groups plus two parity pins are combined and one pair of DQS/DQSn pins from the combined groups can drive all the DQ and parity pins. In

×32/×36 mode, eight adjacent DQS/DQ groups are combined and one pair of DQS/DQSn pins can drive all the DQ and parity pins in the combined groups.

Table 9–7 shows which DQS and DQSn pins are available in each mode and package in the Stratix II or Stratix II GX device family.

Mode	Package		
	484-Pin FineLine BGA 484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA 780-Pin FineLine BGA	1,020-Pin FineLine BGA 1,508-Pin FineLine BGA
×4	7, 9, 11, 13	Odd-numbered pins only	All DQS and DQSn pins
×8/×9	7,11	3, 7, 11, 15	Even-numbered pins only
×16/×18	N/A	5, 13	3, 7, 11, 15
×32/×36	N/A	N/A	5, 13

Note to Table 9–7:

- (1) The numbers correspond to the DQS and DQSn pin numbering in the Stratix II or Stratix II GX pin table. There are two sets of DQS/DQ groups, one corresponding with the top side of the device and one with the bottom side of the device.



On the top and bottom side of the device, the DQ and DQS pins must be configured as bidirectional DDR pins to enable the DQS phase-shift circuitry. The DQSn pins can be configured as input, output, or bidirectional pins. You can use the `altdq` and `altdqs` megafunctions to configure the DQ and DQS/DQSn paths, respectively. However, Altera highly recommends that you use the respective Altera memory controller IP Tool Bench for your external memory interface data paths. The data path is clear-text and free to use. You are responsible for your own timing analysis if you use your own data path. If you only want to use the DQ and/or DQS pins as inputs, you need to set the output enable of the DQ and/or DQS pins to ground.

Stratix II or Stratix II GX side I/O banks (I/O banks 1, 2, 5, and 6) support all the memory interfaces supported in the top and bottom I/O banks. For optimal performance, use the Altera memory controller IP Tool Bench to pick the data and strobe pins for these interfaces. Since these I/O banks do not have any dedicated circuitry for memory interfacing, they can support DDR SDRAM at speeds up to 150 MHz and other DDR memories at speeds up to 200 MHz. You need to use the SSTL-18 Class I I/O standard when interfacing with DDR2 SDRAM devices using pins in I/O bank 1, 2, 5, or 6. These I/O banks do not support the SSTL-18 Class II and

1.8-V HSTL Class II I/O standards on output and bidirectional pins, but you can use SSTL-18 Class I or 1.8-V HSTL Class I I/O standards for memory interfaces.



The Altera memory controller IP Tool Bench generates the optimal pin constraints that allow you to interface these memories at high frequency.

Table 9–8 shows the maximum clock rate supported for the DDR SDRAM interface in the Stratix II or Stratix II GX device side I/O banks.

Stratix II or Stratix II GX Device Speed Grade	DDR SDRAM (MHz)	DDR2 SDRAM (MHz)	QDR II SRAM (MHz)	RLDRAM II (MHz)
-3	150	200	200	200
-4	133	167	167	175
-5	133	167	167	175

Clock Pins

You can use any of the DDR I/O registers to generate clocks to the memory device. For better performance, use the same I/O bank as the data and address/command pins.

Command and Address Pins


You can use any of the user I/O pins in the top or bottom bank of the device for commands and addresses. For better performance, use the same I/O bank as the data pins.

Other Pins (Parity, DM, ECC and QVLD Pins)

You can use any of the DQ pins for the parity pins in Stratix II and Stratix II GX devices. The Stratix II or Stratix II GX device family has support for parity in the $\times 8/\times 9$, $\times 16/\times 18$, and $\times 32/\times 36$ mode. There is one parity bit available per 8 bits of data pins.

The data mask, DM, pins are only required when writing to DDR SDRAM, DDR2 SDRAM, and RLDRAM II devices. A low signal on the DM pins indicates that the write is valid. If the DM signal is high, the memory will mask the DQ signals. You can use any of the I/O pins in the same bank as the DQ pins (or the RLDRAM II SIO's and QDR II SRAM's D pins) for the DM signals. Each group of DQS and DQ signals in DDR

and DDR2 SDRAM devices requires a DM pin. There is one DM pin per RLD RAM II device. The DDR I/O output registers, clocked by the -90° shifted clock, creates the DM signals, similar to DQ output signals.

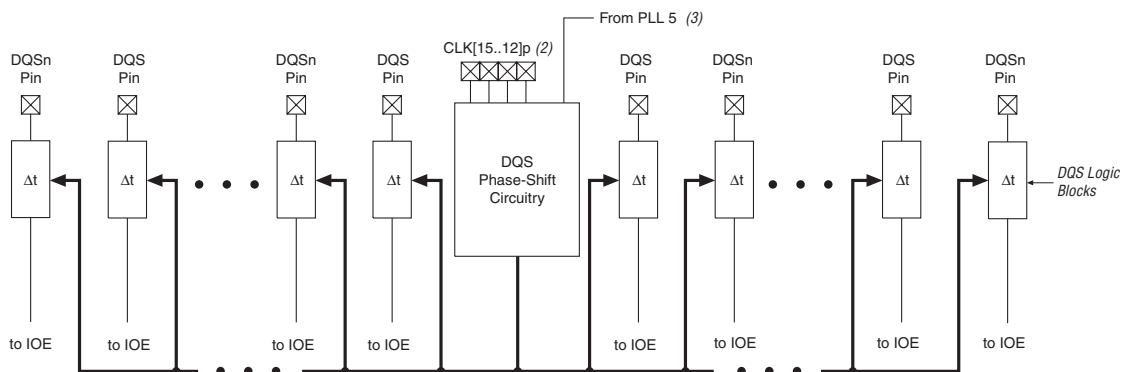
 Perform timing analysis to calculate your write-clock phase shift.

Some DDR SDRAM and DDR2 SDRAM devices support error correction coding (ECC), which is a method of detecting and automatically correcting errors in data transmission. In a 72-bit DDR SDRAM interface, there are eight ECC pins in addition to the 64 data pins. Connect the DDR and DDR2 SDRAM ECC pins to a Stratix II or Stratix II GX device DQS/DQ group. The memory controller needs extra logic to encode and decode the ECC data.

QVLD pins are used in RLD RAM II interfacing to indicate the read data availability. There is one QVLD pin per RLD RAM II device. A high on QVLD indicates that the memory is outputting the data requested. Similar to DQ inputs, this signal is edge-aligned with QK/QK# signals and is sent half a clock cycle before data starts coming out of the memory. You need to connect QVLD pins to the DQVLD pin on the Stratix II or Stratix II GX device. The DQVLD pin can be used as a regular user I/O pin if not used for QVLD. Because the Quartus II software does not differentiate DQVLD pins from DQ pins, you must ensure that your design uses the pin table's recommended DQVLD pin.

DQS Phase-Shift Circuitry

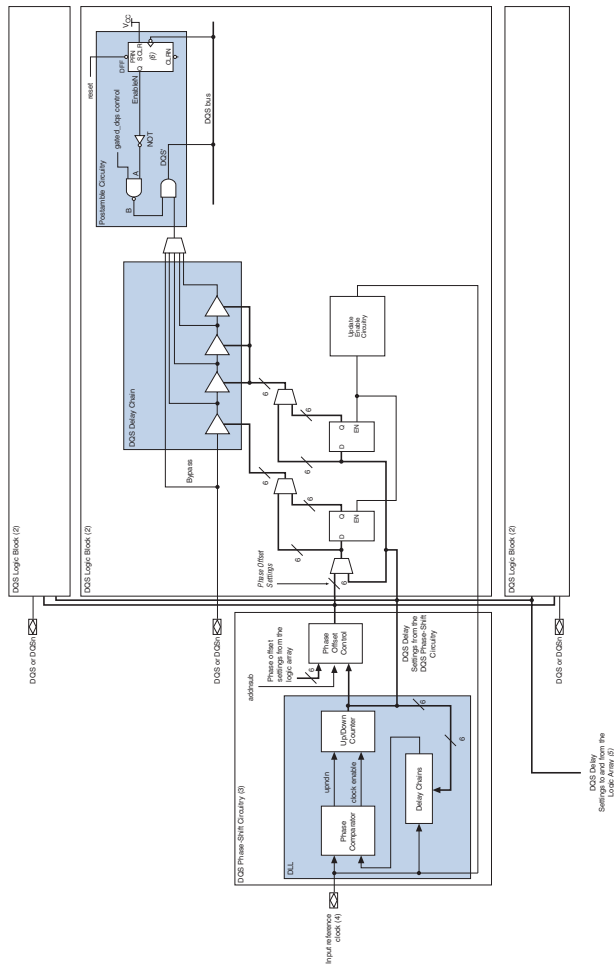
The Stratix II or Stratix II GX phase-shift circuitry and the DQS logic block control the DQS and DQSn pins. Each Stratix II or Stratix II GX device contains two phase-shifting circuits. There is one circuit for I/O banks 3 and 4, and another circuit for I/O banks 7 and 8. The phase-shifting circuit on the top of the device can control all the DQS and DQSn pins in the top I/O banks and the phase-shifting circuit on the bottom of the device can control all the DQS and DQSn pins in the bottom I/O banks. [Figure 9–8](#) shows the DQS and DQSn pin connections to the DQS logic block and the DQS phase-shift circuitry.

Figure 9–8. DQS and DQSn Pins and the DQS Phase-Shift Circuitry *Note (1)***Notes to Figure 9–8:**

- (1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II or Stratix II GX device, up to 8 on the left side of the DQS phase-shift circuitry (I/O banks 3 and 8), and up to 10 on the right side (I/O bank 4 and 7).
- (2) Clock pins CLK [15 . . 12] p feed the phase-shift circuitry on the top of the device and clock pins CLK [7 . . 4] p feed the phase-shift circuitry on the bottom of the device. You can also use a phase-locked loop (PLL) clock output as a reference clock to the phase-shift circuitry. The reference clock can also be used in the logic array.
- (3) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

Figure 9–9 shows the connections between the DQS phase-shift circuitry and the DQS logic block.

Figure 9–9. DQS Phase-Shift Circuitry and DQS Logic Block Connections *Note (1)*



Notes to Figure 9–9:

- (1) All features of the DQS phase-shift circuitry and the DQS logic block are accessible from the `alt_dqs` megafunction in the Quartus II software. You should, however, use Altera’s memory controller IP Tool Bench to generate the data path for your memory interface.
- (2) DQS logic block is available on every DQS and DQSn pin.
- (3) There is one DQS phase-shift circuit on the top and bottom side of the device.
- (4) The input reference clock can come from CLK [15 . . 12] p or PLL 5 for the DQS phase-shift circuitry on the top side of the device or from CLK [7 . . 4] p or PLL 6 for the DQS phase-shift circuitry on the bottom side of the device.
- (5) Each individual DQS and DQSn pair can have individual DQS delay settings to and from the logic array.
- (6) This register is one of the DQS IOE input registers.

The phase-shift circuitry is only used during read transactions where the DQS and DQSn pins are acting as input clocks or strobes. The phase-shift circuitry can shift the incoming DQS signal by 0°, 22.5°, 30°, 36°, 45°, 60°, 67.5°, 72°, 90°, 108°, 120°, or 144°. The shifted DQS signal is then used as clocks at the DQ IOE input registers.

Figure 9–3 shows an example where the DQS signal is shifted by 90°. The DQS signal goes through the 90° shift delay set by the DQS phase-shift circuitry and the DQS logic block and some routing delay from the DQS pin to the DQ IOE registers. The DQ signals only go through routing delay from the DQ pin to the DQ IOE registers and maintains the 90° relationship between the DQS and DQ signals at the DQ IOE registers since the software will automatically set delay chains to match the routing delay between the pins and the IOE registers for the DQ and DQS input paths.

All 18 DQS and DQSn pins on either the top or bottom of the device can have their input signal phase shifted by a different degree amount but all must be referenced at one particular frequency. For example you can have a 90° phase shift on DQS0T and have a 60° phase shift on DQS1T both referenced from a 200-MHz clock. Not all phase-shift combinations are supported, however. The phase shifts on the same side of the device must all be a multiple of 22.5° (up to 90°), a multiple of 30° (up to 120°), or a multiple of 36° (up to 144°).

In order to generate the correct phase shift with the DLL used, you must provide a clock signal of the same frequency as the DQS signal to the DQS phase-shift circuitry. Any of the CLK[15..12] p clock pins can feed the phase circuitry on the top of the device (I/O banks 3 and 4) or any of the CLK[7..4] p clock pins can feed the phase circuitry on the bottom of the device (I/O banks 7 and 8). Stratix II and Stratix II GX devices can also use PLLs 5 or 6 as the reference clock to the DQS phase-shift circuitry on the top or bottom of the device, respectively. PLL 5 is connected to the DQS phase-shift circuitry on the top side of the device and PLL 6 is connected to the DQS phase-shift circuitry on the bottom side of the device. Both the top and bottom phase-shift circuits need unique clock pins or PLL clock outputs for the reference clock.



When you have a PLL dedicated only to generate the DLL input reference clock, you must set the PLL mode to “No Compensation” or the Quartus® II software will change it automatically. Because there are no other PLL outputs used, the PLL doesn’t need to compensate for any clock paths.

DLL

The DQS phase-shift circuitry uses a delay-locked loop (DLL) to dynamically measure the clock period needed by the DQS/DQSn pin (see [Figure 9–10](#)). The DQS phase-shift circuitry then uses the clock period to generate the correct phase shift. The DLL in the Stratix II or Stratix II GX DQS phase-shift circuitry can operate between 100 and 400 MHz. The phase-shift circuitry needs a maximum of 256 clock cycles to calculate the correct input clock period. Data sent during these clock cycles may not be properly captured.



Although the DLL can run up to 400 MHz, other factors may prevent you from interfacing with a 400-MHz external memory device.



You can still use the DQS phase-shift circuitry for any memory interfaces that are less than 100 MHz. The DQS signal will be shifted by 2.5 ns and you can add more shift by using the phase offset module. Even if the DQS signal is not shifted exactly to the middle of the DQ valid window, the IOE should still be able to capture the data in this low frequency application.

There are four different frequency modes for the Stratix II or Stratix II GX DLL. Each frequency mode provides different phase shift, as shown in [Table 9–9](#).

Frequency Mode	Frequency Range (MHz)	Available Phase Shift	Number of Delay Chains
0	100–175	30, 60, 90, 120	12
1	150–230	22.5, 45, 67.5, 90	16
2	200–310	30, 60, 90, 120	12
3	240–400 (C3 speed grade) 240–350 (C4 and C5 speed grades)	36, 72, 108, 144	10

In frequency mode 0, Stratix II devices use a 6-bit setting to implement the phase-shift delay. In frequency modes 1, 2, and 3, Stratix II devices only use a 5-bit setting to implement the phase-shift delay.

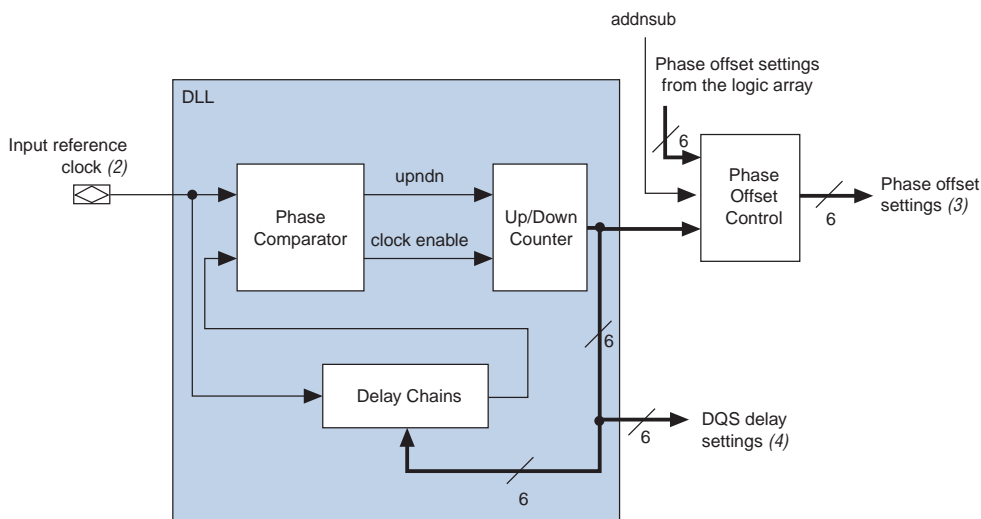
The DLL can be reset from either the logic array or a user I/O pin. This signal is not shown in [Figure 9–10](#). Each time the DLL is reset, you must wait for 256 clock cycles before you can capture the data properly.



The input reference clock for the DQS phase-shift circuitry on the top side of the device can come from CLK[15..12]p or PLL 5. The input reference clock for the DQS phase-shift circuitry on the bottom side of the device can come from CLK[7..4]p or PLL 6.

Table 9–10 lists the maximum delay in the fast timing model for the Stratix II DQS delay buffer. Multiply the number of delay buffers that you are using in the DQS logic block to get the maximum delay achievable in your system. For example, if you implement a 90° phase shift at 200 MHz, you use three delay buffers in mode 2. The maximum achievable delay from the DQS block is then $3 \times .416 \text{ ps} = 1.248 \text{ ns}$.

Frequency Mode	Maximum Delay Per Delay Buffer (Fast Timing Model)	Unit
0	0.833	ns
1, 2, 3	0.416	ns

Figure 9–10. Simplified Diagram of the DQS Phase-Shift Circuitry *Note (1)***Notes to Figure 9–10:**

- (1) All features of the DQS phase-shift circuitry are accessible from the `altdqs` megafunction in the Quartus II software. You should; however, use Altera's memory controller IP Tool Bench to generate the data path for your memory interface.
- (2) The input reference clock for the DQS phase-shift circuitry on the top side of the device can come from `CLK [15 . . 12] p` or PLL 5. The input reference clock for the DQS phase-shift circuitry on the bottom side of the device can come from `CLK [7 . . 4] p` or PLL 6.
- (3) Phase offset settings can only go to the DQS logic blocks.
- (4) DQS delay settings can go to the logic array and/or to the DQS logic block.

The input reference clock goes into the DLL to a chain of up to 16 delay elements. The phase comparator compares the signal coming out of the end of the delay element chain to the input reference clock. The phase comparator then issues the `updn` signal to the up/down counter. This signal increments or decrements a six-bit delay setting (DQS delay settings) that will increase or decrease the delay through the delay element chain to bring the input reference clock and the signals coming out of the delay element chain in phase.

The DQS delay settings contain the control bits to shift the signal on the input DQS pin by the amount set in the `altdqs` megafunction. For the 0° shift, both the DLL and the DQS logic block are bypassed. Since Stratix II and Stratix II GX DQS and DQ pins are designed such that the pin to IOE delays are matched, the skew between the DQ and DQS pin at the DQ IOE registers is negligible when the 0° shift is implemented. You can feed the DQS delay settings to the DQS logic block and the logic array.

Phase Offset Control

The DQS phase-shift circuitry also contains a phase offset control module that can add or subtract a phase offset amount from the DQS delay setting (phase offset settings from the logic array in [Figure 9-10](#)). You should use the phase offset control module for making small shifts to the input signal and use the DQS phase-shift circuitry for larger signal shifts. For example, if you need the input signal to be shifted by 75°, you can set the `alt_dqs` megafunction to generate a 72° phase shift with a phase offset of +3°.

You can either use a static phase offset or a dynamic phase offset to implement the additional phase shift. The available additional phase shift is implemented in 2s-complement between settings -64 to +63 for frequency mode 0, and between settings -32 to +31 for frequency modes 1, 2, and 3. However, the DQS delay settings are at the maximum at setting 64 for frequency mode 0, and at the maximum at setting 32 for frequency modes 1, 2, and 3. Therefore, the actual physical offset setting range will be 64 or 32 subtracted by the DQS delay settings from the DLL.

For example, if the DLL determines that to achieve 30° you will need a DQS delay setting of 28, you can subtract up to 28 phase offset settings and you can add up to 36 phase offset settings to achieve the optimal delay.



Each phase offset setting translates to a certain delay, as specified in the [DC & Switching Characteristics of Stratix III Devices](#) chapter in volume 2 of the *Stratix III Device Handbook*.

When using the static phase offset, you can specify the phase offset amount in the `alt_dqs` megafunction as a positive number for addition or a negative number for subtraction. You can also have a dynamic phase offset that is always added to, subtracted from, or both added to and subtracted from the DLL phase shift. When you always add or subtract, you can dynamically input the phase offset amount into the `dll_offset[5..0]` port. When you want to both add and subtract dynamically, you control the `addnsub` signal in addition to the `dll_offset[5..0]` signals.

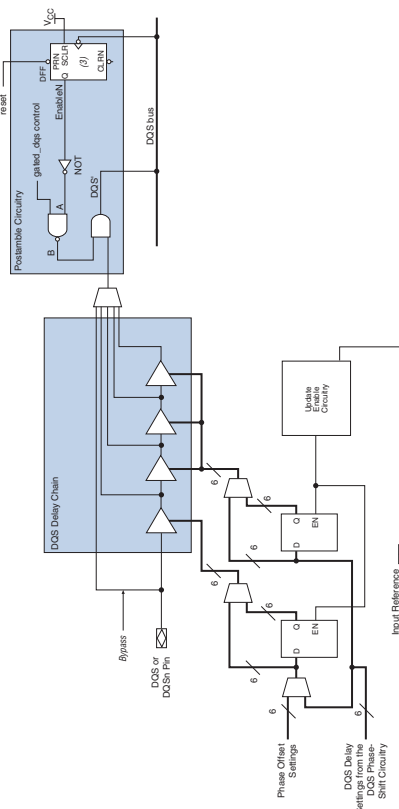
DQS Logic Block

Each DQS and DQSn pin is connected to a separate DQS logic block (see [Figure 9-11](#)). The logic block contains DQS delay chains and postamble circuitry.



The input reference clock for the DQS phase-shift circuitry on the top side of the device can come from CLK[15..12]p or PLL 5. The input reference clock for the DQS phase-shift circuitry on the bottom side of the device can come from CLK[7..4]p or PLL 6.

Figure 9–11. Simplified Diagram of the DQS Logic Block *Note (1)*



Notes to Figure 9–11:

- (1) All features of the DQS logic block are accessible from the altdqs megafunction in the Quartus II software. You should; however, use Altera's memory controller IP Tool Bench to generate the data path for your memory interface.
- (2) The input reference clock for the DQS phase-shift circuitry on the top side of the device can come from CLK[15..12]p or PLL 5. The input reference clock for the DQS phase-shift circuitry on the bottom side of the device can come from CLK[7..4]p or PLL 6.
- (3) This register is one of the DQS IOE input registers.

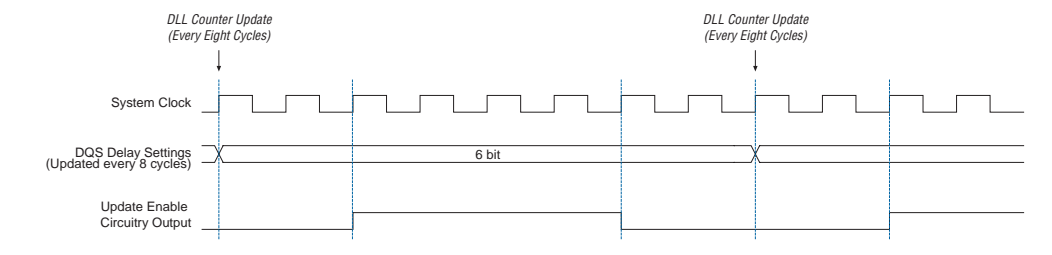
DQS Delay Chains

The DQS delay chains consist of a set of variable delay elements to allow the input DQS and DQSn signals to be shifted by the amount given by the DQS phase-shift circuitry or the logic array. There are four delay elements in the DQS delay chain; the first delay chain closest to the DQS pin can either be shifted by the DQS delay settings or by the sum of the DQS delay setting and the phase-offset setting. The number of delay chains used is transparent to the users because the `alt_dqs` megafunction automatically sets it. The DQS delay settings can come from the DQS phase-shift circuitry on the same side of the device as the target DQS logic block or from the logic array. When you apply a 0° shift in the `alt_dqs` megafunction, the DQS delay chains are bypassed.

The delay elements in the DQS logic block mimic the delay elements in the DLL. When the DLL is not used to control the DQS delay chains, you can input your own 6- or 5-bit settings using the `dqs_delayctrlin[5..0]` signals available in the `alt_dqs` megafunction. These settings control 1, 2, 3, or all 4 delay elements in the DQS delay chains. The amount of delay is equal to the sum of the delay element's intrinsic delay and the product of the number of delay steps and the value of the delay steps.

Both the DQS delay settings and the phase-offset settings pass through a latch before going into the DQS delay chains. The latches are controlled by the update enable circuitry to allow enough time for any changes in the DQS delay setting bits to arrive to all the delay elements. This allows them to be adjusted at the same time. The update enable circuitry enables the latch to allow enough time for the DQS delay settings to travel from the DQS phase-shift circuitry to all the DQS logic blocks before the next change. It uses the input reference clock to generate the update enable output. The `alt_dqs` megafunction uses this circuit by default. See [Figure 9-12](#) for an example waveform of the update enable circuitry output.

The shifted DQS signal then goes to the DQS bus to clock the IOE input registers of the DQ pins. It can also go into the logic array for resynchronization purposes. The shifted DQSn signal can only go to the active-low input register in the DQ IOE and is only used for QDR II SRAM interfaces.

Figure 9–12. DQS Update Enable Waveform

DQS Postamble Circuitry

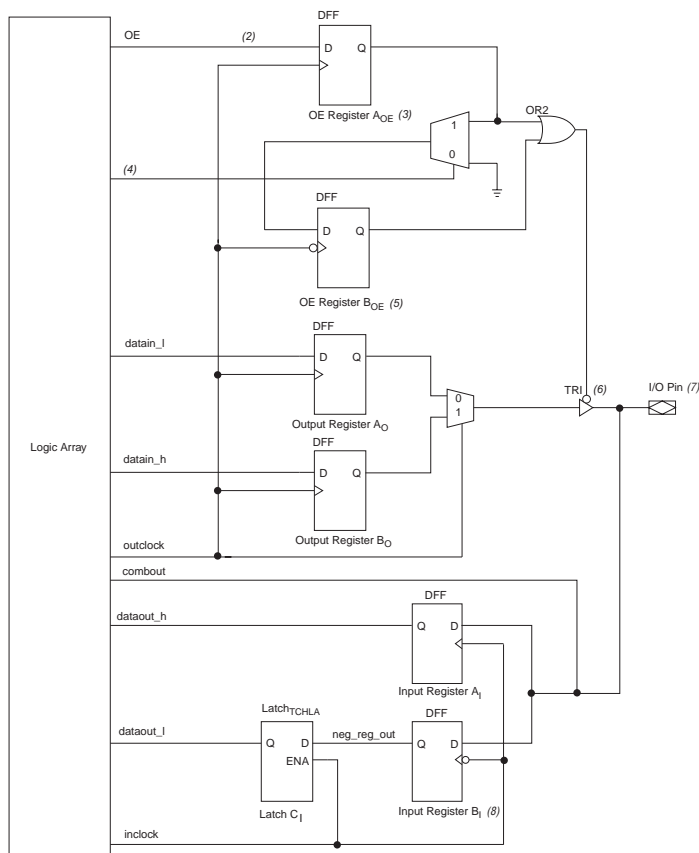
For external memory interfaces that use a bidirectional read strobe like DDR and DDR2 SDRAM, the DQS signal is low before going to or coming from a high-impedance state. See [Figure 9–3](#). The state where DQS is low, just after a high-impedance state, is called the preamble and the state where DQS is low, just before it returns to a high-impedance state, is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR and DDR2 SDRAM. The DQS postamble circuitry ensures data is not lost when there is noise on the DQS line at the end of a read postamble time. It is to be used with one of the DQS IOE input registers such that the DQS postamble control signal can ground the shifted DQS signal used to clock the DQ input registers at the end of a read operation. This ensures that any glitches on the DQS input signals at the end of the read postamble time do not affect the DQ IOE registers.



See [AN 327: Interfacing DDR SDRAM with Stratix II Devices](#) and [AN 328: Interfacing DDR2 SDRAM with Stratix II Devices](#) for more details.

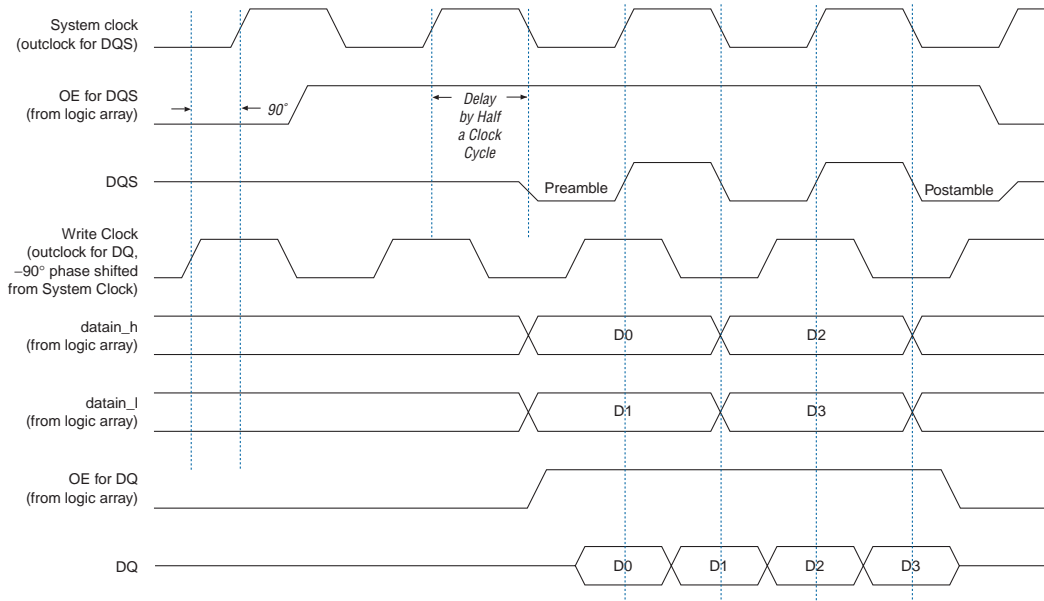
DDR Registers

Each IOE in a Stratix II or Stratix II GX device contains six registers and one latch. Two registers and a latch are used for input, two registers are used for output, and two registers are used for output enable control. The second output enable register provides the write preamble for the DQS strobe in the DDR external memory interfaces. This active low output enable register extends the high-impedance state of the pin by a half clock cycle to provide the external memory's DQS write preamble time specification. [Figure 9–13](#) shows the six registers and the latch in the Stratix II or Stratix II GX IOE and [Figure 9–14](#) shows how the second OE register extends the DQS high-impedance state by half a clock cycle during a write operation.

Figure 9–13. Bidirectional DDR I/O Path in Stratix II and Stratix II GX Devices *Note (1)***Notes to Figure 9–13:**

- (1) All control signals can be inverted at the IOE. The signal names used here match with Quartus II software naming convention.
- (2) The OE signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before input to the A_{OE} register during compilation.
- (3) The A_{OE} register generates the enable signal for general-purpose DDR I/O applications.
- (4) This select line is to choose whether the OE signal should be delayed by half-a-clock cycle.
- (5) The B_{OE} register generates the delayed enable signal for the write strobes or write clocks for memory interfaces.
- (6) The tristate enable is by default active low. You can, however, design it to be active high. The combinational control path for the tristate is not shown in this diagram.
- (7) You can also have combinational output to the I/O pin; this path is not shown in the diagram.
- (8) On the top and bottom I/O banks, the clock to this register can be an inverted register A's clock or a separate clock (inverted or non-inverted). On the side I/O banks, you can only use the inverted register A's clock for this port.

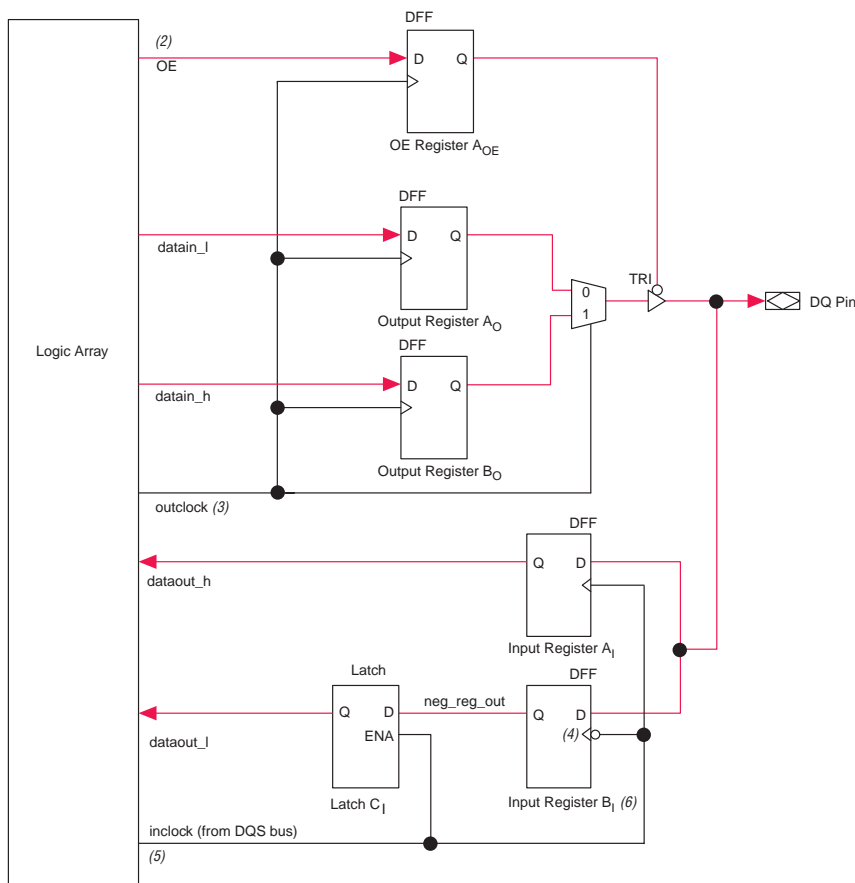
Figure 9–14. Extending the OE Disable by Half-a-Clock Cycle for a Write Transaction *Note (1)*



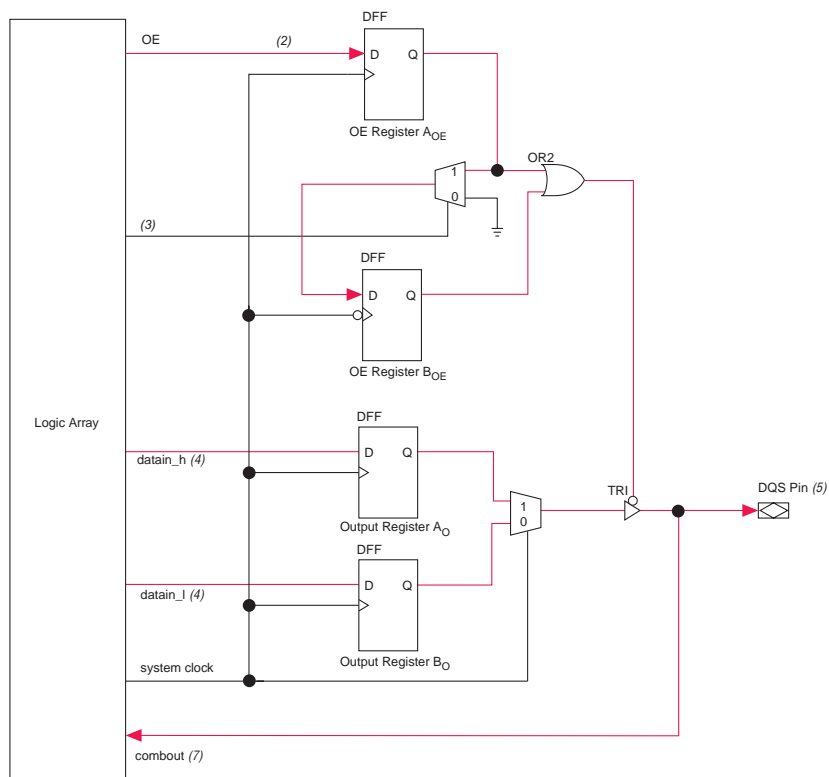
Note to Figure 9–14:

- (1) The waveform reflects the software simulation result. The OE signal is an active low on the device. However, the Quartus II software implements this signal as an active high and automatically adds an inverter before the A_{OE} register D input.

Figures 9–15 and 9–16 summarize the IOE registers used for the DQ and DQS signals.

Figure 9–15. DQ Configuration in Stratix II or Stratix II GX IOE *Note (1)***Notes to Figure 9–15:**

- (1) You can use the `altdq` megafunction to generate the DQ signals. You should, however, use Altera's memory controller IP Tool Bench to generate the data path for your memory interface. The signal names used here match with Quartus II software naming convention.
- (2) The OE signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before the OE register A_{OE} during compilation.
- (3) The `outclock` signal for DDR, DDR2 SDRAM, and QDR II SRAM interfaces has a 90° phase-shift relationship with the system clock. For 300-MHz RLDRAM II interfaces with EP2S60F1020C3, Altera recommends a 75° phase-shift relationship.
- (4) The shifted DQS or DQSn signal can clock this register. Only use the DQSn signal for QDR II SRAM interfaces.
- (5) The shifted DQS signal must be inverted before going to the DQ IOE. The inversion is automatic if you use the `altdq` megafunction to generate the DQ signals. Connect this port to the `combout` port in the `altdqs` megafunction.
- (6) On the top and bottom I/O banks, the clock to this register can be an inverted register A's clock or a separate clock (inverted or non-inverted). On the side I/O banks, you can only use the inverted register A's clock for this port.

Figure 9–16. DQS Configuration in Stratix II or Stratix II GX IOE *Note (1)***Notes to Figure 9–16:**

- (1) You can use the `altdqs` megafunction to generate the DQS signals. You should, however, use Altera's memory controller IP Tool Bench to generate the data path for your memory interface. The signal names used here match with Quartus II software naming convention.
- (2) The OE signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before OE register A_{OE} during compilation. In RLDRAM II and QDRII SRAM, the OE signal is always disabled.
- (3) The select line can be chosen in the `altdqs` megafunction.
- (4) The `datain_l` and `datain_h` pins are usually connected to ground and V_{CC}, respectively.
- (5) DQS postamble circuitry and handling is not shown in this diagram. For more information, see [AN 327: Interfacing DDR SDRAM with Stratix II Devices](#) and [AN 328: Interfacing DDR2 SDRAM with Stratix II Devices](#).
- (6) DQS logic blocks are only available with DQS and DQS_n pins.
- (7) You must invert this signal before it reaches the DQ IOE. This signal is automatically inverted if you use the `altdq` megafunction to generate the DQ signals. Connect this port to the `inclock` port in the `altdq` megafunction.

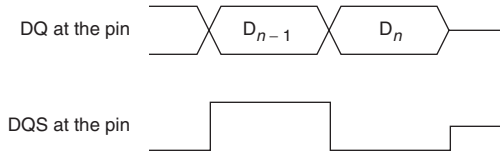
For interfaces to DDR SDRAM, DDR2 SDRAM, and RLDRAM II, the Stratix II or Stratix II GX DDR IOE structure requires you to invert the incoming DQS signal to ensure proper data transfer. This is not required for QDR II SRAM interfaces if the CQ signal is wired to the DQS pin and the CQ# signal is wired to the DQSn pin. The `altdq` megafunction, by default, adds the inverter to the `inclock` port when it generates DQ blocks. The megafunction also includes an option to remove the inverter for QDR II SRAM interfaces. As shown in Figure 9-13, the `inclock` signal's rising edge clocks the A_1 register, `inclock` signal's falling edge clocks the B_1 register, and latch C_1 is opened when `inclock` is 1. In a DDR memory read operation, the last data coincides with DQS being low. If you do not invert the DQS pin, you will not get this last data as the latch does not open until the next rising edge of the DQS signal.

Figure 9-17 shows waveforms of the circuit shown in Figure 9-15.

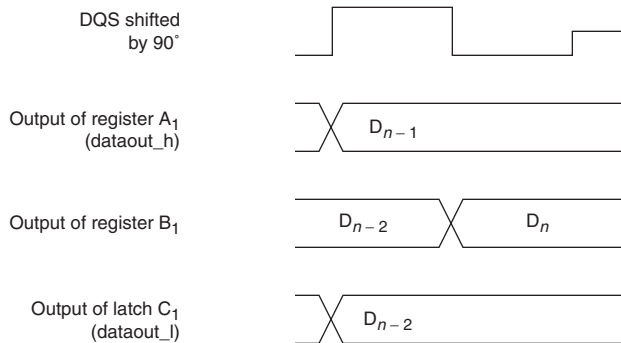
The first set of waveforms in Figure 9-17 shows the edge-aligned relationship between the DQ and DQS signals at the Stratix II or Stratix II GX device pins. The second set of waveforms in Figure 9-17 shows what happens if the shifted DQS signal is not inverted; the last data, D_n , does not get latched into the logic array as DQS goes to tristate after the read postamble time. The third set of waveforms in Figure 9-17 shows a proper read operation with the DQS signal inverted after the 90° shift; the last data, D_n , does get latched. In this case the outputs of register A_1 and latch C_1 , which correspond to `dataout_h` and `dataout_l` ports, are now switched because of the DQS inversion. Register A_1 , register B_1 , and latch C_1 refer to the nomenclature in Figure 9-15.

Figure 9–17. DQ Captures with Non-Inverted and Inverted Shifted DQS

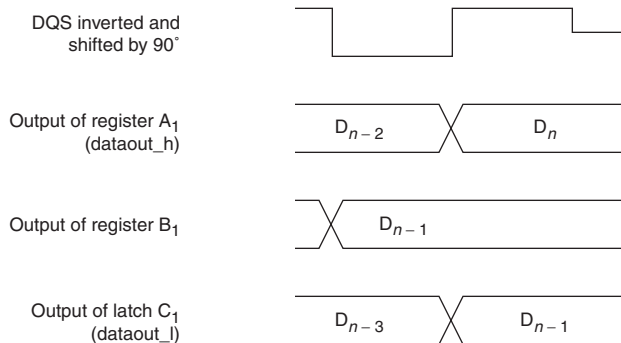
DQ & DQS Signals



Shifted DQS Signal is Not Inverted



Shifted DQS Signal is Inverted



PLL

When using the Stratix II and Stratix II GX top and bottom I/O banks (I/O banks 3, 4, 7, or 8) to interface with a DDR memory, at least one PLL with two outputs is needed to generate the system clock and the write clock. The system clock generates the DQS write signals, commands, and addresses. The write clock is either shifted by -90° or 90° from the system clock and is used to generate the DQ signals during writes.

For DDR and DDR2 SDRAM interfaces above 200 MHz, Altera also recommends a second read PLL to help ease resynchronization.

When using the Stratix II and Stratix II GX side I/O banks 1, 2, 5, or 6 to interface with DDR SDRAM devices, two PLLs may be needed per I/O bank for best performance. Since the side I/O banks do not have dedicated circuitry, one PLL captures data from the DDR SDRAM and another PLL generates the write signals, commands, and addresses to the DDR SDRAM device. Stratix II and Stratix II GX side I/O banks can support DDR SDRAM up to 150 MHz.

Enhancements In Stratix II and Stratix II GX Devices

Stratix II and Stratix II GX external memory interfaces support differs from Stratix external memory interfaces support in the following ways:

- A PLL output can now be used as the input reference clock to the DLL.
- The shifted DQS signal can now go into the logic array.
- The DLL in Stratix II and Stratix II GX devices has more phase-shift options than in Stratix devices. It also has the option to add phase offset settings.
- Stratix II and Stratix II GX devices have DQS logic blocks with each DQS pin that helps with fine tuning the phase shift.
- The DQS delay settings can be routed from the DLL into the logic array. You can also bypass the DLL and send the DQS delay settings from the logic array to the DQS logic block.
- Stratix II and Stratix II GX devices support DQSn pins.
- The DQS/DQ groups now support $\times 4$, $\times 9$, $\times 18$, and $\times 36$ bus modes.
- The DQS pins have been enhanced with the DQS postamble circuitry.

Conclusion

Stratix II and Stratix II GX devices support SDR SDRAM, DDR SDRAM, DDR2 SDRAM, RLDRAM II, and QDRII SRAM external memories. Stratix II and Stratix II GX devices feature high-speed interfaces that transfer data between external memory devices at up to 300 MHz/600 Mbps. DQS phase-shift circuitry and DQS logic blocks within the Stratix II and Stratix II GX devices allow you to fine-tune the phase shifts for the input clocks or strobes to properly align clock edges as needed to capture data.

Referenced Documents

This chapter references the following documents:

- *AN 325: Interfacing RLD RAM II with Stratix II & Stratix GX Devices*
- *AN 326: Interfacing QDR II & QDR II+ SRAM with Stratix II, Stratix, & Stratix GX Devices*
- *AN 327: Interfacing DDR SDRAM with Stratix II Devices*
- *AN 328: Interfacing DDR2 SDRAM with Stratix II Devices*
- *DC & Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook*

Document Revision History

Table 9–11 shows the revision history for this chapter.

Date and Document Version	Changes Made	Summary of Changes
October 2007, v4.5	Added the “Referenced Documents” section.	—
	Minor text edits.	—
No change	For the <i>Stratix II GX Device Handbook</i> only: Formerly chapter 8. The chapter number changed due to the addition of the <i>Stratix II GX Dynamic Reconfiguration</i> chapter. No content change.	—
May 2007, v4.4	Updated the “Phase Offset Control” section.	—
	Updated Figure 9–2.	—
	Updated Table 9–1.	—
	Added Table 9–4 and Table 9–6.	—
	Updated Note (1) to Figure 9–10.	—
February 2007 v4.3	Added the “Document Revision History” section to this chapter.	—
April 2006, v4.2	Chapter updated as part of the <i>Stratix II Device Handbook</i> update.	—
No change	Formerly chapter 7. Chapter number change only due to chapter addition to Section I in February 2006; no content change.	—
December 2005 v4.1	Chapter updated as part of the <i>Stratix II Device Handbook</i> update.	—
October 2005 v4.0	Added chapter to the <i>Stratix II GX Device Handbook</i> .	—

