

IEEE Std. 1149.1 JTAG Boundary- Scan Support

All Stratix® II GX devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1. You can perform JTAG boundary-scan testing either before or after, but not during configuration. Stratix II GX devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc).

Stratix II GX devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the CONFIG_IO instruction. You can use this capability for JTAG testing before configuration when some of the Stratix II GX pins drive or receive from other devices on the board using voltage-referenced standards. Since the Stratix II GX device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming these I/O standards via JTAG allows you to fully test I/O connections to other devices.

A device operating in JTAG mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. The TCK pin has an internal weak pull-down resistor, while the TDI, TMS, and TRST pins have weak internal pull-up resistors. The JTAG input pins are powered by the 3.3-V VCCPD pins. The TDO output pin is powered by the VCCIO power supply in I/O bank 4.

Stratix II GX devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Stratix II GX devices support the JTAG instructions shown in [Table 3-1](#).



Stratix II GX devices must be within the first eight devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II GX devices appear after the eighth device in the JTAG chain, they will fail configuration. This does not affect SignalTap II embedded logic analysis.

Table 3–1. Stratix II GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST (1)	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ (1)	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP (1)	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding the I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a .jam or .jbc via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO (2)	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Notes to Table 3–1:

- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.
- (2) For more information on using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper*.

The Stratix II GX device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Stratix II GX devices.

Table 3–2. Stratix II GX Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2SGX30	1,320
EP2SGX60	1,506
EP2SGX90	2,016
EP2SGX130	2,454

Table 3–3. 32-Bit Stratix II GX Device IDCODE

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit)
EP2SGX30	0000	0010 0000 1110 0001	000 0110 1110	1
EP2SGX60	0000	0010 0000 1110 0010	000 0110 1110	1
EP2SGX90	0000	0010 0000 1110 0011	000 0110 1110	1
EP2SGX130	0000	0010 0000 1110 0100	000 0110 1110	1

SignalTap II Embedded Logic Analyzer

Stratix II GX devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix II GX architecture are configured with CMOS SRAM elements. Altera® FPGAs are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Stratix II GX devices are configured at system power-up with data stored in an Altera configuration device or provided by an external controller (for example, a MAX® II device or microprocessor). You can configure Stratix II GX devices using the fast passive parallel (FPP), active serial

(AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. The Stratix II GX device's optimized interface allows microprocessors to configure it serially or in parallel and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix II GX devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

In addition to the number of configuration methods supported, Stratix II GX devices also offer the design security, decompression, and remote system upgrade features. The design security feature, using configuration bitstream encryption and advanced encryption standard (AES) technology, provides a mechanism to protect designs. The decompression feature allows Stratix II GX FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of Stratix II GX designs. For more information, refer to the ["Configuration Schemes" on page 3–6](#).

Operating Modes

The Stratix II GX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow you to reconfigure Stratix II GX devices in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, re-initializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

The `PORSEL` pin is a dedicated input used to select power-on reset (POR) delay times of 12 ms or 100 ms during power up. When the `PORSEL` pin is connected to ground, the POR time is 100 ms. When the `PORSEL` pin is connected to V_{CC} , the POR time is 12 ms.

The `nIO_PULLUP` pin is a dedicated input that chooses whether the internal pull-up resistors on the user I/O pins and dual-purpose configuration I/O pins (`nCSO`, `ASDO`, `DATA [7..0]`, `nWS`, `nRS`, `RDYnBSY`, `nCS`, `CS`, `RUnLU`, `PGM [2..0]`, `CLKUSR`, `INIT_DONE`, `DEV_OE`, `DEV_CLR`) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-up resistors, while a logic low turns them on.

Stratix II GX devices also offer a new power supply, V_{CCPD} , which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (`TCK`, `TMS`, `TDI`, and `TRST`) and the following configuration pins: `nCONFIG`, `DCLK` (when used as an input), `nIO_PULLUP`, `DATA [7..0]`, `RUnLU`, `nCE`, `nWS`, `nRS`, `CS`, `nCS`, and `CLKUSR`. The `VCCSEL` pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO} voltage, you do not have to take the V_{IL} and V_{IH} levels driven to the configuration inputs into consideration. The configuration input pins, `nCONFIG`, `DCLK` (when used as an input), `nIO_PULLUP`, `RUnLU`, `nCE`, `nWS`, `nRS`, `CS`, `nCS`, and `CLKUSR`, have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The `VCCSEL` input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by V_{CCPD} , while the 1.8-V/1.5-V input buffer is powered by V_{CCIO} .

V_{CCSEL} is sampled during power-up. Therefore, the `VCCSEL` setting cannot change on-the-fly or during a reconfiguration. The `VCCSEL` input buffer is powered by V_{CCINT} and must be hardwired to V_{CCPD} or ground. A logic high `VCCSEL` connection selects the 1.8-V/1.5-V input buffer; a logic low selects the 3.3-V/2.5-V input buffer. `VCCSEL` should be set to comply with the logic levels driven out of the configuration device or the MAX II microprocessor.

If the design must support configuration input voltages of 3.3 V/2.5 V, set `VCCSEL` to a logic low. You can set the V_{CCIO} voltage of the I/O bank that contains the configuration inputs to any supported voltage. If the design must support configuration input voltages of 1.8 V/1.5 V, set `VCCSEL` to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.



For more information on multi-volt support, including information on using `TDO` and `nCEO` in multi-volt systems, refer to the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Configuration Schemes

You can load the configuration data for a Stratix II GX device with one of five configuration schemes (refer to [Table 3–4](#)), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II GX device. A configuration device can automatically configure a Stratix II GX device at system power-up.

Multiple Stratix II GX devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Stratix II GX FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect designs
- Remote system upgrades for remotely updating Stratix II GX designs

[Table 3–4](#) summarizes which configuration features can be used in each configuration scheme.



Refer to the [Configuring Stratix II & Stratix II GX Devices](#) chapter in volume 2 of the *Stratix II GX Device Handbook* for more information about configuration schemes in Stratix II GX devices.

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ (1)	✓ (1)	✓
	Enhanced configuration device		✓ (2)	✓
AS	Serial configuration device	✓	✓	✓ (3)
PS	MAX II device or microprocessor and flash device	✓	✓	✓
	Enhanced configuration device	✓	✓	✓
	Download cable (4)	✓	✓	
PPA	MAX II device or microprocessor and flash device			✓

Table 3–4. Stratix II GX Configuration Features (Part 2 of 2)

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
JTAG	Download cable (4)			
	MAX II device or microprocessor and flash device			

Notes for Table 3–4:

- (1) In these modes, the host system must send a DCLK that is 4× the data rate.
- (2) The enhanced configuration device decompression feature is available, while the Stratix II GX decompression feature is not available.
- (3) Only remote update mode is supported when using the AS configuration scheme. Local update mode is not supported.
- (4) The supported download cables include the Altera USB-Blaster universal serial bus (USB) port download cable, MasterBlaster serial/USB communications cable, ByteBlaster II parallel port download cable, and the ByteBlasterMV parallel port download cable.

Device Security Using Configuration Bitstream Encryption

Stratix II and Stratix II GX FPGAs are the industry’s first FPGAs with the ability to decrypt a configuration bitstream using the AES algorithm. When using the design security feature, a 128-bit security key is stored in the Stratix II GX FPGA. To successfully configure a Stratix II GX FPGA that has the design security feature enabled, the device must be configured with a configuration file that was encrypted using the same 128-bit security key. The security key can be stored in non-volatile memory inside the Stratix II GX device. This nonvolatile memory does not require any external devices, such as a battery back up, for storage.



An encrypted configuration file is the same size as a non-encrypted configuration file. When using a serial configuration scheme such as passive serial (PS) or active serial (AS), configuration time is the same whether or not the design security feature is enabled. If the fast passive parallel (FPP) scheme is used with the design security or decompression feature, a 4× DCLK is required. This results in a slower configuration time when compared to the configuration time of an FPGA that has neither the design security nor the decompression feature enabled. For more information about this feature, contact an Altera sales representative.

Device Configuration Data Decompression

Stratix II GX FPGAs support decompression of configuration data, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other

memory, and transmit this compressed bitstream to Stratix II GX FPGAs. During configuration, the Stratix II GX FPGA decompresses the bitstream in real time and programs its SRAM cells. Stratix II GX FPGAs support decompression in the FPP (when using a MAX II device or microprocessor and flash memory), AS, and PS configuration schemes. Decompression is not supported in the PPA configuration scheme nor in JTAG-based configuration.

Remote System Upgrades

Shortened design cycles, evolving standards, and system deployments in remote locations are difficult challenges faced by system designers. Stratix II GX devices can help effectively deal with these challenges with their inherent reprogrammability and dedicated circuitry to perform remote system updates. Remote system updates help deliver feature enhancements and bug fixes without costly recalls, reducing time to market, and extending product life.

Stratix II GX FPGAs feature dedicated remote system upgrade circuitry to facilitate remote system updates. Soft logic (Nios processor or user logic) implemented in the Stratix II GX device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

Remote system configuration is supported in the following Stratix II GX configuration schemes: FPP, AS, PS, and PPA. Remote system configuration can also be implemented in conjunction with Stratix II GX features such as real-time decompression of configuration data and design security using AES for secure and efficient field upgrades.



Refer to the *Remote System Upgrades with Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information about remote configuration in Stratix II GX devices.

Configuring Stratix II GX FPGAs with JRunner

The JRunner™ software driver configures Altera FPGAs, including Stratix II GX FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (.rbf) format. JRunner also requires a Chain Description File (.cdf)

generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.



For more information on the JRunner software driver, refer to the *AN 414: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site (www.altera.com).

Programming Serial Configuration Devices with SRrunner

A serial configuration device can be programmed in-system by an external microprocessor using SRrunner. SRrunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRrunner reads a Raw Programming Data file (.rpd) and writes to serial configuration devices. The serial configuration device programming time using SRrunner is comparable to the programming time when using the Quartus II software.



For more information about SRrunner, refer to the *AN 418 SRrunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera web site.



For more information on programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.



For more information on the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site.

PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides

considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.



See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on Stratix II GX PLLs.

Temperature Sensing Diode (TSD)

Stratix II GX devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II GX diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus 1 sign bit). The external device's output represents the junction temperature of the Stratix II GX device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II GX device to connect to the external temperature-sensing device, as shown in [Figure 3-1](#). The temperature sensing diode is a passive element and therefore can be used before the Stratix II GX device is powered.

Figure 3-1. External Temperature-Sensing Diode

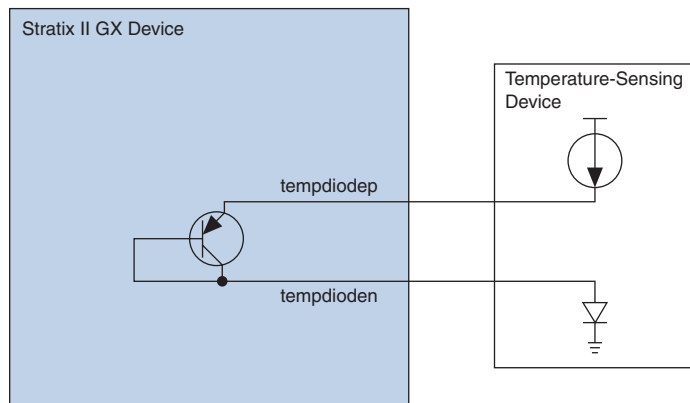
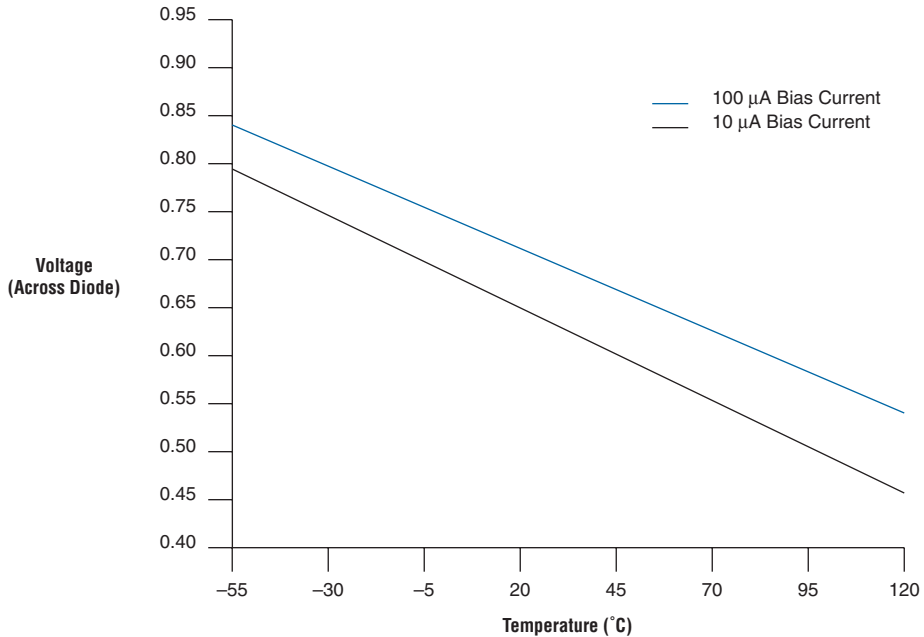


Table 3-5 shows the specifications for bias voltage and current of the Stratix II GX temperature sensing diode.

Parameter	Minimum	Typical	Maximum	Unit
IBIAS high	80	100	120	μA
IBIAS low	8	10	12	μA
VBP - VBN	0.3		0.9	V
VBN		0.7		V
Series resistance			3	Ω

The temperature-sensing diode works for the entire operating range shown in Figure 3-2.

Figure 3-2. Temperature Versus Temperature-Sensing Diode Voltage



The temperature sensing diode is a very sensitive circuit which can be influenced by noise coupled from other traces on the board, and possibly within the device package itself, depending on device usage. The interfacing device registers temperature based on millivolts of difference as seen at the TSD. Switching I/O near the TSD pins can affect the temperature reading. Altera recommends you take temperature readings during periods of no activity in the device (for example, standby mode where no clocks are toggling in the device), such as when the nearby I/Os are at a DC state, and disable clock networks in the device.

Automated Single Event Upset (SEU) Detection

Stratix II GX devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole will require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Stratix II GX devices, eliminating the need for external logic. Stratix II GX devices compute CRC during configuration and checks the computed-CRC against an automatically computed CRC during normal operation. The `CRC_ERROR` pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built into Stratix II GX devices to automatically perform error detection. This circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

Beginning with version 4.1 of the Quartus II software, you can turn on the automated error detection CRC feature in the **Device & Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the Stratix II GX FPGA.



For more information on CRC, refer to [AN 357: Error Detection Using CRC in Altera FPGA Devices](#).

Referenced Documents

This chapter references the following documents:

- *AN 357: Error Detection Using CRC in Altera FPGA Devices*
- *AN 414: An Embedded Solution for PLD JTAG Configuration*
- *AN 418 SRrunner: An Embedded Solution for Serial Configuration Device Programming*
- *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper*
- *Configuring the MicroBlaster Passive Serial Software Driver White Paper*
- *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper*
- *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Remote System Upgrades with Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*
- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Document Revision History

Table 3–6 shows the revision history for this chapter.

Date and Document Version	Changes Made	Summary of Changes
October 2007 v1.4	Minor text edits.	—
August 2007 v1.3	Updated the note in the “ IEEE Std. 1149.1 JTAG Boundary-Scan Support ”	—
	Updated Table 3–3 .	—
	Added the “ Referenced Documents ” section.	—
May 2007 v1.2	Updated the “Temperature Sensing Diode (TSD)” section.	—
February 2007 v1.1	Added the “Document Revision History” section to this chapter.	Added support information for the Stratix II GX device.
October 2005 v1.0	Added chapter to the <i>Stratix II GX Device Handbook</i> .	—

