



Stratix II GX EP2SGX90 Transceiver Signal Integrity Development Board

Reference Manual



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About this Manual

Revision History

The table below displays the revision history for the chapters in this reference manual.

Chapter	Date	Version	Changes Made
All	May 2006	1.0.0	First publication

This reference manual provides comprehensive information about the Altera® Stratix® II GX family of devices and the Stratix II GX EP2SGX90 transceiver signal integrity development board.








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Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: Save As dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: f_{MAX} , lqdesigns directory, d: drive, chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Document titles are shown in italic type with initial capital letters. Example: <i>AN 75: High-Speed Board Design</i> .
<i>Italic type</i>	Internal timing parameters and variables are shown in italic type. Examples: <i>t_{PIA}</i> , <i>n + 1</i> . Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <file name>, <project name>.pdf file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
Courier type	Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input. Active-low signals are denoted by suffix n, e.g., resetn. Anything that must be typed exactly as it appears is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword SUBDESIGN), as well as logic function names (e.g., TRI) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets are used in a list of items when the sequence of the items is not important.
	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

General Description

The Stratix® II GX EP2SGX90 transceiver signal integrity development board provides a hardware platform for developing and prototyping high-speed designs using power-efficient Stratix II GX devices. The transceiver technology embedded in Stratix II GX devices ensures that signal integrity extends to high frequencies while also providing a power-efficient, single-chip solution that supports the following high-speed serial protocols:

- PCI-Express
- CEI-6G
- Gigabit Ethernet
- XAUI
- Serial RapidIO™
- SONET Backplane
- SDI
- SerialLite II

As board designs move into the Gbps space, it is increasingly more difficult to maintain signal integrity. In fact, increasing data rates for both I/O interfaces and memory interfaces can present significant data transmission problems and performance issues.

The Stratix II GX device's embedded transceivers provide enhanced transmit pre-emphasis technology that conditions the signal prior to transmission as well as programmable receiver equalization circuitry. Also, because the Stratix II GX device's embedded transceivers have built-in clock data recovery, you do not have to route the clock and data on the board, which greatly simplifies high-speed board designs.

To further simplify the process, Altera® provides a reference design for use as either a design starting point or an experimental platform. The reference design is designed and tested by Altera engineers and distributed with the Transceiver SI Development Kit, Stratix II GX Edition (ordering code: DK-SI-2SGX90N).

Board Component Blocks

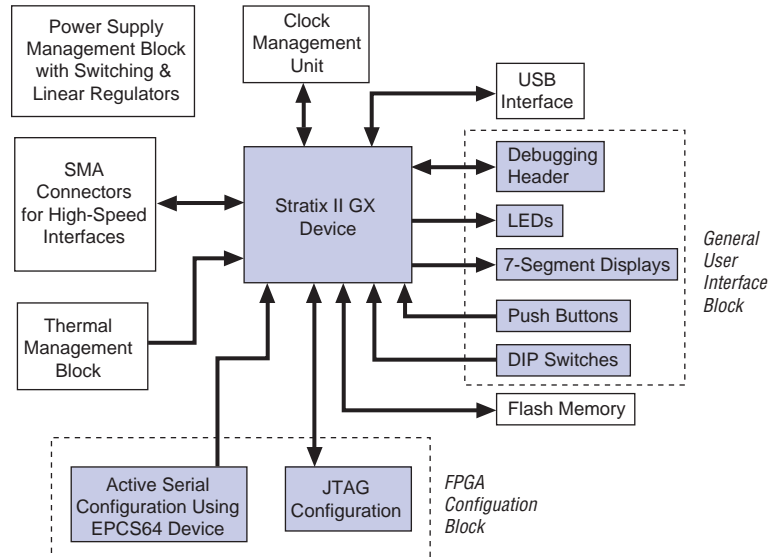
The board provides the following major component blocks:

- Flexible clock management system
 - Four high-speed clock oscillators to support a variety of protocols:
 - 156.25 MHz
 - 25, 100, 125, and 200-MHz from the clock generator
 - 50 MHz
 - SMA connectors for clock input and output
- High-speed I/O & SMA connectors
 - SMA connectors for high-speed interfaces
 - Six channels of transmit differential output and six channels of receive differential input at up to 6.375 Gbps
- Power-supply management
 - 5-V, 3.3-V, and 1.2-V switching regulators
 - 3.3-V and 1.5-V/1.2-V linear regulators
- USB interface
 - Operates like a COM port on a host PC
 - Eliminates the need for:
 - Full USB software and hardware implementation
 - USB software driver
- General user-interface
 - Debugging header
 - LEDs
 - 7-Segment LEDs
 - Push-buttons
 - DIP switches
- Thermal management
- Flash memory
 - 56-pin TSOP package
 - Compliant with common Flash interface (CFI)
 - Reduces development time when used with the Altera SOPC Builder CFI controller module
- FPGA configuration
 - JTAG interface header
 - Active serial configuration scheme using EPCS64 device
 - Configures Stratix II GX device on power-up

Block Diagram

Figure 1–1 shows a functional block diagram of the Stratix II GX EP2SGX90 transceiver signal integrity development board.

Figure 1–1. Stratix II GX EP2SGX90 Transceiver Signal Integrity Development Board Block Diagram



Target Applications

The board is used for the following applications:

- Demonstrating key Stratix II GX device features
- Device qualification, e.g., jitter, pre-emphasis, equalization, and signal integrity testing, as well as receiver sensitivity.
- De-coupling Quartus® II software, transceiver architecture, and Altera MegaWizard® Plug-In Manager demonstrations (supporting devices and interfaces included)
- Demonstrating Stratix II GX device transceiver features
- Characterization testing of high-speed serial interfaces
- Interoperability testing between various devices via on-board SMA connectors
- Power supply evaluation (on-board regulation and banana jack options)

- Clocking evaluation to qualify the Stratix II GX device with user clock sources
- Demonstrate signal integrity features on a standalone basis

Data Rate & Clock Frequency Support Per Protocol

Table 1–1 shows the board’s data rate and clock frequency support per protocol.

Protocol	Data Rate (Gbps)	Clock Frequency (MHz)	Clock Source
6G - CEI	6.25	156.25	On board oscillator
5G scrambled	5	156.25	On board oscillator
4G FC, (1)	4.25	–	SMA clock input
XAUI	3.125	156.25	On board oscillator
PCI-Express/PIPE	2.5	100	On board oscillator
SONET backplane	2.488	–	SMA clock input
2G FC, (1)	2.125	–	SMA clock input
HD - SDI	1.485	–	SMA clock input
GIGE	1.25	125	On board oscillator
1G FC, (1)	1.063	–	SMA clock input

Note to Table 1–1:

- (1) There is no support planned for Fibre channel protocol. This table only shows supported data rate.

Handling the Board

When handling the board, it is important to observe the following precaution:



Static Discharge Precaution—Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Board Overview

This chapter provides operational and connectivity detail for the board's major components and interfaces and is divided into the following major blocks:

- Featured device
- Clocking circuitry
- Interfaces
 - SMA connectors for high-speed I/O
 - USB interface
 - General user interfaces
- Power supply
- Thermal management
- FPGA configuration
- Flash memory



Board schematics, the physical layout database, and manufacturing files for the Stratix® II GX EP2SGX90 transceiver signal integrity development board are included in the Transceiver SI Development Kit, Stratix II GX Edition in the following directory:

`<install path>\SIIGX_SI_Kit-v1.0.0\Docs\BoardDesignFiles`



For information on powering-up the Stratix II GX transceiver signal integrity development board and installing the demo software, refer to the *Transceiver SI Development Kit, Stratix II GX Edition Getting Started User Guide*.

Figure 2-1 shows the top view of the Stratix II GX EP2SGX90 transceiver signal integrity development board.

Figure 2-1. Top View of the Stratix II GX EP2SGX90 Transceiver Signal Integrity Development Board

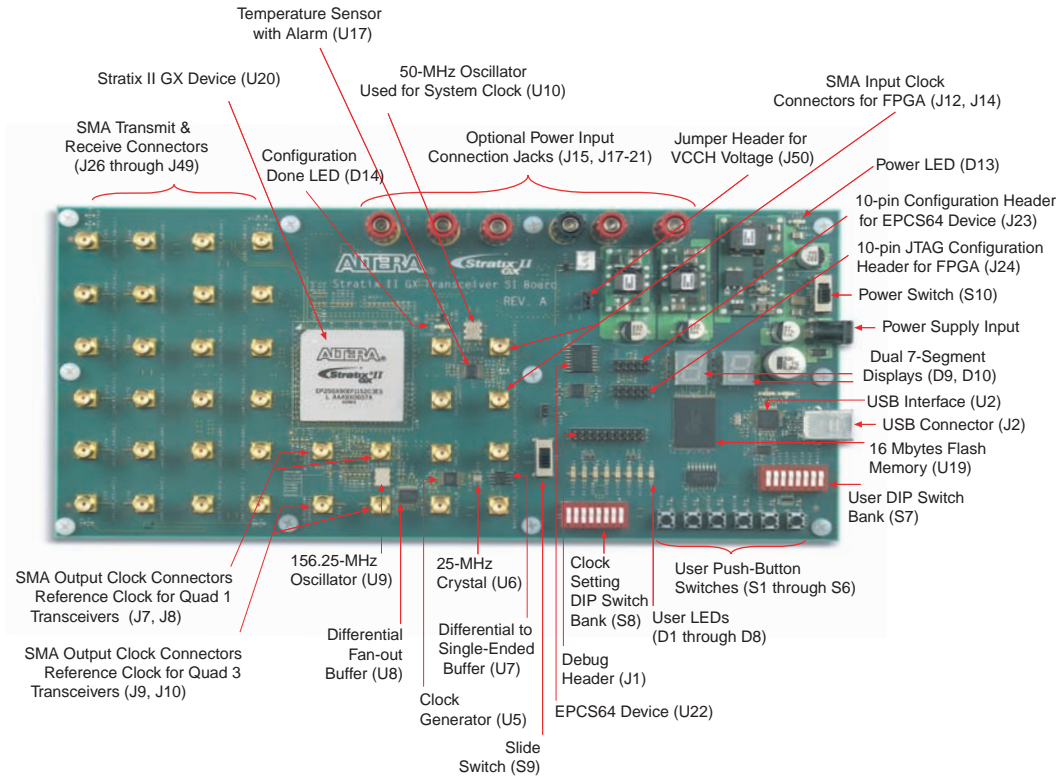


Figure 2–2 shows the diagonal view of the Stratix II GX EP2SGX90 transceiver signal integrity development board.

Figure 2–2. Diagonal View of the Stratix II GX EP2SGX90 Transceiver Signal Integrity Development Board

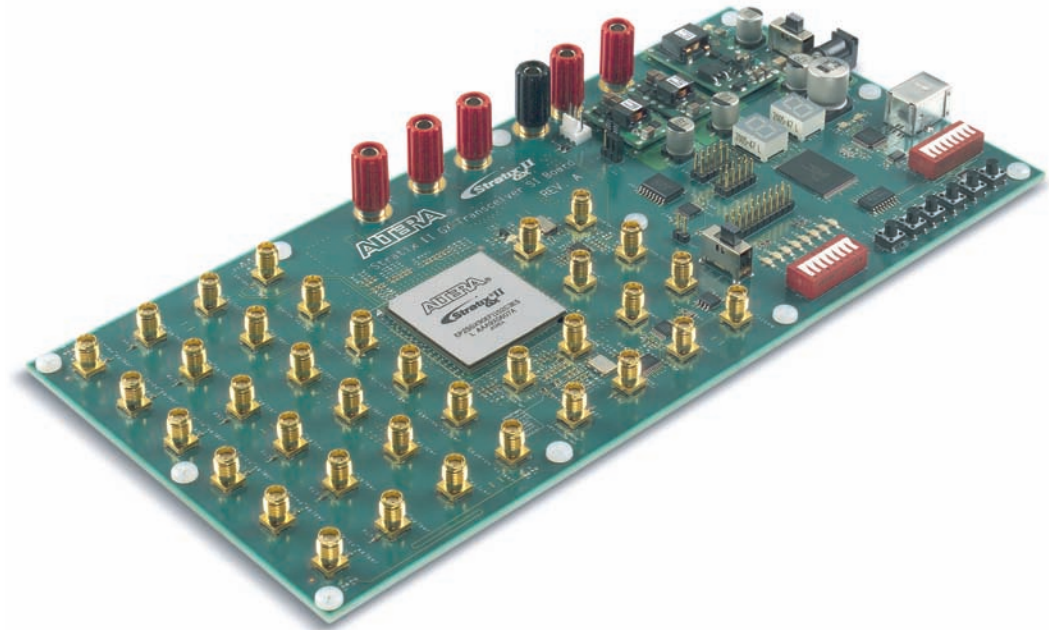


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Stratix II GX Transceiver SI Development Board Components & Interfaces (Part 1 of 3)				
Type	Component/Interface	Board Reference	Description	Page
Featured Device				
FPGA	Stratix II GX device	U20	EP2SGX90EF1152C3NES or EP2SGX90EF35C3NES	2–6
User Interfaces				
I/O	Push-button switches	S1-S6	Six push-button switches for user-defined, logic inputs.	2–21
I/O	DIP switch	S7	Eight toggle DIP switches for user-defined, logic inputs.	2–22
I/O	LEDs	D1-D8	Eight user-defined LEDs	2–18
I/O	Dual seven-segment display	D9, D10	Dual seven-segment display	2–19
I/O	Slide switch	S9	Double-pole, single-throw slide switch for selecting between the 156.25 MHz oscillator and the SMA external clock inputs to supply the clocks to the three quad transceivers.	2–24
I/O	DIP switch	S8	Eight toggle DIP switches for selecting PCIe clock speed, PCIe clock spread-spectrum setting, and the output enable of the clocks to the three quad transceivers.	2–22
Debugging Interfaces				
I/O	Debug header	J1	A twenty-pin connector that is connected to 20 general I/Os on the FPGA.	2–16
Connections & Interfaces				
I/O	USB UART	U2, J2	USB interface to the Stratix II GX device for device configuration and communication with applications running on the device.	2–14
I/O	SMA transmit and receive connectors	J26-J49	SMA connectors with the transmit and receive signals from the quad transceivers	2–12
Configuration & Reset				
Input	Connector	J23	Header for programming the EPCS64 serial configuration device.	2–28
Input	Connector	J24	Header for configuring the Stratix II GX device.	2–28
Input	Jumper header	J25	Jumper header to select which JTAG source the board uses, i.e., the JTAG header configuration or the USB JTAG configuration.	2–28

Table 2–1. Stratix II GX Transceiver SI Development Board Components & Interfaces (Part 2 of 3)

Type	Component/ Interface	Board Reference	Description	Page
Display	Configuration done LED	D14	LED that illuminates upon successful FPGA configuration.	2–28
Memory				
Flash	16 Mbytes of flash memory	U19	16 Mbytes of non-volatile memory.	2–30
Serial flash	64 Mbits of serial flash memory	U22	Altera® EPCS64 low-cost serial configuration device to configure the Stratix II GX device	2–28
Clock Circuitry				
Crystal	Clock	U6	Crystal 25MHz	2–7
Clock Generator	Clock	U5	Spread spectrum clock generator for 25-MHz, 100-MHz, 125-MHz, and 200-MHz clocks.	2–10
Oscillator	Clock	U9	156.25-MHZ oscillator	2–7
Buffer	Clock	U8	1:4 differential fan-out buffer	2–9
Buffer	Clock	U7	Differential to single-ended converter for providing trigger clocks.	2–9
Input	SMA external clock input connectors	J5, J6	SMA connectors for providing an external clock to the three quad transceivers.	2–12
Output	SMA trigger clock connector	J3	SMA connector for the PCIe trigger clock.	2–12
Output	SMA trigger clock connector	J4	SMA connector for the basic trigger clock associated with the three quad transceivers.	2–12
Oscillator	Clock	U10	50-MHz clock oscillator used for the system clock.	2–7
Input	SMA input clock connectors	J7, J8	Reference clock input for quad 1 transceiver	2–12
Input	SMA input clock connectors	J9, J10	Reference clock input for quad 3 transceiver	2–12
Output	SMA output clock connectors	J12, J14	Output clock from Stratix II GX	2–12

Table 2–1. Stratix II GX Transceiver SI Development Board Components & Interfaces (Part 3 of 3)

Type	Component/Interface	Board Reference	Description	Page
Power Supply				
Input	DC power jack	J16	16-V DC unregulated power source.	2–25
Input	Power switch	S10	Switches the board's power on and off.	2–25
Input	Optional power input connection jacks	J17, J15, J18, J19, J20, J21	External power supply can be connected for high current applications.	2–25
Input	Jumper header	J50	Jumper header for selecting between 1.5-V DC and 1.2-V DC supplied to the quad transceivers. Jumper pins 1 and 2 select 1.5-V output, and jumper pins 2 and 3 select 1.2-V output.	2–25
Output	Temperature sensor	U17	Performs thermal management, i.e., turning the cooling fan on and off to regulate the FPGA temperature.	2–25

Featured Device

The Transceiver SI Development Kit, Stratix II GX Edition features the EP2SGX90EF1152 FPGA (U20) in a 1152-pin FineLine BGA® (FBGA) package. [Table 2–2](#) lists some Stratix II GX device features.

Table 2–2. Stratix II GX Features

Architectural Feature	Results
Altera's third-generation FPGA with embedded transceivers	<ul style="list-style-type: none"> • Provides a robust design solution for the most popular high-speed serial interfaces • Provides optimum jitter performance across the entire operating range of 622 Mbps to 6.375 Gbps • Provides best-in class signal integrity performance • Offers enhanced transmit pre-emphasis technology, programmable receiver equalization, and output voltage control
Innovative clock management system	<ul style="list-style-type: none"> • Clock signals are automatically routed to the appropriate destination • Greatly simplifies high-speed board designs • Internal clock frequency of up to 500 MHz
Based on the 1.2-V, 90-nm SRAM process	<ul style="list-style-type: none"> • Provides up to 6.7 Mbits of on-chip TriMatrix™ memory • Provides up to 63 DSP blocks for efficient implementation of high-performance filters and other DSP functions • Supports a wide range of external memory interfaces



For additional information about Altera devices, go to www.altera.com/products/devices.

Clocking Circuitry

You can configure the Stratix II GX device in one of two ways:

- Active serial configuration via the EPCS64 device
- JTAG configuration

The Stratix II GX transceiver signal integrity development board's clocking circuitry is designed to be flexible and easy to use. In fact, with the Stratix II GX device's embedded transceivers, you do not need to route the board's clock and data signals. Instead, the embedded transceivers route the clock and data signals to the appropriate destination.

The Stratix II GX devices have dedicated phase-locked loops (PLLs) for high-speed transceivers, enhanced PLLs for spread-spectrum and general purpose clocking, and fast PLLs for high-speed differential I/O clocking, which support the high-speed interfaces described in this chapter. See [Figure 2-3](#).

The clocking block is comprised of:

- High-speed clock oscillators:
 - 156.25-MHz oscillator
 - 50-MHz oscillator
- 25 MHz crystal
- SMA connectors for clocking input and output signals

[Table 2-3](#) lists the board's clocking parts list.

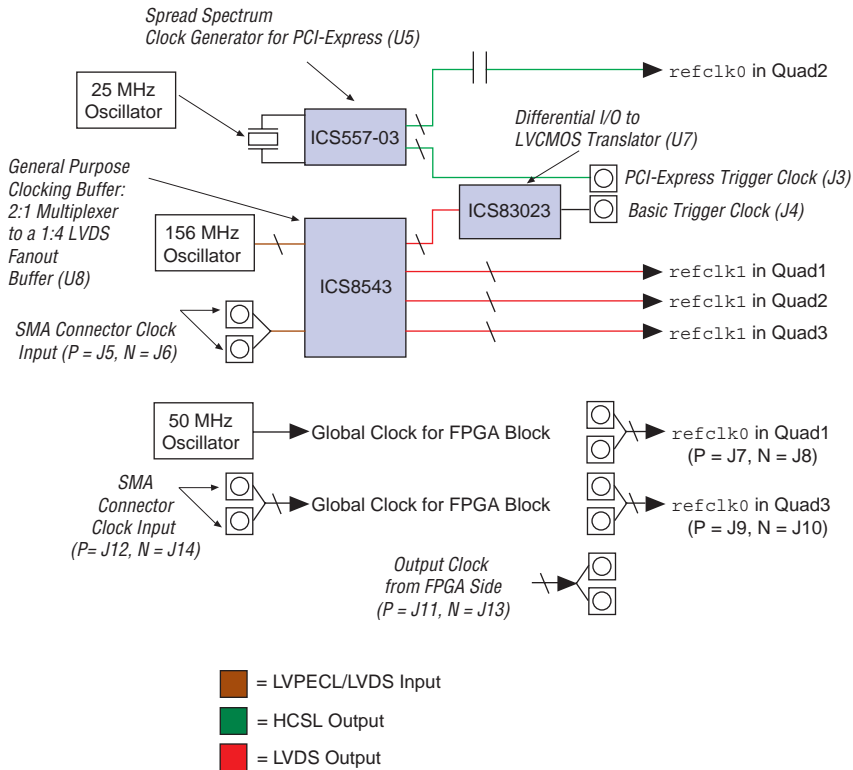
Part Name	Number of Units	Board Reference	Purpose
ICS557-03	1	U5	Spread spectrum PLL
ICS8543	1	U8	Clock buffer to input multiplexer to 4 LVDS outputs
ICS830231	1	U7	Clock buffer differential to single-ended converter
SMA connectors	12	J3 - J14	High-speed interface support
25-MHz crystal	1	U6	Supports the ICS557-03 clock buffer
156.25-MHz oscillator	1	U9	Supports the OIF, CEI-6G, and XAUI protocols
50-MHz oscillator	1	U10	Supports the ICS8543 clock buffer

Table 2-4 lists the clocking circuitry's board references, speeds, interface support, and manufacturing information.

Table 2-4. Board Clocking Circuitry				
Board Reference	Speed	I/O Support	Manufacturing Information	Additional Information
U9	156.25 MHz	XAUI CEI-6G	SMD package, 3.3V, low-voltage positive emitter coupled logic (LVPECL) output	Supports the OIF, CEI-6G, and XAUI protocols.
U5	25, 100, 125, and 200 MHz	PCI-Express GbE	16-pin TSSOP package, 3.3V, and high-speed current steering logic (HCSL) output Part # ICS557-03	Spread-spectrum clock generator for PCIe clocks. The integrated circuit system's (ICS) PLL uses a 25 MHz crystal input and produces two pairs of differential outputs at 25-MHz, 100-MHz, 125-MHz, and 200-MHz clock frequencies. The PLL also provides spread selection of $\pm 25\%$, -0.5% , -0.75% , and no spread.
U7	25 MHz	Differential I/O to single-ended buffer	Small outline integrated circuit (SOIC) 8-pin package, 3.3V, and LVDS/LVPECL/HCSL input and LVCOMS output Part # ICS83023	Differential I/O to LVCMOS translator.
U8	50 MHz	General purpose clocking	20-pin TSSOP package, 3.3V, LVPECL/LVDS input and LVDS output Part # ICS8543	A 2:1 multiplexer to a 4:1 low-voltage differential signaling (LVDS) fanout buffer.

Figure 2–3 shows the clock signals passing through logic translators and automatically routing to the appropriate destination.

Figure 2–3. Clocking Circuitry Automatic Routing Paths



Clock Buffer Functional Descriptions

This section provides functional descriptions for the board's three clock buffers:

- ICS557-03 (U5)
- ICS8543 (U8)
- ICS83023 (U7)

ICS557-03 (U5): Spread Spectrum Clock Generator for PCI-Express

The ICS557-03 is a spread spectrum clock generator supporting PCIe and Ethernet protocol requirements. The device is used to substantially reduce electromagnetic interference (EMI) in PC or embedded systems. The device provides two differential spread spectrum outputs, and is pin-configured for clock and spread selection. Using phase-locked loop (PLL) techniques, the device takes a 25 MHz crystal input and produces two pairs of differential outputs (HCSL) at 25 MHz, 100 MHz, 125 MHz and 200 MHz clock frequencies. The device also provides spread selection of $\pm 0.25\%$, -0.5% , -0.75% , and no spread.

Table 2-5 lists output clock DIP switch settings.

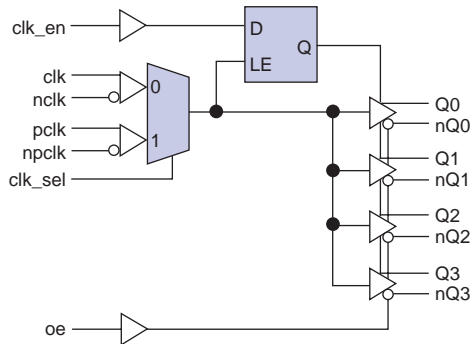
Switch	25 MHz	100 MHz	125 MHz	200 MHz
SW1	Closed	Open	Closed	Open
SW2	Closed	Closed	Open	Open

Table 2-6 lists spread spectrum output selection DIP switch settings.

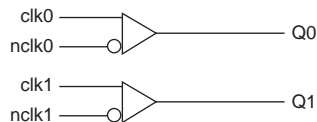
Switch	Center ± 0.25	Down -0.5	Down -0.75	No Spread
SW3	Closed	Open	Closed	Open
SW4	Closed	Closed	Open	Open

ICS8543 (U8): General Purpose 1:4 Differential Fanout Buffer

The ICS8543 is a general purpose clock buffer with a 2:1 multiplexer input and a 1:4 differential fanout. The `clk_sel` signal determines which clock input (i.e., `clk` or `pclk`) is used; the chosen signal is then converted to four output clocks. See [Figure 2-4](#).

Figure 2-4. ICS8543 Clock Buffer Block Diagram*ICS83023 (U7): Differential I/O to Single Converter for Trigger Clock*

The ICS83023 is a differential I/O to a single-ended clock buffer, which is used for both the PCI-Express and Basic trigger clocks. See [Figure 2-5](#).

Figure 2-5. ICS83023 Clock Buffer Block Diagram

Interfaces

This section describes the Stratix II GX EP2SGX90 transceiver signal integrity development board's interface architecture. There are three main interface blocks:

- SMA connectors for high-speed I/O
- USB interface
- General user interfaces

SMA Connectors for High-Speed I/O

The Stratix II GX EP2SGX90 transceiver signal integrity development board has SMA connectors supporting the most commonly-used, high-speed interface protocols. The SMA connectors are helpful for equipment testing. The board has six channels of transmit (TX) differential output as well as six channels of receive (RX) differential input running at up to 6.375 Gbps. See [Figure 2–6](#).

[Table 2–7](#) lists the SMA-to-FPGA pinout table.

SMA Board Reference	Schematic Signal Name	Stratix II GX (U20) Pin Number
J7	REFCLKOP_QUAD1	G1
J8	REFCLKON_QUAD1	G2
J9	REFCLKOP_QUAD3	AK4
J10	REFCLKON_QUAD3	AK5
J11	CLOCKOUT_P	AP17
J12	GLK_P	AP18
J13	CLOCKOUT_N	AN17
J14	GCLK_N	AP19

Figure 2–6. SMA Connector Block Diagram

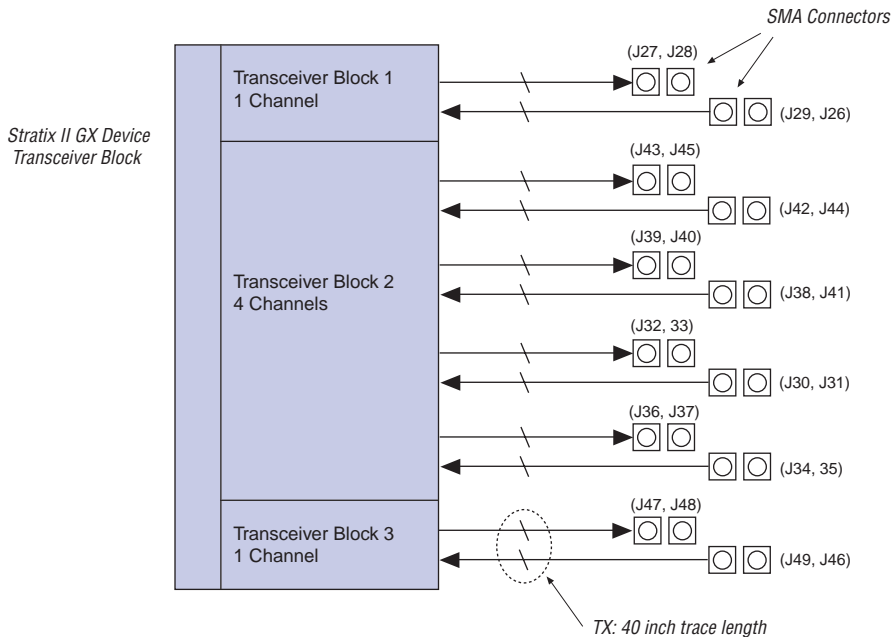


Table 2–8 lists transceiver block’s transmit and receive signals, corresponding SMA reference designators and FPGA pins.

Table 2–8. Transceiver Block Corresponding Signals, SMA Designator, and FPGA Pin (Part 1 of 2)

Block	Signal	SMA Reference Designator	Stratix II GX Pin
Transceiver Block 1, 1 Channel	TX_P0	J27	A4
	TX_N0	J28	A5
	RX_P0	J29	C1
	RX_N0	J26	C2

Table 2–8. Transceiver Block Corresponding Signals, SMA Designator, and FPGA Pin (Part 2 of 2)

Block	Signal	SMA Reference Designator	Stratix II GX Pin
Transceiver Block 2, 4 Channels	TX_P4	J43	AB4
	TX_N4	J45	AB5
	RX_P4	J42	AB1
	RX_N4	J44	AB2
	TX_P3	J39	Y4
	TX_N3	J40	Y5
	RX_P3	J38	Y1
	RX_N3	J41	Y2
	TX_P2	J32	N4
	TX_N2	J33	N5
	RX_P2	J30	N1
	RX_N2	J31	N2
	TX_P1	J36	R4
	TX_N1	J37	R5
	RX_P1	J34	R1
RX_N1	J35	R2	
Transceiver Block 3, 1 Channel	TX_P5	J47	AF4
	TX_N5	J48	AF5
	RX_P5	J49	AF1
	RX_N5	J46	AF2

USB Interface

The USB interface to the board provides a communication port to a host PC. A USB physical connection is used to enable laptops without RS232 ports to communicate with the demo board.

To simplify the USB interface, the board contains a FTDI FT2232L USB universal asynchronous receiver/transmitter (UART) circuit. The UART eliminates the need for full USB software and hardware implementation. In addition, the USB UART design allows the software to be designed as if writing directly to the host PC's COM port, which eliminates the need for designing a USB software driver (see [Figure 2–7](#)).

Also, the 1 M Baud rate should be sufficient for the intended communication applications. The FTDI circuit also has a downloadable non-license USB direct driver and SLL software interface that configures the USB connection into the host PC's COM port.

Figure 2–7. USB Interface to Stratix II GX Transceiver Signal Integrity Development Board

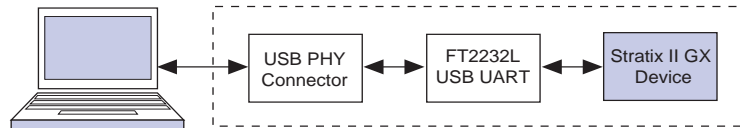


Table 2–9 lists the USB interface to FPGA pinout.

Table 2–9. USB Interface to FPGA Pinout Table

USB Interface (U2) Pin Number	Schematic Signal Name	Stratix II GX (U20) Pin Number
40	UART_DATA0	F30
39	UART_DATA1	G31
38	UART_DATA2	D33
37	UART_DATA3	D32
36	UART_DATA4	H29
35	UART_DATA5	G30
33	UART_DATA6	E32
32	UART_DATA7	E31
30	UART_DATA8	J28
29	UART_DATA9	K27
28	UART_DATA10	E34
27	UART_DATA11	D34

General User Interfaces

To allow you to fully leverage the I/O capabilities of the Stratix II GX device for debugging, control, and monitoring purposes, the following general user interfaces are available on the board:

- Debug Header
- LEDs
- 7-segment display
- LCD interface
- Push buttons
- DIP switches

Debug Header (J1)

Board reference J1 is a simple 20-pin debug header connected to the Stratix II GX device's general user I/O. The form factor is a dual row header such as a FCI 20-pin header (Samtec TSW-110-07-G-D). [Table 2-10](#) lists the schematic signal name and the corresponding Stratix II GX device pin number.

Table 2-10. Debug Header Pin-Out (Part 1 of 2)		
Header Number	Schematic Signal Name	Stratix II GX (U20) Pin Number
1	D_HED0	AB30
2	D_HED1	AA23
3	D_HED2	AB23
4	D_HED3	AB33
5	D_HED4	AB32
6	D_HED5	AA26
7	D_HED6	AA25
8	D_HED7	AA34
9	D_HED8	AB34
10	D_HED9	AB29
11	D_HED10	AB28
12	D_HED11	AC32
13	D_HED12	AC31
14	D_HED13	AB24
15	D_HED14	AC24
16	D_HED15	AC34
17	D_HED16	AC33

Table 2–10. Debug Header Pin-Out (Part 2 of 2)

Header Number	Schematic Signal Name	Stratix II GX (U20) Pin Number
18	D_HED17	AB26
19	D_HED18	AB25
20	D_HED19	AD32

Figure 2–8 shows the debug header’s schematic.

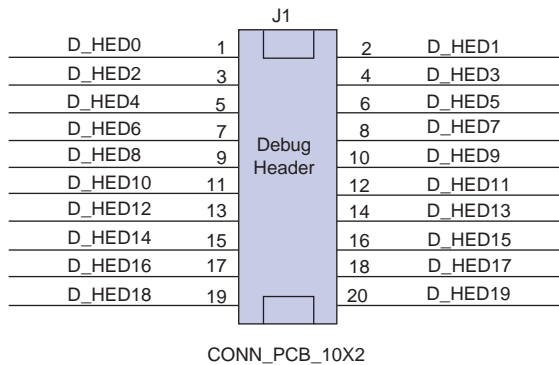
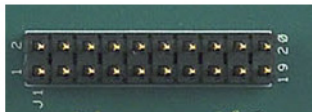
Figure 2–8. Debug Header (J1) Schematic

Figure 2–9 shows the debug header’s board labels.

Figure 2–9. Debug Header (J1) Board Labels

LEDs (D1 Through D8)

The board provides eight user-defined LEDs. D1 through D8 are connected to general purpose I/O pins on the Stratix II GX EP2SGX90 device. When the EP2SGX90 device drives logic 0, the corresponding LED illuminates. [Table 2–11](#) lists the schematic signal name and the corresponding Stratix II GX device’s pin number.

Table 2–11. User-Defined LED Pin-Out		
Board Reference	Schematic Signal Name	Stratix II GX (U20) Pin Number
D1	USER_LED0	AE33
D2	USER_LED1	AE32
D3	USER_LED2	AD26
D4	USER_LED3	AD25
D5	USER_LED4	AD34
D6	USER_LED5	AE34
D7	USER_LED6	AC29
D8	USER_LED7	AC28

[Figure 2–10](#) shows a board image of the user-defined LEDs.

Figure 2–10. User-Defined LEDs

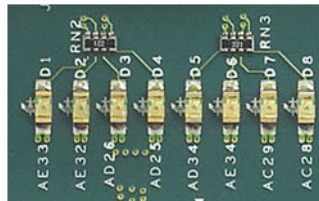
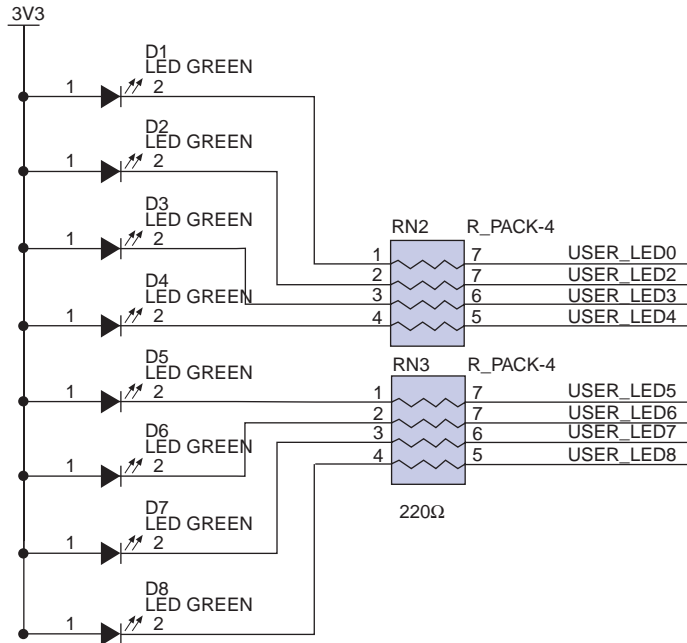


Figure 2–11 shows the LED schematic.

Figure 2–11. LED Schematic



7-Segment Displays (D9, D10)

Board references D9 and D10 are dual user-defined, seven-segment displays. The primary function of the 7-segment displays is to display the board's hardware version, which simplifies board revision control.

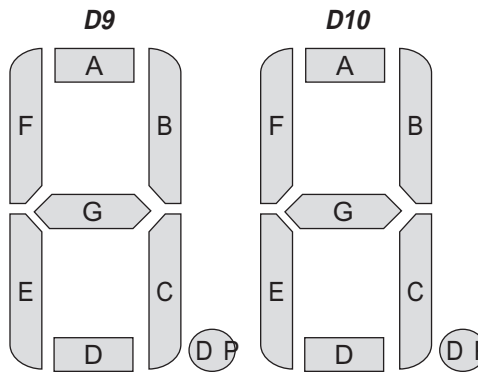
To save board space, the 7-segment displays are a small form factor. Each segment is individually controlled by a general purpose I/O pin. When the EP2SGX90 FPGA pin drives logic 0, the corresponding segment illuminates. See [Figure 2–12](#).

Table 2–12 lists the 7-segment display pinouts.

Board Reference D9			Board Reference D10		
Segment Display Name	Schematic Signal Name	Stratix II GX Pin Name	Segment Display Name	Schematic Signal Name	Stratix II GX Pin Name
A	DIG_1_A	W31	A	DIG_2_A	Y32
B	DIG_1_B	W30	B	DIG_2_B	Y31
C	DIG_1_C	V23	C	DIG_2_C	W28
D	DIG_1_D	W23	D	DIG_2_D	Y29
E	DIG_1_E	W33	E	DIG_2_E	Y34
F	DIG_1_F	W32	F	DIG_2_F	Y33
G	DIG_1_G	Y24	G	DIG_2_G	Y28
DP	DIG_1_DP	Y23	DP	DIG_2_DP	Y27

Figure 2–12 shows the board image and name of each segment.

Figure 2–12. Segment Names for the Dual 7-Segment Displays



Push-Button Switches (S1 Through S6)

Board references S1 through S6 are push-button switches allowing general user I/O interfaces to the Stratix II GX device.

S1-S6 are user-defined, momentary-contact push-button switches used to provide stimulus to a user design on the board. Each push-button is connected through debounce circuitry to a Stratix II GX general-purpose I/O pin as listed in [Table 2-13](#). When the switch is pressed and held down, the device pin is set to logic 0, when the switch is released, the device pin is set to logic 1.

The push button device is a small form factor switch similar to the Panasonic Tactile Switches (EVQPAC07K). [Table 2-13](#) provides operational descriptions and schematic signal names.

Table 2-13. Push-Button Switches (S1 Through S6)

Push-Button Name	Board Reference Designator	Schematic Signal Name	Stratix II GX Device (U20) Pin Number
PB0	S1	PB0_IN	AD28
PB1	S2	PB1_IN	AF34
PB2	S3	PB2_IN	AF33
PB3	S4	PB3_IN	AF30
PB4	S5	PB4_IN	AF29

Note to [Table 2-13](#):

- (1) The PB5 is a special purpose button, called DEV_CLRn, connected to the AH20 pin of the FPGA. The PB5 clears the FPGA data.

Figure 2–13 shows the push-button switch circuitry.

Figure 2–13. Push-Button Switch Circuitry

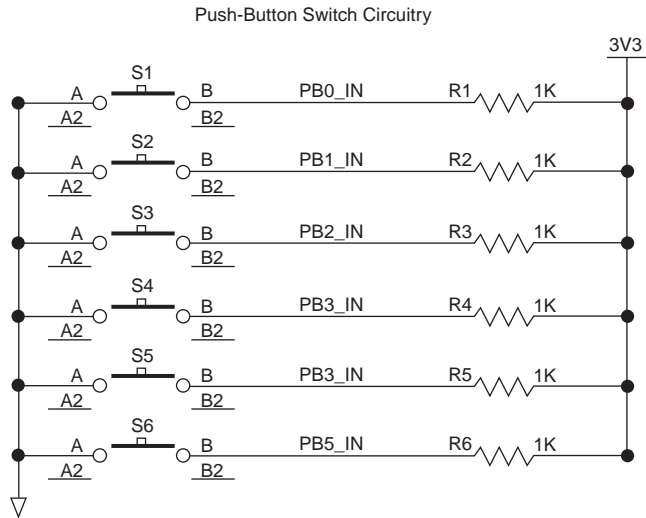
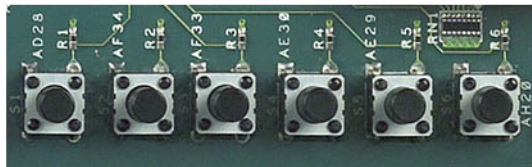


Figure 2–14 shows the push-button board image.

Figure 2–14. Push-Button Board Image



DIP Switches (S7 and S8)

Board references S7 and S8 are banks of six DIP switches. The DIP switches in S7 are user-defined, and DIP switches in S8 control the PCIe clock speed, PCIe clock spread spectrum setting, and the output enable of the clocks to the three quad transceivers. In the open position, the selected signal is driven to logic 1. In the closed position, the selected signal is driven to logic 0.

Table 2–14 lists the S7 output clock DIP switch settings.

S7 Switch	Stratix II GX Pin
S7_1	AH33
S7_2	AH32
S7_3	AF28
S7_4	AF27
S7_5	AJ34
S7_6	AJ33
S7_7	AG29
S7_8	AG28

Figure 2–15 shows the DIP switch board image.

Figure 2–15. DIP Switch Board Image

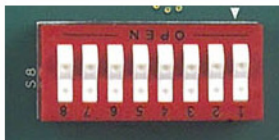


Table 2–15 lists the S8 output clock DIP switch settings.


Switch	25 MHz	100 MHz	125 MHz	200 MHz
SW1	Closed	Open	Closed	Open
SW2	Closed	Closed	Open	Open

Table 2–16 lists the spread spectrum output selection DIP switch settings.

Switch	Center \pm -0.25	Down -0.5	Down -0.75	No Spread
SW3	Closed	Open	Closed	Open
SW4	Closed	Closed	Open	Open

Table 2–17 lists PCIe clock and quad transceiver clock DIP switch settings.

PCIe Clock DIP Switch Setting			Quad Transceiver Clock DIP Switch Setting		
Switch	Enable Clock	Disable Clock	Switch	Enable Clock	Disable Clock
SW5	Open	Closed	SW6	Open	Closed

 Switches 7 and 8 are not connected.

Clock Selection Switches (S9 and S10)

Switch S9 is used to control whether the clock input is driven from an external or an on-board source. Switch S10 is used to apply power to the board. The positions for these switches are labelled on the silk-screen.

Table 2–18 lists clock selection switch settings for board reference S9.

Switch Setting	Result
Switch in OSC setting	Selects the 156.25-MHz oscillator
Switch in SMA position	Selects external clock input

Power Supply

The power supply block distributes clean power to the Stratix II GX device. You can either power-up using an on-board regulator or an external power supply via banana jacks. However, if the Stratix II GX device's power consumption is above 4 W, you should use an external power supply and a heat sink.

The board has two types of voltage regulators:

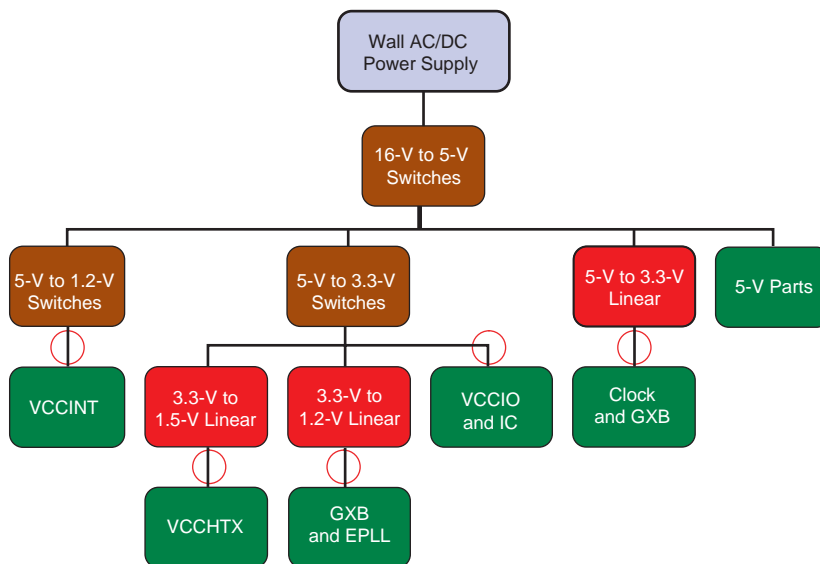
- Switching regulators
- Linear regulators

Switching regulators are used for digital circuits and linear regulators are used for analog circuits. [Table 2–19](#) lists board regulators' specifications.

Board Reference	Type	Voltage Output	Provides Power To	Manufacturer	Manufacturer Part Number
U12	Switching regulator	16 V to 5 V	<ul style="list-style-type: none"> ● USB UART ● Regulators 	Texas Instruments	PTN78020W
U11	Dual output switching regulator	5 V to 3.3 V	<ul style="list-style-type: none"> ● VCCIO for FPGA ● 7-segment display ● LEDs ● Push buttons ● EPCS64 device 	Texas Instruments	PTH05060W
U13	Dual output switching regulator	5 V to 1.2 V	<ul style="list-style-type: none"> ● VCCINT for FPGA 	Texas Instruments	PTH05060W
U14	Linear regulator	5 V to 3.3 V	<ul style="list-style-type: none"> ● FPGA transceiver block (VCCA pins) ● Clock circuitry 	Texas Instruments	TPS78633KTTR
U15	Dual output linear regulator	3.3 V to 1.5 V/1.2 V	<ul style="list-style-type: none"> ● FPGA transceiver block (VCCH pins) 	National Semiconductor	LP38842MR-ADJ
U16	Linear regulator	3.3 V to 1.2 V	<ul style="list-style-type: none"> ● FPGA transceiver block (VCCT, VCCR, and VCCL pins) 	National Semiconductor	LP3883ES-1.2

Figure 2–16 shows the board’s power supply block.

Figure 2–16. Power Supply Block Diagram



The decoupling analysis for this board is performed for a maximum current consumption by the different power supplies, see Table 2–20.

Table 2–20. Power Supply Pins & Maximum Current Consumption

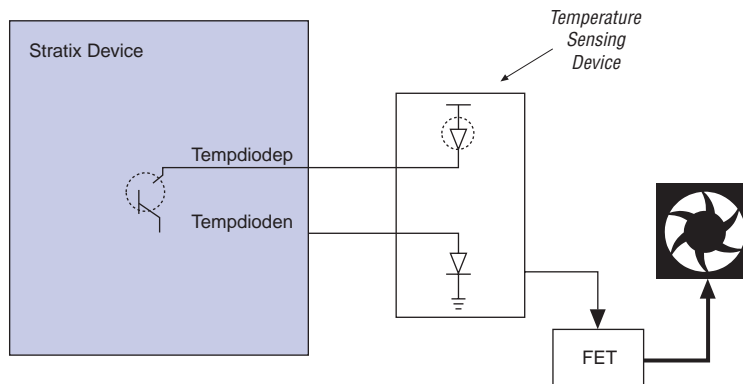
Power Supply Net Name in Schematic	Power Supply Pins Connected in Stratix II GX Device	Maximum Expected Current Consumption
1V2	VCCINT and VCCP	4.75 A
VCCTX	VCCH	290 mA
1V2A	VCCR and VCCT	1.70 A
3V3	VCCIO and external components	2.45 A
3V3A	VCCA and external components	1.04 A

Thermal Management Block

To ensure that the Stratix II GX device operates in the specified thermal operating conditions, a thermal management unit is included on the board. The on-chip temperature sensing diode needs to be monitored by an external temperature sensor, which is the Maxim MAX1619 device (U17). Accordingly, a SMBus interface in the PLD fabric of the Stratix II GX device is required to monitor the thermal data, and potentially, be an active participant with the active-cooling mechanism.

Figure 2-17 shows the on-board thermal management system diagram.

Figure 2-17. Stratix II GX Thermal Management System



The active-cooling device is similar to the Radian FB35+K52+T725 active BGA cooler with clip.



For more information, go to the Radian website at <http://www.radianheatsinks.com/products.html>.

FPGA Configuration Block

To enable the highest configuration flexibility while maintaining the lowest-cost and lowest-component usage, the on-board Stratix II GX device can be configured in one of two ways:

- JTAG configuration
- Active serial configuration using an EPCS64 device

JTAG Configuration

The Stratix II GX device can be configured after power is applied to the board. The JTAG interface permits the Quartus® II software to load the Stratix II GX device with a user design through an Altera download cable. The user design remains in the Stratix II GX device until power is removed from the board.

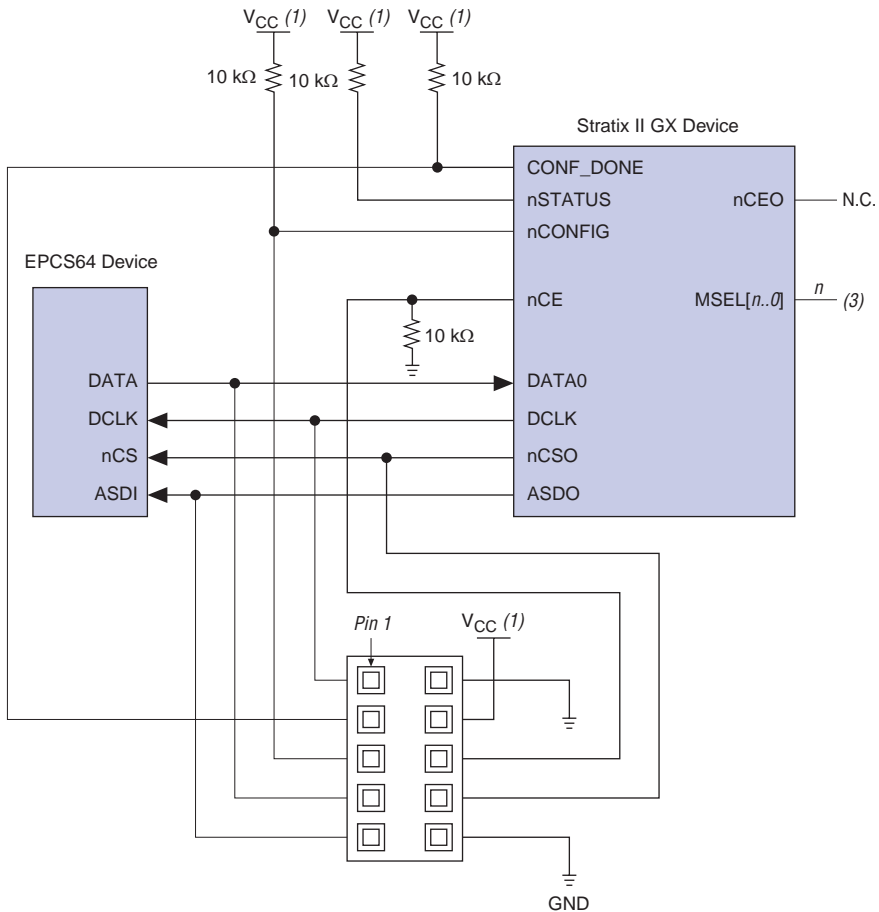


The JTAG configuration scheme bonds the JTAG ports to a set of header connections. This scheme allows direct device configuration as well as support for the Altera SignalTap® II embedded logic analyzer for debugging and logic probing.

Active Serial Configuration Using EPCS64 Device (U22)

The active serial configuration scheme uses a serial configuration device (EPCS64), allowing the board to support the out-of-the-box experience. The demo design and the Nios II embedded processor's user code are stored on the EPCS64 device and automatically configure the Stratix II GX device upon power-up. If the load is not successful, the CONF DONE LED (D14) does not illuminate and the Stratix II GX device is not configured. If the load is successful, the CONF DONE LED illuminates. See [Figure 2-18](#).

Figure 2–18. Active Serial Configuration Scheme



For more information about Stratix II GX configuration, refer to the *Configuring Stratix II and Stratix II GX Devices* chapter in volume 1 of the *Configuration Handbook*.

Flash Memory

To support the board's out-of-the-box configuration option, flash memory is available on the board. The flash memory also provides a second option when storing non-volatile memory for the Nios II processor's user code. Therefore, the non-volatile memory can either be stored in internal memory (after configuration with an EPCS64 device) or in flash memory.

The on-board flash memory provides two main benefits:

- Provides a second option when storing non-volatile memory
- Useful when a smaller density, but migratable device, is used on the board but does not have enough internal memory to support the demo design.

To reduce the flash controller's development cycle, a common flash interface (CFI) flash memory is used. This provides device-specific information to the system, allowing host software to easily reconfigure for different flash devices. On this board, the CFI controller available in the Quartus II SOPC Builder library is used, which reduces development time when interfacing with flash memory.

The on-board flash memory is the Spansion LLC S29GL128N11TFI020, which is a 128-Mbit memory module. The memory is available in either a 56-pin TSOP or a 64-pin FBGA. For simplicity and cost effectiveness, the board uses the TSOP package.