



Reduce Cost, Power, and Size

Designing Remote Radio Head Applications with Transceiver FPGAs

To drive down cost, power consumption, and form factor of your remote radio head (RRH) and RF card applications, build your designs with custom logic devices with transceivers. Altera's broad portfolio of transceiver FPGAs and ASICs, combined with easy-to-use software tools and intellectual property (IP), offers a variety of system-on-a-chip (SOC) options for RRH and RF card applications.

Faster Design Cycle, Lower Costs, Low Power

Our technologies support energy-efficient multi-mode RF/RRH module development, while also providing tools to help streamline your design cycle and reduce related costs.

Highly integrated, scalable, reconfigurable FPGA and ASIC SOC platforms

- Compact RRH with lower power consumption and bill of materials (BOM)
- Reconfigurable multi-mode, multi-band support
- Scalable multi-sector, multi-antenna support

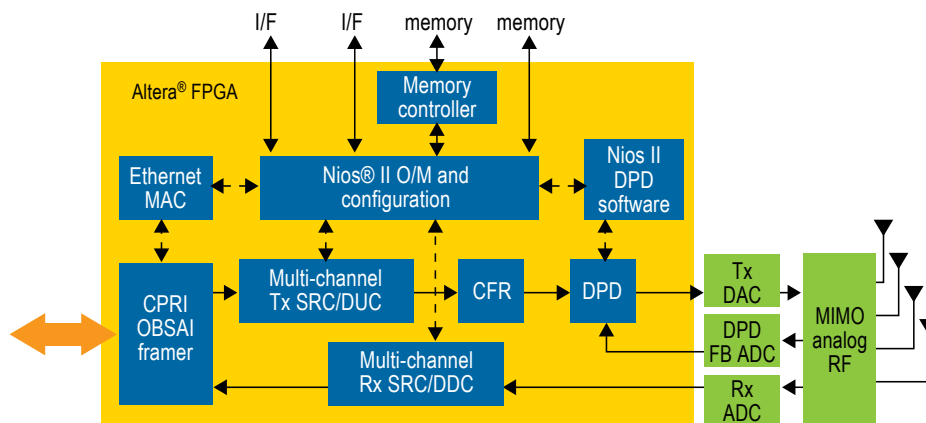
Multi-mode crest-reduction factor (CFR) and digital predistortion (DPD) solutions

- Improved power amplifier (PA) efficiency and lowered operating expenses
- Easy-to-use CFR and DPD reference designs

Productivity-enhancing tools, IP, and development boards

- Easy multi-channel digital upconverter (DUC) and digital downconverter (DDC) reference design with DSP Builder Advanced Blockset library
- Off-the-shelf IP cores for Common Public Radio Interface (CPRI) and Open Base Station Architecture Initiative (OBSAI) and JESD204A interfaces
- State-of-the-art RF hardware development and demonstration kits

RF Integration with Transceiver FPGAs



- Single sector, 2x2 MIMO - One Arria® II GX FPGA or multiple Cyclone IV GX FPGAs
- Single sector 4x4 MIMO or 8x8 MIMO. One Stratix® IV GX/HardCopy® IV GX device or multiple Arria II GX and GZ FPGAs

Choosing the Right Device

Our transceiver FPGAs and ASICs provide a number of options for performance, densities, transceiver channels, power, and more. The portfolio includes:

- Stratix V GX FPGAs, which feature up to 622K logic elements (LEs), 612 18x18 multipliers, and 66 full-duplex clock data recovery- (CDR-) based transceivers at up to 12.5 Gbps.
- HardCopy V ASICs, which feature an equivalent transceiver block and package- and pin-compatibility to Stratix V FPGAs to help you achieve the lowest risk and lowest total cost in ASIC designs with embedded transceivers.
- Arria II GX and GZ FPGAs, low-power, cost-effective FPGAs that make using transceivers for applications up to 6.375 Gbps easy.
- Cyclone IV GX FPGAs, the market's lowest cost, lowest power FPGAs with up to 150K LEs, 360 18x18 multipliers, and up to 8 integrated 3.125-Gbps transceivers

Nios II Embedded Soft Processor

You can use Altera's Nios II soft processor to implement the DPD adaptation algorithm in software while also handling all the operation and maintenance functionality for the RRH.

- Time-critical software algorithms can be accelerated by adding custom instructions to the Nios II processor instruction set.
- Using custom instructions, you can reduce a complex sequence of standard instructions to a single instruction implemented in hardware.
- The Nios II configuration wizard, part of Quartus II software's SOPC Builder, provides a GUI used to add up to 256 custom instructions to the Nios II processor, including floating point operations.
- Alternatively, hardware accelerators can also be created using the C-to-Hardware (C2H) acceleration compiler included in the Nios II Embedded Design Suite.

RF/RRH Reference Designs

RF/RRH Reference Designs	Altera	Partner
Interface IP	CPRI, OBSAI RP3-01, JESD204A	
DUC/DDC	Multi-standard, multi-carrier, multi-antenna DUC/DDC	
CFR	Multi-standard CFR	
DPD	DPD framework	Multi-standard DPD
Hardware platforms	Stratix IV GX, Arria II GX, and Cyclone IV GX development kits	System-level analog platforms

DSP Builder Advanced Blockset Tool

With the DSP Builder feature of Quartus® II design software, you have a synthesis tool that quickly implements Simulink designs in high-performance FPGA platforms. An enhancement to this feature, the DSP Builder Advanced Blockset library, provides a number of new Simulink blocksets that further increase productivity, particularly for the synthesis of multi-channel designs. You'll also have a unique synthesis technology that optimizes the high-level, unregistered netlist into a pipelined register transfer level (RTL) targeted and optimized to your chosen device and desired clock rate.

Want to Dig Deeper?

For more information about how Altera's transceiver device portfolio can support your RRH applications, contact your local sales representative or FAE, or visit www.altera.com/wireless.

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