



*Reduce System Cost, Power, and Size*

## Designing Base Transceiver Station (BTS) Channel Cards with Transceiver FPGAs and ASICs

Low total system cost, scalable form factor, low power consumption, programmability—all are key requirements for reducing both capital and operating expenses for Long Term Evolution (LTE) basestations. To meet these mandates—while increasing your design team's productivity—look to Altera for the market's broadest portfolio of transceiver FPGAs and ASICs.

Delivering a variety of system-on-a-chip (SOC) options for channel card applications, our portfolio includes:

- Stratix® IV GX FPGAs, high-performance 40-nm devices with up to 530K logic elements (LEs) and unprecedented system bandwidth with superior signal integrity.
- HardCopy® IV GX ASICs, low-risk 40-nm ASIC technology with 6.5-Gbps transceiver option and package and pin compatibility with Stratix IV FPGAs.
- Arria® II GX and GZ FPGAs, the lowest power, cost-optimized 40-nm FPGAs with transceivers up to 6.375 Gbps.
- Cyclone® IV GX FPGAs, the market's lowest cost, lowest power FPGAs, with integrated 3.125-Gbps transceivers.
- Quartus® II software, a single, comprehensive design environment providing the industry's fastest compile times.
- A common set of intellectual property (IP) cores that provide building blocks you can drop into your system designs for a variety of functions.

### Unleashing Silicon Potential with SOC IP and Solutions

- Best-in-class hardware acceleration IP for algorithmic functions (FFT, IDFT, matrix manipulation, etc.) and bit manipulation (turbo decoding, rate de-matching, etc.)
- Differentiation with custom hardware accelerators
- Software controlled, C-based design entry on soft processors
- Soft datapath task scheduler to abstract control complexity and avoid state machines
- Heterogeneous multi-core solution provides performance capabilities beyond traditional digital signal processing (DSP) devices
- Highly scalable and flexible SOC platform architecture allowing scaling for various targets, from macrocell down to femtocell
- SOPC Builder system integration tool, which synthesizes connectivity by assembling SOC library components

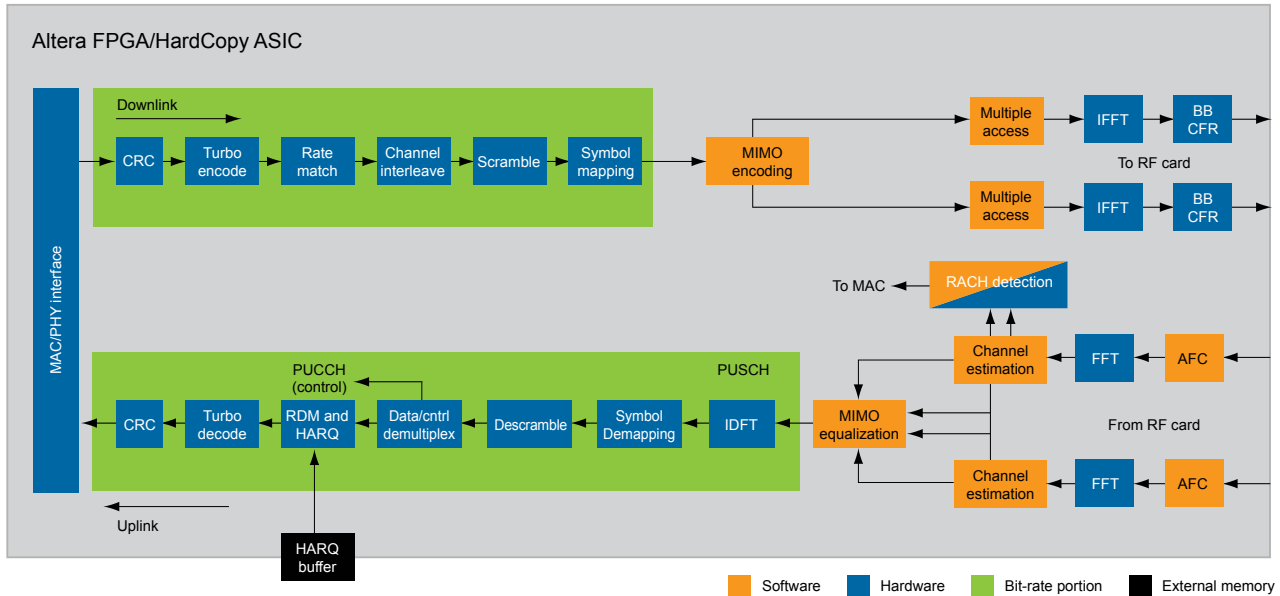
### Integrated SOC Solutions

As the lowest power, highest performance high-end FPGAs, Stratix IV FPGAs can be the foundation of highly integrated SOC solutions, providing these key benefits:

- Single-chip SOC for 1 sector, 20 MHz, 4x4 multiple-input, multiple-output (MIMO) technology.
- Fewer devices for multi-sector configurations, enabling compact platforms at lower bill of materials (BOM) cost.
- Lower power consumption with 40-nm process benefits and Programmable Power Technology, which automatically optimizes logic, digital signal processing (DSP), and memory blocks for the lowest power at your required performance.
- Superior vertical migration portfolio with the same pin-out, allowing scalable form factor solutions for various channel card configurations.
- Seamless migration path to HardCopy IV ASICs for volume production.

Arria II FPGAs deliver the processing bandwidth, predictable latency, low power, and flexibility for coprocessing and interface functionalities on the channel card. Cyclone IV FPGAs are ideal for cost-sensitive implementations requiring transceivers and low power consumption.

## Example of Hardware/Software Partitioning for Custom SOC



### LTE single sector, 20-MHz, 4x4 MIMO in a single FPGA or HardCopy ASIC device

## Advantages of Latest-Generation FPGAs and ASICs in SOC Designs

- High performance at lower BOM cost
- High integration for reduced board footprint
- Fewer devices and unique hardware/software partitioning, which lower power consumption
- Same SOC platform architecture for both FPGA and HardCopy ASIC, which reduces risk and significantly lowers development cost
- Custom hardware/software partition determined by your system architect, to optimize for your specific requirements
- **Net result**—a custom, single-device, SOC, scalable, reprogrammable platform that offers:
  - Higher MIMO and bandwidth density compared to competitive offerings
  - Lower power consumption per channel

## Want to Dig Deeper?

For more information about channel card system design with FPGAs and ASICs, contact your local Altera sales representative or FAE. Find white papers, webcasts, reference designs, and other resources at [www.altera.com/wireless](http://www.altera.com/wireless).

## Altera IP Reduces Development Time and Cost

Mixed radix DFT/IDFT

Symbol demapper (SDM)

Descrambler

Rate de-matching (RDM)

Turbo encoder for LTE and UMTS

Turbo decoder for LTE and UMTS

Transport block CRC

PUSCH uplink bit rate chain

24K FFT for RACH detection

FFT/IFFT compiler

1536 FFT/IFFT

2x2 MMSE MIMO equalisation

Channel estimation

Zadoff-Chu sequence generation

Uplink symbol rate chain

Crest factor reduction

Matrix decomposition

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