



Nios II Embedded Design Suite 7.1 Release Notes

May 2007, Version 7.1

Release Notes

This document contains release notes for the Nios® II Embedded Design Suite (EDS) version 7.1.

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New Features and Enhancements

The Nios II EDS version 7.1 addresses issues found in previous releases, and adds the following primary features:

- Nios II Software Build Tools design flow
- Arria™ GX device family support
- Design examples including new SOPC Builder components
 - Triple Speed Ethernet Media Access Controller (MAC) MegaCore
 - Scatter-gather Direct Memory Access (DMA) Controller

The following sections provide a detailed list of all product updates, including known issues fixed in this release.

Device and Host Support

This release supports the following Altera® FPGA families:

- Arria GX
- Cyclone™ III
- Stratix® III
- Stratix II and Stratix II GX
- Stratix and Stratix GX
- Cyclone II
- Cyclone



The host system requirements for the Nios II EDS are based on the requirements for the Altera Complete Design Suite. Refer to *Quartus® II Installation and Licensing for PCs* or *Quartus II Installation and Licensing for UNIX and Linux Workstations* manual.

Installation and Licensing Instructions



For installation instructions, refer to *Quartus II Installation and Licensing for PCs* or *Quartus II Installation and Licensing for UNIX and Linux Workstations* on the Altera website at www.altera.com/literature/lit-qts.jsp.

Using Previously Installed Versions of the Nios II EDS

SOPC Builder and the Nios II Integrated Development Environment (IDE) refer to the most recently installed version of components (such as the Nios II processor and peripherals) and their software drivers. To revert to a prior released version of the Nios II development tools, you can reinstall the previous version of tools or modify the following environment variables:

- `SOPC_BUILDER_PATH` — Ensure that `SOPC_BUILDER_PATH` points to the installation directory of the desired Nios II version and no other Nios II versions. `SOPC_BUILDER_PATH` must also contain the paths of other IP, separated by `+`. For example:

```
SOPC_BUILDER_PATH=C:\altera\71\ip\sopc_builder_ip+C:\altera\71\ip\nios2_ip+
C:\altera\71\ip\triple_speed_ethernet\lib\sopc_builder+C:\altera\71\ip\ddr_ddr2_sdram\lib\sopc_builder
```

- `SOPC_BUILDER_PATH_<version>` — Ensure that `SOPC_BUILDER_PATH_<version>` points to the installation directory of the corresponding Nios II version. This environment variable is necessary only for versions 6.0 and 5.1. Exclude the period in `<version>`. For example:

```
SOPC_BUILDER_PATH_60=c:\altera\kits\nios2_60
```

- `SOPC_KIT_NIOS2` — Ensure `SOPC_KIT_NIOS2` points to the installation directory of the desired Nios II version and no other Nios II versions. For example:

```
SOPC_KIT_NIOS2=C:\altera\71\nios2eds
```

After modifying `SOPC_BUILDER_PATH`, `SOPC_BUILDER_PATH_<version>`, and `SOPC_KIT_NIOS2`, launch the corresponding version of the Quartus II software to ensure that the `QUARTUS_ROOTDIR` environment variable is updated. Exit the Quartus II software immediately. After you complete this step, the next time you launch any part of the Altera Complete Design Suite, the version you select runs.

For Windows, there is a batch script called **Altera_Tool_Switch.bat**, along with a special version of **setenv.exe** which can update system variables. **Altera_Tool_Switch.bat** automates the process of updating the system variables to switch versions of Altera software. To get these tools, download ftp://ftp.altera.com/outgoing/download/kdb/Altera_Tool_Switch.zip.



Altera strongly recommends that you uninstall any Beta versions of the Nios II EDS v7.1 before installing the release version.

Installation Path Length

During installation of the Nios II EDS on Windows, you might receive a **Feature Transfer Error** message indicating that the filename or extension is too long. This error might occur if your install path is too long. Use an install location with a shorter path, for example, `C:\altera\`.

Nios II Processor Cores

This section describes changes to the Nios II processor cores.

There are no major changes to Nios II processor cores in this release.

SOPC Builder

This section describes changes to SOPC Builder which affect Nios II designers.



For complete revision history of SOPC Builder and the Quartus II software, refer to the release notes for the Quartus II software version 7.1. The *Quartus II Handbook, Volume 4: SOPC Builder* contains complete documentation for SOPC Builder.

The Quartus II version 7.1 release notes include information on SOPC Builder changes and the new embedded peripherals provided with SOPC Builder in this release.

When you open an SOPC builder system created in a previous version of the tools, a dialog box appears. For information on upgrading SOPC Builder systems to version 7.1, select the **More Information** option.

Nios II IDE

This section describes changes to the Nios II integrated development environment (IDE).

There are no major changes to the Nios II IDE in this release.

Nios II Software Build Tools

The Nios II Software Build Tools are introduced in the Nios II EDS version 7.1. The Nios II software build tools are command line utilities and scripts that provide similar functionality to the New Project wizard and the System Library properties page in the Nios II IDE. The software build tools also provide scripting capabilities.



Refer to the *Nios II Software Build Tools* chapter in the *Nios II Software Developer's Handbook* for details.

Nios II C-to-Hardware Acceleration (C2H) Compiler

This section describes changes to the Nios II C2H Compiler.

Integration with Nios II Software Build Tools

The C2H Compiler is supported by the Nios II software build tools.

Interrupt Generation

You can compile a top-level function to an accelerator that runs in interrupt mode.



For details on these features, refer to the *Nios II C2H Compiler User Guide*.

Flash Programmer

This section describes changes to the flash programmer in the Nios II IDE.

There are no major changes to the Flash Programmer in this release.

Target Software

This section describes changes to Altera-provided target software which runs on the Nios II processor, such as the hardware abstraction layer (HAL).

There are no major changes to the target software in this release.

Example Designs

Hardware Example Designs

HDL Top Level Design Files

The hardware examples in version 7.1 contain Verilog HDL or VHDL top level files. Block Design Files (**.bdf**), formerly included as schematic top level files, are no longer present. The system HDL file generated by SOPC Builder is the top level file for most of the example projects, demonstrating how SOPC Builder can simplify your system design process. This change removes the chance of introducing incorrect pin connections in the top level schematic file. For instructions on creating BDF top level files for the examples, refer to the **readme.txt** file included with any hardware example design.

Nios Development Board, Stratix ES Edition Example Designs Removed

The hardware examples for the Nios II 1S10ES development boards are removed in the Nios II EDS v7.1. These boards are obsolete.

TSE SG-DMA

The new Triple Speed Ethernet Scatter-Gather DMA (TSE SG-DMA) hardware design example is included for the Nios Development Board, Stratix II RoHS-compliant edition and Cyclone II edition. This design demonstrates the use of the Altera TSE MAC and SG-DMA components for Ethernet applications. For details on the design examples, refer to the Nios II EDS v7.1 Documentation Launch Pad. To view the Documentation Launch Pad, in the Windows Start menu point to **Programs, Altera, Nios II EDS 7.1**, and click on **Nios II 7.1 Documentation**.

Fast

Fast hardware example designs are included targeting Cyclone III and Stratix III devices. Refer to the Nios II EDS v7.1 Documentation Launch Pad for details on the design examples. To view the Documentation Launch Pad, in the Windows Start menu point to **Programs >>> Altera >>> Nios II EDS 7.1**, and click on **Nios II 7.1 Documentation**.

Small

A Joint Test Action Group (JTAG) UART is now included in the **small** hardware example designs to enable communication with the host machine.

Software Example Designs

Web Server

The Web Server software example now demonstrates control of board components over Ethernet.

Simple Socket Server and Web Server Default IP Address

The default IP addresses in these examples are updated to allow for Dynamic Host Configuration Protocol (DHCP) request packets to penetrate secure routers. The address was changed from **192.168.X.X** to **0.0.0.0**.

Errata Fixed in This Release

This section lists those errata items from previous releases that are fixed in version 7.1.

Fixed in Version 7.1: Nios II/e Core Burst Support

The Nios II wizard incorrectly allowed you to select burst support for the instruction master port in the Nios II/e core. Instruction master burst support in Nios II requires an instruction cache. The Nios II/e core does not include an instruction cache; therefore burst support can not be enabled.

Fixed in Version 7.1: Interrupt Vector Custom Instruction in Multiprocessor Systems

In designs containing multiple Nios II processors, enabling the interrupt vector custom instruction in more than one of the processors caused the following errors during Quartus II compilation:

```
Error (10430): VHDL Primary Unit Declaration error at
interruptvector_cpu_1.vhd(26): primary unit "interrupt_vector" already exists in
library "work"
Error (10523): Ignored construct interruptvector_cpu_1 at
interruptvector_cpu_1.vhd(64) due to previous errors
Error: Node instance "the_interruptvector_cpu_1" instantiates undefined entity
"interruptvector_cpu_1"
```

Fixed in Version 7.1: "nios_cpu: Unknown Break Location" Error Message

If you modified the Nios II core in an existing system by disabling the JTAG debug module in the Nios II configuration wizard, you might have received the error message **nios_cpu: Unknown Break Location nios_cpu/jtag_debug_module** during SOPC Builder generation.

Fixed in Version 7.1: Windows XP: Internal Error When Repeatedly Using Step Into

If you repeatedly used the **Step Into** command while debugging on Windows XP, you might have received the internal error, **Retrieving Children: An internal error occurred during: Retrieving Children**.

Fixed in Version 7.1: Unable to Save Files Containing Copyright Symbol

On computers using character encoding other than Windows-1252, the copyright symbol included in the **board_diag.c** file was not recognized. Because of this character, the file could not be saved using the Nios II IDE.

Fixed in Version 7.1: MicroC/OS-II "Source not found" Error When Debugging

You might have received a **Source not found** error message if you stepped into MicroC/OS-II code or broke on a program entry point while debugging your application.

Fixed in Version 7.1: Incorrect Stack Checking with Interrupt Vector Custom Instruction

If you enabled run-time stack checking in systems that included the interrupt vector custom instruction, the Nios II IDE sometimes erroneously reported a stack overflow or sometimes failed to report an actual stack overflow.

Fixed in Version 7.1: Nios II IDE Did Not Recognize Executable File Built Outside IDE

If you used a build process external to the Nios II IDE, the IDE sometimes did not recognize when you generated or regenerated the executable linkable file (.elf) for your project. In this case, the IDE debugger reported that the executable file did not exist.

Fixed in Version 7.1: Comma Operators Not Supported

The C2H Compiler did not support comma operators, such as in the following example:

```
for(i = 0, j = 3; i < 10; i++, j++)
{
    /* statements */
}
```

Fixed in Version 7.1: Failure Verifying Flash With the nios2-flash-programmer Command

Using the **nios2-flash-programmer** command line utility to verify flash contents using the `--verify` argument sometimes resulted in a verify failure, even when flash contents were correct. The failure message was similar to the following:

```
Verifying 00000000 ( 0%)Failed to verify at around 00000000 Verify failed
```

Fixed in Version 7.1: Using Nios II Flash Programmer With Override File in <Nios II EDS path>/bin Generated Error

An error resembling the following sometimes appeared:

```
4 [main] nios2-flash-programmer 4440 _cygtls::handle_exceptions: Error while
dumping state (probably corrupted stack) Segmentation fault (core dumped)
```

Fixed in Version 7.1: Nios II Processor Reference Handbook Referred Erroneously to the Data Bus

In the *Implementing the Nios II Processor in SOPC Builder* chapter of the *Nios II Processor Reference Handbook*, under *Caches and Tightly Coupled Memories Tab*, the following text appeared under *Instruction Settings*: "Usually you enable bursts on the processor's data bus when processor data is stored in DRAM, and disable bursts when processor data is stored in SRAM." This sentence now reads "Usually you enable bursts on the processor's instruction master when instructions are stored in DRAM, and disable bursts when instructions are stored in SRAM."

Revision History

Table 1 shows the revision history for the Nios II Embedded Design Suite v7.1 Release Notes.

Table 1. Nios II Embedded Design Suite v7.1 Errata Sheet Revision History

Version	Date	Summary
1.0	May 2007	First release
1.1	May 2007	<ul style="list-style-type: none"> Remove mention of Web Server remote configuration Remove mention of incorrect SSRAM PLL phase shift in Stratix 2S60 RoHS and Cyclone II 2C35 designs



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