

Stratix V FPGA Family Package and I/O Selector Guide



Stratix V FPGA Features

The following features, packages, and I/O matrices give you an overview of our devices. To get the full story, check out our online selector guide: www.altera.com/selector.

		Stratix® V GX and GT FPGAs (0.85 V), Up to 28G Transceivers ¹									
		5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXAB	5SGXB5	5SGXB6	5SGTC5	5SGTC7
Density and Speed	ALMs	75,500	113,000	160,500	234,750	317,000	397,000	185,000	225,000	160,500	234,750
	Equivalent LEs	200,000	300,000	425,000	622,000	840,000	1,052,000	490,000	597,000	425,000	622,000
	Registers ²	302,000	452,000	642,000	939,000	1,268,000	1,588,000	740,000	901,000	642,000	939,000
	M20K memory blocks	800	1,316	2,304	2,560	1,600	2,016	2,100	2,660	2,304	2,560
	MLAB memory (Mb)	2.3	3.44	4.89	7.16	9.67	12.12	5.65	6.87	4.89	7.16
	Embedded memory (Mb)	16	26	45	50	31	39	41	52	45	50
	18-bit x 18-bit multipliers	376	376	512	512	1,000	1,500	798	798	512	512
	Speed grades (fastest to slowest)	-2, -3, -4									
Architectural Features	Global clock networks	16									
	Regional clock networks	92									
	Design security	✓									
	HardCopy® series device support	✓									
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3 ²									
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)									
	LVDS channels, 1.4 Gbps (receive/transmit)	156	156	210	210	210	210	150	150	150	150
	Embedded DPA circuitry	✓									
	Series and differential OCT	✓									
	Transceiver (SERDES) channels (28 Gbps/ 14.1 Gbps)	0/24 or 36	0/24 or 36	0/24, 36, or 48	0/24, 36, or 48	0/36 or 48	0/36 or 48	0/66	0/66	4/32	4/32
	PCI Express® hard IP blocks	1 or 2	1 or 2	1 or 4	1 or 4	1 or 4	1 or 4	1 or 4	1 or 4	1	1
	100-Gbps Ethernet (100GbE) hard IP blocks	No	No	Yes	Yes	No	No	No	No	Yes	Yes
Memory devices supported	DDR3, DDR2, DDR, QDR II, RLD RAM II, SDR										

¹ All data is preliminary

² 3.3-V compliant, requires a 3.0-V power supply
















Stratix V FPGA Features Cont.

		Stratix V GS and E FPGAs (0.85 V), Up to 14.1-Gbps Transceivers ¹							
		5SGSD2	5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8	5SEE9	5SEEA
Density and Speed	ALMs	49,000	89,000	125,000	174,000	220,000	265,000	317,000	397,000
	Equivalent LEs	130,000	236,000	332,000	462,000	583,000	703,000	804,000	1,052,000
	Registers ²	196,000	356,000	500,000	696,000	880,000	1,060,000	1,268,000	1,588,000
	M20K memory blocks	450	688	1,062	1,950	2,320	2,688	1,600	2,016
	MLAB memory (Mb)	1.50	2.70	3.80	5.30	6.70	8.10	9.67	12.12
	Embedded memory (Mb)	9	14	22	40	48	55	31	39
	18-bit x 18-bit multipliers	650	1,260	1,892	2,966	3,550	4,096	1,000	1,500
	Speed grades (fastest to slowest)	-2, -3, -4							
Architectural Features	Global clock networks	16							
	Regional clock networks	92							
	Design security	✓							
	HardCopy series device support	✓							
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3 ²							
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)							
	LVDS channels, 1.4 Gbps (receive/transmit)	100	125	140	175	225	225	210	210
	Embedded DPA circuitry	✓						x	
	Series and differential OCT	✓							
	Transceiver (SERDES) channels (14.1 Gbps)	12	18	36	36	48	48	0	0
	PCI Express hard IP blocks	1	1	1	1	2	2	0	0
	100GbE hard IP blocks	No							
Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR								


¹ All data is preliminary

² 3.3-V compliant, requires a 3.0-V power supply

Stratix V Series Package and I/O Matrices

Stratix V GX, GT, GS, and E FPGAs (0.85 V), Up to 28G Transceivers							
	Hybrid FPGA (H)		FBGA (F)				
	780 pin ¹ 35 x 35 (mm) 1.0-mm pitch	1,152 pin ² 40 x 40 (mm) 1.0-mm pitch	484 pin 23 x 23 (mm) 1.0-mm pitch	780 pin 29 x 29 (mm) 1.0-mm pitch	1,152 pin 35 x 35 (mm) 1.0-mm pitch	1,152 pin 35 x 35 (mm) 1.0-mm pitch	1,517 pin 40 x 40 (mm) 1.0-mm pitch
5SGXA3	264, 66, 24 				552, 138, 24 	444, 111, 36 	624, 156, 36 
5SGXA4	264, 66, 24 				552, 138, 24	444, 111, 36	624, 156, 36
5SGXA5					552, 138, 24	444, 111, 36	696, 174, 36
5SGXA7					552, 138, 24	444, 111, 36 	696, 174, 36
5SGXA9							696, 174, 36
5SGXAB							696, 174, 36
5SGXB5							
5SGXB6							
5SGTC5							
5SGTC7							
5SGSD2			240, 60, 9 	400, 100, 12 			
5SGSD3			240, 60, 9 	400, 100, 12 	500, 125, 18		
5SGSD4				400, 100, 12 	560, 140, 24		700, 175, 36
5SGSD5					560, 140, 24 		700, 175, 36
5SGSD6							700, 175, 36
5SGSD8							700, 175, 36 
5SEE9		552, 138, 0 					
5SEE9		552, 138, 0 					

 Number indicates available user I/O pins.

 Vertical migration (same V_{CC}, GND, ISP, and input pins). User I/Os may be less than labelled for vertical migration.
Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

¹These device and pincount combinations are supported in the Hybrid F780 (35 mm) package

²These device and pincount combinations may only be supported in the Hybrid (40 mm) or SuperHybrid (43 mm) package

Stratix V Series Package and I/O Matrices Cont.

Stratix V GX, GT, GS, and E FPGAs (0.85 V), Up to 28G Transceivers						
FBGA (F)						
	1,517 pin 40 x 40 (mm) 1.0-mm pitch	1,517 pin 40 x 40 (mm) 1.0-mm pitch	1,517 pin 40 x 40 (mm) 1.0-mm pitch	1,760 pin 43 x 43 (mm) 1.0-mm pitch	1,932 pin 45 x 45 (mm) 1.0-mm pitch	1,932 pin 45 x 45 (mm) 1.0-mm pitch
5SGXA3						
5SGXA4						
5SGXA5	600, 150, 48				840, 210, 48	
5SGXA7	600, 150, 48				840, 210, 48	
5SGXA9					840, 210, 48	
5SGXAB					840, 210, 48	
5SGXB5		432, 108, 66		600, 150, 66		
5SGXB6		432, 108, 66		600, 150, 66		
5SGTC5	600, 150, 48					
5SGTC7	600, 150, 48					
5SGSD2						
5SGSD3						
5SGSD4						
5SGSD5						
5SGSD6					900, 225, 48	
5SGSD8					900, 225, 48	
5SEE9			696, 174, 0			840, 210, 0
5SEE9			696, 174, 0			840, 210, 0

²⁸⁸ Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). User I/Os may be less than labelled for vertical migration.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.