

# HardCopy III ASIC Product Table



v0.995	HardCopy® III ASIC		Stratix® III FPGA Prototype		HardCopy III Resource (Stratix III FPGA Prototype Max Resource) <sup>1</sup>							
HardCopy Base Die	Package <sup>2</sup> (Body Size)	Generic Part Number	Prototyping Device	LEs	ASIC Gates <sup>3</sup>	I/O Pins <sup>4</sup>	Full Duplex LVDS Pairs <sup>5</sup>	18x18 Multipliers	PLLs	Total Embedded Memory Bits <sup>6</sup>	M9Ks	M144Ks
HC325	WF484 (23 mm) FF484 (23 mm)	HC325WF484N HC325FF484N	EP3SL110--F780 <sup>7</sup>	107K	2.7M	296 (488)	48 (56)	288	4	4.1M	275	12
			EP3SL150--F780 <sup>7</sup>	142K	3.6M	296 (488)	48 (56)	384	4	5.4M	355	16
			EP3SE110--F780 <sup>7</sup>	107K	5.8M	296 (488)	48 (56)	896	4	7.9M	639	16
			EP3SL200--H780 <sup>7</sup>	199K	5.3M	296 (488)	48 (56)	576	4	8.6M (9.2M)	468	32 (36)
			EP3SE260--H780 <sup>7</sup>	254K	6.9M	296 (488)	48 (56)	768	4	12.1M (14.3M)	864	32 (48)
			EP3SL340--H1152 <sup>7</sup>	338K	7.0M	296 (744)	48 (88)	576	4 (8)	12.1M (15.9M)	864 (1,040)	32 (48)
	WF780 (29 mm)	HC325WF780N	EP3SL110--F780	107K	2.7M	392 (488)	48 (56)	288	4	4.1M	275	12
			EP3SL150--F780	142K	3.6M	392 (488)	48 (56)	384	4	5.4M	355	16
			EP3SE110--F780	107K	5.8M	392 (488)	48 (56)	896	4	7.9M	639	16
			EP3SL200--H780	199K	5.3M	392 (488)	48 (56)	576	4	8.6M (9.2M)	468	32 (36)
			EP3SE260--H780	254K	6.9M	392 (488)	48 (56)	768	4	12.1M (14.3M)	864	32 (48)
			EP3SL340--H1152 <sup>7</sup>	338K	7.0M	392 (744)	48 (88)	576	4 (8)	12.1M (15.9M)	864 (1,040)	32 (48)
	FF780 (29 mm)	HC325FF780N	EP3SL110--F780	107K	2.7M	488	56	288	4	4.1M	275	12
			EP3SL150--F780	142K	3.6M	488	56	384	4	5.4M	355	16
			EP3SE110--F780	107K	5.8M	488	56	896	4	7.9M	639	16
			EP3SL200--H780	199K	5.3M	488	56	576	4	8.6M (9.2M)	468	32 (36)
			EP3SE260--H780	254K	6.9M	488	56	768	4	12.1M (14.3M)	864	32 (48)
			EP3SL340--H1152 <sup>7</sup>	338K	7.0M	488 (744)	56 (88)	576	4 (8)	12.1M (15.9M)	864 (1,040)	32 (48)
HC335	FF1152 (35 mm)	HC335FF1152N	EP3SL150--F1152	142k	3.6M	744	88	384	8	5.4M	355	16
			EP3SE110--F1152	107K	5.8M	744	88	896	8	7.9M	639	16
			EP3SL200--F1152	199K	5.3M	744	88	576	8	9.2M	468	36
			EP3SE260--F1152	254K	6.9M	744	88	768	8	14.3M	864	48
			EP3SL340--H1152	338K	7.0M	744	88	576	8	15.9M	1040	48
	FF1517 (40 mm)	HC335FF1517N	EP3SL200--F1517	199K	5.3M	880 (976)	88	576	12	9.2M	468	36
			EP3SE260--F1517	254K	6.9M	880 (976)	88 (112)	768	12	14.3M	864	48
			EP3SL340--F1517	338K	7.0M	880 (976)	88 (112)	576	12	15.9M	1040	48

1. Number outside of () indicates available resource in HardCopy device, number inside () indicates maximum resource in FPGA

2. WF: low-cost wire-bond package; FF: performance-optimized flip-chip package

3. Calculated as 12 gates per LE plus 5,000 gates per 18x18 multiplier. Does not include RAMs, PLLs, test circuitry, and I/O registers.

4. For the F484, F780, and F1152 packaged devices, I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p and CLK10n) that can be used for data inputs. For the F1517 packaged devices, I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) and eight dedicated corner PLL clock inputs (PLL\_L1\_CLKp, PLL\_L1\_CLKn, LL\_L4\_CLKp, PLL\_L4\_CLKn, PLL\_R4\_CLKp, PLL\_R4\_CLKn, PLL\_R1\_CLKp, and PLL\_R1\_CLKn) that can be used for data inputs.

5. Each LVDS pair has one TX channel and one RX channel with DPA and soft CDR support

6. Memory bit count does not include MLAB memories which are constructed with HCells; 1 Mb = 1,024 x 1,024 bits

7. HardCopy devices are non-socket replacements for FPGAs