

HardCopy IV ASIC family features



All HardCopy® series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

HardCopy IV ASICs (0.9V) with 6.5+Gbps transceivers option¹

		HC4GX1YZ ⁵	HC4GX2YZ	HC4GX3YZ	HC4GX4YZ	HC4GX5YZ	HC4GX6YZ	HC4E2YZ	HC4E3YZ	HC4E4YZ	HC4E5YZ	HC4E6YZ	HC4E7YZ
FBGA (F)	484-pin (WF ²)							✓	✓				
	484-pin (LF ⁴)	✓	✓	✓				✓	✓				
	780-pin (WF)							✓	✓	✓			
	780-pin (LF)	✓	✓	✓	✓	✓		✓	✓	✓	✓		
	1,152-pin (LF)		✓	✓	✓	✓				✓	✓		
	1,152-pin (FF ³)			✓	✓	✓	✓			✓	✓	✓	✓
	1,517-pin (FF)			✓	✓	✓	✓			✓	✓	✓	✓

- ¹ All data is preliminary.
- ² WF = wire bond
- ³ FF = Performance-optimized flip chip
- ⁴ LF = Cost-optimized flip chip
- ⁵ Y = I/O count, Z = package type

HardCopy IV transceiver protocol support (GX only)

Protocol	Data rate
3G SDI	2.97
ASI	0.27
CEI-6G/SR/LR	6.375/4.976 - 6.375/4.976 - 6.375
CPRI	0.6144, 1.2288, 2.4576, 3.072
DDR-XAUI	6.25
Ethernet-XAUI	4 x 3.125
Fibre channel	1.0625, 2.125, 4.25, 6.52
Gigabit Ethernet	1.25
GPON	1.244 uplink, 2.488 downlink
HiGig+	3.75
HiGig2	4.0625
Interlaken	3.125 - 6.375
OBSAI	0.768, 1.536, 3.072
PCI Express Gen1, Gen2	2.5, 5.0
PCI Express Cable	2.5
SAS	1.5, 3.0, 6.0
SATA	1.5, 3.0
SDI SD/HD	0.27/1.485
SerialLite II	0.6 - 6.375
Serial RapidIO®	1.25, 2.5, 3.125
SFI5.1	2.488 - 3.125 (up to 8 channels)
SONET OC-3/OC-12/OC-48	0.155, 0.622, 2.488
SPAUI	3.2, 6.4

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		HC4GX1YZ	HC4GX2ZY	HC4GX3YZ	HC4GX4YZ	HC4GX5YZ	HC4GX6YZ	HC4E2YZ	HC4E3YZ	HC4E4YZ	HC4E5YZ	HC4E6YZ	HC4E7YZ	
Density and speed	Usable ASIC gates	2.8M	3.9M	9.2M	7.6M	9.5M	11.5M	3.9M	9.2M	7.6M	9.5M	11.5M	13.3M	
	Embedded memory (Mbits)	6.3	8.1	9.8-12.2	10.6-12.7	10.6-13.3	13.3	8.1	10.7	12.1-13.3	16.8	16.8	16.8	
	Max. 18-bit x 18-bit multipliers	384	512	1,288	832	1,040	1,024	512	1,288	832	1,040	1,024	1,024	
Architectural features	Embedded processor available	Nios® II processor												
	Phase-locked loops (PLLs)	3	3/4	3/6/8	3/6/8	3/6/8	6/8	4	4	4/8/12	4/8/12	8/12	8/12	
	Design security ²	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	Stratix® series prototyping support	EP4SGX 70	EP4SGX 110	EP4SGX 230	EP4SGX 290	EP4SGX 360	EP4SGX 530	EP4SE 110	EP4SE 230	EP4SE 290	EP4SE 360	EP4SE 530	EP4SE 680	
I/O features	I/O voltage levels supported	1.2, 1.5, 1.8, 2.5, 3.0												
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)												
	True-LVDS maximum data rate (Mbps)	150 to >1,250												
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength ³	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) data rate range	600 Mbps - 6.5+Gbps with PCS + PMA ⁴												
	6.5-Gbps transceiver (SERDES) channels	4/8	4/8/16	4/8/16/24	16/24	16/24	24	-	-	-	-	-	-	-
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RDRAM II SDR												

¹ All data is preliminary.

² Since all HardCopy ASICs contain hard-wired logic, they are inherently secure.

³ Settings are fixed post Design Review 2 (DR2).

⁴ Subject to increase, pending characterization.