



## Stratix IV GX FPGAs (0.9V) up to 8.5-Gbps transceivers <sup>1</sup>

**368** Number indicates available user I/O pins.

Vertical migration (same V<sub>CC</sub>, GND, ISP, and input pins). User I/O may be less than labelled for vertical migration.

All Stratix® series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

	Pin count	Body size	EP4SGX70D	EP4SGX110D	EP4SGX110F	EP4SGX230D	EP4SGX230F	EP4SGX230H	EP4SGX230K	EP4SGX290F	EP4SGX290H	EP4SGX290K	EP4SGX360F	EP4SGX360H	EP4SGX360K	EP4SGX530H	EP4SGX530K	EP4SGX530N
FBGA (F)	780-pin	29 x 29 mm	368	368		368				288 <sup>2</sup>			288 <sup>2</sup>					
	1,152-pin	35 x 35 mm			368		560			560			560					
	1,152-pin	35 x 35 mm						560			560			560			560 <sup>2</sup>	
	1,517-pin	40 x 40 mm							736			736			736		736	
	1,932-pin	45 x 45 mm																904

<sup>1</sup> All data is preliminary

<sup>2</sup> Hybrid package (flip chip) FBGA

## Stratix IV E FPGAs (0.9V) High density, high performance, low power <sup>1</sup>

## Stratix III FPGAs Balanced logic, memory, DSP

**480** Number indicates available user I/O pins.

Vertical migration (same V<sub>CC</sub>, GND, ISP, and input pins).

All Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

	Pin count	Body size	EP4SE110	EP4SE230	EP4SE290	EP4SE360	EP4SE530	EP4SE680	EP3SL200	EP3SE260	EP3SL340
FBGA (F)	780-pin	29 x 29 mm	480	480	480 <sup>2</sup>	480 <sup>2</sup>					
	1,152-pin	35 x 35 mm			736	736	736 <sup>2</sup>	736 <sup>2</sup>			
	1,517-pin	40 x 40 mm			864	864	960	960	960	960	960
	1,760-pin	43 x 43 mm					960	1,104			1,104

<sup>1</sup> All data is preliminary

<sup>2</sup> Hybrid package (flip chip) FBGA

## Stratix IV transceiver protocol support (GX only)

Protocol	Data rate	Protocol	Data rate
PCI Express Gen1, Gen2	2.5, 5.0	DDR-XAUI	6.25
PCI Express Cable	2.5	SFI5.1	2.488 - 3.125
SAS	1.5, 3.0, 6.0	SONET OC-3/OC-12/OC-48	0.155, 0.622, 2.488
SATA	1.5, 3.0	Ethernet-XAUI	4 x 3.125
SDI SD/HD	0.27/1.485	Gigabit Ethernet	1.25
3G SDI	2.97	CEI-6G/SR/LR	6.375/4.976 - 6.375/4.976 - 6.375
ASI	0.27	HiGig+	3.75
CPRI	0.6144, 1.2288, 2.4576, 3.072	HiGig2	4.0625
OBSAI	0.768, 1.536, 3.072	Interlaken	3.125 - 6.375
Serial RapidIO®	1.25, 2.5, 3.125	Fibre Channel	1.0625, 2.125, 4.25, 8.5
GPON	1.244 uplink, 2.488 downlink	HyperTransport™ 3.0	0.4, 2.4, 2.8, 3.2
SPAUI	3.2, 6.4	SerialLite II	0.6 - 6.375

## Stratix IV GX FPGAs (0.9V) up to 8.5-Gbps transceivers <sup>1</sup>

		EP4SGX70D	EP4SGX110D	EP4SGX110F	EP4SGX230D	EP4SGX230F	EP4SGX230H	EP4SGX230K	EP4SGX290F
Density and speed	Equivalent LEs	72,600	105,600	105,600	228,000	228,000	228,000	228,000	291,200
	ALMs	29,040	42,240	42,240	91,200	91,200	91,200	91,200	116,480
	Registers <sup>2</sup>	58,080	84,480	84,480	182,400	182,400	182,400	182,400	232,960
	M9K memory blocks	462	660	660	1,235	1,235	1,235	1,235	936
	M144K memory blocks	16	16	16	22	22	22	22	36
	Embedded memory (Mbits)	6.3	8.1	8.1	13.9	13.9	13.9	13.9	13.3
	MLAB memory (Kbits)	908	1,320	1,320	2,850	2,850	2,850	2,850	3,640
	Max. 18-bit x 18-bit multipliers	384	512	512	1,288	1,288	1,288	1,288	832
	Speed grades (fastest to slowest)	-3, -4	-3, -4	-3, -4	-3, -4	-3, -4	-2, -3, -4	-2, -3, -4	-3, -4
Architectural features	Embedded processor available	Nios® II processor							
	Global clock networks	16	16	16	16	16	16	16	16
	Regional clock networks	64	64	64	64	64	64	64	88
	Periphery clock networks	56	56	56	88	88	88	88	88
	PLLs/unique outputs	3/27	3/27	4/34	3/27	6/54	6/54	8/68	6/54
	Design security	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy® series device support	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy companion device	HC4GX1	HC4GX2		HC4GX3			HC4GX4	
I/O features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3 <sup>3</sup>							
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)							
	Medium performance LVDS channels	128	128	128	128	192	192	192	192
	Number of LVDS channels, 1.6 Gbps (receive/transmit)	28/28	28/28	28/28	28/28	44/44	44/44	88/88	44/44
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓	✓
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) data rate range	600 Mbps - 8.5 Gbps with PCS + PMA							
	Transceiver (SERDES) channels	8	8	16	8	16	16	24	16
	Transceiver (SERDES) data rate range	600 Mbps - 3.2 Gbps with PMA only							
	Transceiver (SERDES) channels <sup>4</sup>	–	–	–	–	–	8	12	–
PCI Express hard IP blocks	1	1	2	1	2	2	2	2	
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II SDR							
Configuration file sizes	Configuration file size (Mbits)	52	52	52	102	102	102	102	140

<sup>1</sup> All data is preliminary

<sup>2</sup> This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

<sup>3</sup> 3.3V compliant, requires a 3.0V power supply

<sup>4</sup> These are additional transceivers, total transceiver count is sum of 8.5-Gbps transceivers plus 3.2-Gbps transceivers.

**Stratix IV GX FPGAs (0.9V)  
up to 8.5-Gbps transceivers <sup>1</sup>**

		EP4SGX290H	EP4SGX290K	EP4SGX360F	EP4SGX360H	EP4SGX360K	EP4SGX530H	EP4SGX530K	EP4SGX530N
<b>Density and speed</b>	Equivalent LEs	291,200	291,200	353,600	353,600	353,600	531,200	531,200	531,200
	ALMs	116,480	116,480	141,440	141,440	141,440	212,480	212,480	212,480
	Registers <sup>2</sup>	232,960	232,960	282,880	282,880	282,880	424,960	424,960	424,960
	M9K memory blocks	936	936	1,248	1,248	1,248	1,280	1,280	1,280
	M144K memory blocks	36	36	48	48	48	64	64	64
	Embedded memory (Mbits)	13.3	13.3	17.7	17.7	17.7	20.3	20.3	20.3
	MLAB memory (Kbits)	3,640	3,640	4,420	4,420	4,420	6,640	6,640	6,640
	Max 18-bit x 18-bit multipliers	832	832	1,040	1,040	1,040	1,024	1,024	1,024
	Speed grades (fastest to slowest)	-2, -3, -4	-2, -3, -4	-3, -4	-2, -3, -4	-2, -3, -4	-3, -4	-3, -4	-3, -4
<b>Architectural features</b>	Embedded processor available	Nios II processor							
	Global clock networks	16	16	16	16	16	16	16	16
	Regional clock networks	88	88	88	88	88	88	88	88
	Periphery clock networks	88	88	88	88	88	112	112	112
	PLLs/unique outputs	6/54	12/96	6/54	6/54	12/96	6/54	8/68	12/96
	Design security	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy series device support	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy companion device	HC4GX4		HC4GX5			HC4GX6		
<b>I/O features</b>	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3 <sup>3</sup>							
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)							
	Medium performance LVDS channels	192	192	192	192	192	192	192	256
	Number of LVDS channels, 1.6 Gbps (receive/transmit)	44/44	88/88	44/44	44/44	88/88	44/44	88/88	98/98
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓	✓
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) data rate range	600 Mbps - 8.5 Gbps with PCS + PMA							
	Transceiver (SERDES) channels	16	24	16	16	24	16	24	32
	Transceiver (SERDES) data rate range	600 Mbps - 3.2 Gbps with PMA only							
	Transceiver (SERDES) channels <sup>4</sup>	8	12	–	8	12	8	12	16
PCI Express hard IP blocks	2	2	2	2	2	4	4	4	
<b>External memory interfaces</b>	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II SDR							
<b>Configuration file sizes</b>	Configuration file size (Mbits)	140	140	140	140	140	189	189	189

<sup>1</sup> All data is preliminary<sup>2</sup> This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.<sup>3</sup> 3.3V compliant, requires a 3.0V power supply.<sup>4</sup> These are additional transceivers, total transceiver count is sum of 8.5-Gbps transceivers plus 3.2-Gbps transceivers

# Stratix IV FPGA family features

## Stratix IV E FPGAs (0.9V) High density, high performance, low power <sup>1</sup>

		EP4SE110	EP4SE230	EP4SE290	EP4SE360	EP4SE530	EP4SE680
Density and speed	Equivalent LEs	105,600	228,000	291,200	353,600	531,200	681,100
	ALMs	42,240	91,200	116,480	141,440	212,480	272,440
	Registers <sup>2</sup>	84,480	182,400	232,960	282,880	424,960	544,880
	M9K memory blocks	660	1,235	936	1,248	1,280	1,529
	M144K memory blocks	16	22	36	48	64	64
	Embedded memory (Mbits)	8.1	13.9	13.3	17.7	20.3	22.4
	MLAB memory (Kbits)	1,320	2,850	3,640	4,420	6,640	8,514
	Max 18-bit x 18-bit multipliers	512	1,288	832	1,040	1,024	1,360
	Speed grades (fastest to slowest)	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-3, -4	-3, -4
Architectural features	Embedded processor available	Nios II processor					
	Global clock networks	16	16	16	16	16	16
	Regional clock networks	88	88	88	88	88	88
	Periphery clock networks	56	88	88	88	112	112
	PLLs/unique outputs	6/54	12/96	6/54	6/54	12/96	6/54
	Design security	✓	✓	✓	✓	✓	✓
	HardCopy series device support	✓	✓	✓	✓	✓	✓
	HardCopy companion device	HC4GX1	HC4GX2	HC44	HC4GX3	HC46	HC47
I/O features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3 <sup>3</sup>					
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)					
	Medium performance LVDS channels	128	128	256	256	256	288
	Number of LVDS channels, 1.6 Gbps (receive/transmit)	56/56	56/56	88/88	88/88	112/112	132/132
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓
	Series and differential on-chip termination	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RDRAM II SDR					
Configuration file sizes	Configuration file size (Mbits)	52	102	140	140	189	230

<sup>1</sup> All data is preliminary

<sup>2</sup> This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

<sup>3</sup> 3.3V compliant, requires a 3.0V power supply