

| | | Stratix II (1.2 V) High Density, High Performance | | | | | | Stratix II GX (1.2 V) 6.375-Gbps Transceivers | | | | | | | |
|-------------------------------|--|---|-------------|------------|------------|------------|------------|--|------------|------------|------------|------------|------------|------------|------------|
| | | EP2S15 | EP2S30 | EP2S60 | EP2S90 | EP2S130 | EP2S180 | EP2SGX30C | EP2SGX30D | EP2SGX60C | EP2SGX60D | EP2SGX60E | EP2SGX90E | EP2SGX90F | EP2SGX130G |
| Density & Speed | Equivalent Logic Elements | 15,600 | 33,880 | 60,440 | 90,960 | 132,540 | 179,400 | 33,880 | 33,880 | 60,440 | 60,440 | 60,440 | 90,960 | 90,960 | 132,540 |
| | Adaptive Logic Modules | 6,240 | 13,552 | 24,176 | 36,384 | 53,016 | 71,760 | 13,552 | 13,552 | 24,176 | 24,176 | 24,176 | 36,384 | 36,384 | 53,016 |
| | Adaptive Look-Up Tables (ALUTs) | 12,480 | 27,104 | 48,352 | 72,768 | 106,032 | 143,520 | 27,104 | 27,104 | 48,352 | 48,352 | 48,352 | 72,768 | 72,768 | 106,032 |
| | Total RAM Bits (K) ¹ | 419 | 1,369 | 2,544 | 4,520 | 6,747 | 9,383 | 1,369 | 1,369 | 2,544 | 2,544 | 2,544 | 4,520 | 4,520 | 6,747 |
| | M512 RAM Blocks (512 Bits + 64 Parity Bits) | 104 | 202 | 329 | 488 | 699 | 930 | 202 | 202 | 329 | 329 | 329 | 488 | 488 | 699 |
| | M4K RAM Blocks (4 Kbits + 512 Parity Bits) ² | 78 | 144 | 255 | 408 | 609 | 768 | 144 | 144 | 255 | 255 | 255 | 408 | 408 | 609 |
| | M-RAM Blocks (512 Kbits + 65,536 Parity Bits) ² | 0 | 1 | 2 | 4 | 6 | 9 | 1 | 1 | 2 | 2 | 2 | 4 | 4 | 6 |
| | Speed Grades (Fastest to Slowest) | -3, -4, -5 | --3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 | -3, -4, -5 |
| Architectural Features | Embedded Processor Available | Nios® II | | | | | | Nios II | | | | | | | |
| | DSP Blocks | 12 | 16 | 36 | 48 | 63 | 96 | 16 | 16 | 36 | 36 | 36 | 48 | 48 | 63 |
| | 18-Bit x 18-Bit/9-Bit x 9-Bit Embedded Multipliers | 48/96 | 64/128 | 144/288 | 192/384 | 252/504 | 384/768 | 64/128 | 64/128 | 144/288 | 144/288 | 144/288 | 19/384 | 19/384 | 252/504 |
| | I/O Registers per I/O Element | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| | True Dual-Port RAM | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Global & Regional Clock Networks | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 48 |
| | PLLs/Unique Outputs | 6/28 | 6/28 | 12/56 | 12/56 | 12/56 | 12/56 | 4/18 | 4/18 | 8/36 | 8/36 | 8/36 | 8/36 | 8/36 | 8/36 |
| | Design Security | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| HardCopy® II Device Support | – | ✓ | ✓ | ✓ | ✓ | ✓ | – | – | – | – | – | – | – | – | |
| I/O Features | I/O Voltage Levels Supported (V) | 1.5, 1.8, 2.5, 3.3 | | | | | | 1.5, 1.8, 2.5, 3.3 | | | | | | | |
| | I/O Standards Supported | LVDS, LVPECL, HyperTransport™, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I & II), SSTL-2 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, PCI-X 1.0, LVTTL, LVCMOS | | | | | | | | | | | | | |
| | True-LVDS™ Maximum Data Rate (Mbps) | 125–1,000 | | | | | | 125–1,000 | | | | | | | |
| | True-LVDS Channels (Receive/Transmit) | 38/38 | 58/58 | 80/84 | 114/118 | 152/156 | 152/156 | 31/29 | 31/29 | 31/29 | 31/29 | 42/42 | 47/45 | 59/59 | 73/71 |
| | Embedded DPA Circuitry | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Series & Differential On-Chip Termination | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Programmable Drive Strength | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Transceiver (SERDES) Data Rate Range | – | – | – | – | – | – | 622 Mbps–6.375 Gbps | | | | | | | |
| Transceiver (SERDES) Channels | – | – | – | – | – | – | 4 | 8 | 4 | 8 | 12 | 12 | 16 | 20 | |
| External Memory Interfaces | Memory Devices Supported | QDRII, DDR2, RLD RAM II, DDR, SDR | | | | | | QDRII, DDR2, RLD RAM II, DDR, SDR | | | | | | | |
| | MegaCore® Controller With Clear-Text Datapath | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | System Timing Analysis | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Board Layout Guidelines | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

¹ K = 1,000
² Kbits = 1,024 bits

Stratix FPGA Series Features (Continued)



| | | Stratix (1.5 V) High Density, High Performance | | | | | | Stratix GX (1.5 V) 3.1875-Gbps Transceivers | | | | | | | |
|--------------------------------------|--|---|------------|------------|------------|------------|------------|--|------------|------------|------------|------------|------------|------------|------------|
| | | EP1S10 | EP1S20 | EP1S25 | EP1S30 | EP1S40 | EP1S60 | EP1S80 | EP1SGX10C | EP1SGX10D | EP1SGX25C | EP1SGX25D | EP1SGX25F | EP1SGX40D | EP1SGX40G |
| Density & Speed | Logic Elements (LEs) | 10,570 | 18,460 | 25,660 | 32,470 | 41,250 | 57,120 | 79,040 | 10,570 | 10,570 | 25,660 | 25,660 | 25,660 | 41,250 | 41,250 |
| | Total RAM Bits (K) ¹ | 920 | 1,669 | 1,944 | 3,317 | 3,423 | 5,215 | 7,427 | 920 | 920 | 1,944 | 1,944 | 1,944 | 3,423 | 3,423 |
| | M512 RAM Blocks (512 Bits + 64 Parity Bits) | 94 | 194 | 224 | 295 | 384 | 574 | 767 | 94 | 94 | 224 | 224 | 224 | 384 | 384 |
| | M4K RAM Blocks (4 Kbits + 512 Parity Bits) ² | 60 | 82 | 138 | 171 | 183 | 292 | 364 | 60 | 60 | 138 | 138 | 138 | 183 | 183 |
| | M-RAM Blocks (512 Kbits + 65,536 Parity Bits) ² | 1 | 2 | 2 | 4 | 4 | 6 | 9 | 1 | 1 | 2 | 2 | 2 | 4 | 4 |
| | Speed Grades (Fastest to Slowest) | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 | -5, -6, -7 |
| Architectural Features | Embedded Processor Available | Nios II | | | | | | Nios II | | | | | | | |
| | DSP Blocks | 6 | 10 | 10 | 12 | 14 | 18 | 22 | 6 | 6 | 10 | 10 | 10 | 14 | 14 |
| | 18-Bit x 18-Bit/9-Bit x 9-Bit Embedded Multipliers | 24/48 | 40/80 | 40/80 | 48/96 | 56/112 | 72/144 | 88/176 | 24/48 | 24/48 | 40/80 | 40/80 | 40/80 | 56/112 | 56/112 |
| | I/O Registers per I/O Element | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| | True Dual-Port RAM | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Global & Regional Clock Networks | 36 | 36 | 36 | 40 | 40 | 40 | 40 | 36 | 36 | 36 | 36 | 36 | 40 | 40 |
| | PLLs/Unique Outputs | 6/32 | 6/32 | 6/32 | 10/40 | 12/52 | 12/52 | 12/52 | 4/26 | 4/26 | 4/26 | 4/26 | 4/26 | 8/42 | 8/42 |
| HardCopy Device Support | - | - | ✓ | ✓ | ✓ | ✓ | ✓ | - | - | - | - | - | - | - | |
| I/O Features | I/O Voltage Levels Supported (V) | 1.5, 1.8, 2.5, 3.3 | | | | | | 1.5, 1.8, 2.5, 3.3 | | | | | | | |
| | I/O Standards Supported | LVDS, LVPECL, HyperTransport, 3.3-V PCML, Differential SSTL-2, Differential HSTL, SSTL-18 (I & II), SSTL-2 (I & II), SSTL-3 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, Compact-PCI, PCI-X 1.0, AGP (1x & 2x), GTL, GTL+, CTT, LVTTTL, LVCMOS) | | | | | | | | | | | | | |
| | True-LVDS Maximum Data Rate (Mbps) | 840 | | | | | | 1000 | | | | | | | |
| | True-LVDS Channels (Receive/Transmit) | 44/44 | 66/66 | 78/78 | 80/80 | 80/80 | 80/80 | 80/80 | 22/22 | 22/22 | 39/39 | 39/39 | 39/39 | 45/45 | 45/45 |
| | Medium-Speed LVDS Channels | - | - | - | 462 | 462 | 462 | 462 | - | - | - | - | - | - | - |
| | Embedded DPA Circuitry | - | - | - | - | - | - | - | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Series & Differential On-Chip Termination | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Programmable Drive Strength | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Transceiver (SERDES) Data Rate Range | - | - | - | - | - | - | - | 500 Mbps–3.1875 Gbps | | | | | | | |
| Transceiver (SERDES) Channels | - | - | - | - | - | - | - | 4 | 8 | 4 | 8 | 16 | 8 | 20 | |
| External Memory Interfaces | Memory Devices Supported | QDRII, QDR, ZBT, DDR, SDR | | | | | | QDRII, QDR, ZBT, DDR, SDR | | | | | | | |
| | MegaCore Controller With Clear-Text Datapath | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | |
| | System Timing Analysis | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | |
| | Board Layout Guidelines | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | |

¹ K = 1,000

² Kbits = 1,024 bits

HardCopy Structured ASIC Series Features and Package & I/O Matrix

Altera's HardCopy® structured ASICs offer a seamless migration from Stratix® and Stratix II FPGAs to a low-cost, pin-compatible, functionally equivalent device.

951 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial and industrial temperatures and lead-free packages.

| | HardCopy II (1.2 V) Structured ASIC | | | | | HardCopy Stratix (1.5 V) Structured ASIC | | | | | |
|-------------------------------|--|---|----------------------------|-----------------------------|------------------------------|---|---------------------------|-----------|-----------|-----------|-----------|
| | HC210W | HC210 | HC220 | HC230 | HC240 | HC1S25 | HC1S30 | HC1S40 | HC1S60 | HC1S80 | |
| Density & Speed | ASIC Gates | 1,000,000 | 1,000,000 | 1,600,000 | 2,200,000 | 2,200,000 | – | – | – | – | – |
| | Additional Gates for DSP Blocks | 0 | 0 | 300,000 | 700,000 | 1,400,000 | – | – | – | – | – |
| | Logic Elements | – | – | – | – | – | 25,660 | 32,470 | 41,250 | 57,120 | 79,040 |
| | Total RAM Bits | 875,520 | 875,520 | 3,059,712 | 6,368,256 | 8,847,360 | 1,944,576 | 2,137,536 | 2,244,096 | 5,215,104 | 5,658,048 |
| | M512 RAM Blocks (512 Bits + 64 Parity Bits) | – | – | – | – | – | 224 | 295 | 384 | 574 | 767 |
| | M4K RAM Blocks (4 Kbits + 512 Parity Bits) ¹ | 190 | 190 | 408 | 614 | 768 | 138 | 171 | 183 | 292 | 364 |
| | M-RAM Blocks (512 Kbits + 65,536 Parity Bits) ¹ | 0 | 0 | 2 | 6 | 9 | 2 | 2 | 2 | 6 | 6 |
| | Speed Grades (Fastest to Slowest) | – | – | – | – | – | – | – | – | – | – |
| Architectural Features | Embedded Processor Available | Nios II | | | | | Nios II | | | | |
| | DSP Blocks | Implemented in HCell Macros | | | | | 10 | 12 | 14 | 18 | 22 |
| | 18-Bit x 18-Bit/9-Bit x 9-Bit Embedded Multipliers | Implemented in HCell Macros | | | | | 40/80 | 48/96 | 56/112 | 72/144 | 88/176 |
| | I/O Registers per I/O Element | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| | True Dual-Port RAM | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Global & Regional Clock Networks | 16/32 | 16/32 | 16/32 | 16/32 | 16/32 | 36 | 40 | 40 | 40 | 40 |
| | PLLs | 4 | 4 | 4 | 8 | 12 | 6 | 6 | 6 | 12 | 12 |
| I/O Features | I/O Voltage Levels Supported (V) | 1.5, 1.8, 2.5, 3.3 | | | | | 1.5, 1.8, 2.5, 3.3 | | | | |
| | I/O Standards Supported | LVDS, LVPECL, HyperTransport, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I & II), SSTL-2 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, PCI-X 1.0, LVTTTL, LVCMOS | | | | | | | | | |
| | External Memory Device Interfaces | QDRII, DDR2, RDRAM II, DDR, SDR | | | | | QDRII, QDR, ZBT, DDR, SDR | | | | |
| | True-LVDS Maximum Data Rate (Mbps) | 125–1,000 | | | | | 840 | | | | |
| | True-LVDS Channels (Receive/Transmit) | 19/21 | 19/21 | 29/31 | 42/42 | 118/118 | 78/78 | 80/80 | 80/80 | 80/80 | 80/80 |
| | Medium-Speed LVDS Data Rate (Mbps) (Receive/Transmit) | – | – | – | – | – | – | 2/2 | 10/10 | 36/36 | 46/72 |
| | Series & Differential On-Chip Termination | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | FPGA Prototype Options | EP2S30 EP2S60 EP2S90 | EP2S30 EP2S60 EP2S90 | EP2S60 EP2S90 EP2S130 | EP2S90 EP2S130 EP2S180 | EP2S180 | EP1S25 | EP1S30 | EP1S40 | EP1S60 | EP1S80 |
| FineLine BGA (F) | 484-Pin FBGA (Wirebond) | 308 | | | | | | | | | |
| | 484-Pin FBGA (FlipChip) | | 334 | | | | | | | | |
| | 672-Pin FBGA (Wirebond) | | | | | 473 | | | | | |
| | 672-Pin FBGA (FlipChip) | | | 492 | | | | | | | |
| | 780-Pin FBGA | | | 494 | | | 597 | 615 | | | |
| | 1,020-Pin FBGA | | | | 698 | 742 | | | | 773 | 773 |
| 1,508-Pin FBGA | | | | | 951 | | | | | | |

¹ Kbits = 1,024 bits