

Monthly Spotlight

[Download a Free Evaluation of the Video & Image Processing Suite](#)

Altera's Video and Image Processing (VIP) Suite is a collection of IP cores that jump-start your designs for video surveillance, broadcast, video conferencing, and other applications. These IP cores can be directly instantiated within SOPC Builder. New features include:

- A motion adaptive algorithm for improved progressive video quality and double or triple buffering in external RAM. This feature of the Deinterlacer IP core reduces throughput problems.
- Run-time control for resolution and image size, which are included with the Alpha Blending Mixer and Chroma Resampler IP cores.

[Download the VIP User Guide](#) (PDF) to learn more about the updated VIP Suite!

FPGAs, CPLDs, and Structured ASICs

[Make Sure Your FPGA Has the Memory to Match Its Logic](#)

Video applications often run out of memory before they run out of logic. Stratix® III FPGAs can protect you from that issue with their additional and configurable memory. With Stratix III FPGAs, you can fit your design in a smaller, more cost-effective device, and get optimum signal processing performance. Learn more about Stratix III FPGA advantages for video processing applications.

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Intellectual Property & Solutions

[Reference Design: Video & Image Processing Up Conversion](#)

After downloading the VIP Suite, you'll want to check out Altera's VIP Up-Conversion reference design. This reference design shows you how to build your video processing data path within DSP Builder, and how to build control and memory interfaces within SOPC Builder. It's a great way to start developing your video data path to perform deinterlacing, chroma resampling, color space conversion, and scaling.

[Design Example: Polyphase Modulation with Aliasing for Data Up-Conversion](#)

Download this DSP Builder design example to learn how to build a polyphase up-converter using Altera's FIR Compiler, NCO, and CIC IP cores. Conventional digital up converters modulate signals on carrier frequencies that are limited by the Nyquist theory. This design example avoids those limits by generating a carrier frequency that exceeds the NCO



sampling frequency, easing requirements for analog modulation.

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Training

[Implementing DSP Designs in FPGAs](#)

Chelmsford, MA and Schaumburg, IL (March 2008) Sign up for this instructor-lead class, where you'll learn the FPGA design flow for implementing your DSP designs. You will analyze, design, and implement DSP systems using the IP cores and DSP Builder blockset in The MathWorks' Matlab/Simulink. Everyone who attends this instructor-led course will get a 20% discount on a DSP development kit!

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Literature

[Application Note: 1536-Point FFT for 3GPP Long Term Evolution \(PDF\)](#)

A 3GPP LTE system must support variable transmission bandwidths from 1.25 to 20 MHz, and each bandwidth has a unique corresponding fast Fourier transform size ranging from 128 to 2,048 points. Altera's parameterizable FFT IP core supports 2ⁿ sizes-from 32 to 16k points-with radix-2 and radix-4 engines satisfying the majority of the required 3GPP LTE transform sizes. But what about the 15 MHz transmission bandwidth, which requires a 1,536 point size transform? Download this application note to see how an FFT IP core constructs a transform length of 1,536 points.

[White Paper: Designing High-Performance DSP Hardware Using Catapult C Synthesis and the Altera Accelerated Libraries \(PDF\)](#)

Struggling to manually convert your C-based algorithm into FPGA-optimized RTL? Learn about an exciting new design flow that streamlines potentially time-consuming RTL creation and yields better quality of results.

[White Paper: DSP-FPGA System Partitioning for MIMO-OFDMA Wireless Basestations \(PDF\)](#)

Download this white paper for a flexible, high-performance, and obsolescence-proof cost-reduction partition for a wireless basestation design. You'll discover Stratix series FPGA, HardCopy structured ASIC, and DSP system partitioning ideas that will help you meet your time-to-market goals while contributing to future market success.

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Altera in the News

[Mentor Catapult optimizes algorithms and flow for Altera DSP-centric FPGAs, EDN](#)

Read about how you can get the most performance out of Cyclone and Stratix FPGA DSP blocks.

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