

### Quarterly Spotlight

#### [Download Video Processing Reference Design for Up Conversion](#)

Altera's updated Video Processing Reference Design demonstrates up conversion from an SD video stream in NTSC format and picture-in-picture (PiP) mixing with a background layer. The video stream is output in HD (1024x768) over a digital video interface.

This reference design uses the latest version of IP cores from Altera's Video & Image Processing (VIP) Suite, including the scaler (polyphase mode), deinterlacer (motion adaptive mode), and alpha blending mixer cores.

[Download the reference design today](#) to get started on your next video processing project!



### From Altera's DSP Desk

#### [Buy Bitec's Cyclone III Video Development Kit & Get a 1080p PiP Reference Design](#)

Check out Bitec's complete video development kit that comes with a set of daughter cards for interfacing with various video sources and displays, a reference design to demonstrate 1080p PiP video processing, and more.

The kit's 1080p PiP reference design combines a single composite/s-video channel with a full HD 1080p video stream to generate a 1080p PiP output video stream. The resulting image stream is the combination of both input video signals.

The Cyclone III Video Development Kit is [available for immediate purchase from Bitec](#), so get yours today!

#### [Download Version 8.0 of the VIP Suite](#)

The VIP Suite v8.0 features five new IP cores, including the Clocked Video Input/Output core that can be used to convert video signals from industry-standard BT-656 format to Avalon<sup>®</sup>-ST video format. Also included in v8.0 is the Frame Buffer core, which provides an easy interface with external video frame buffer memory, including a provision for frame dropping and repeat.

The VIP Suite now includes 14 cores that you can use to develop a complete video application, or you can use in conjunction with your own custom video IP. [Download v8.0 of the VIP Suite today!](#)

#### [Timing-Driven Simulink FPGA Synthesis, DSP DesignLine](#)

Simulink is popular among DSP designers, and FPGA vendors have taken note. These vendors have created blockset libraries that enable Simulink designs to be synthesized for FPGA implementation. While these blocksets



are useful, DSP designers have lacked an automated method to transform the Simulink design to a timing-optimized FPGA implementation.

The latest system design tools, including Altera's DSP Builder, offer timing-driven Simulink synthesis that enables automatic generation of timing-optimized HDL. This means that the HDL generated by DSP Builder now meets the timing constraints set within Simulink.

See the design productivity advantages of using these tools, along with examples, [in this article](#).

## **New DSP Resources**

### **[Check out the Altera DSP Designer Curriculum](#)**

Are you new to DSP design with FPGAs, or ready to refresh your memory? In this multi-course curriculum, you'll learn how to start and optimize your DSP design. With both instructor-led and on-line training, you'll find the courses that fit your needs and help you master the complexities of developing DSP applications.

Find all of Altera's DSP tools for engineers at [www.altera.com/dsp](http://www.altera.com/dsp).

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