

The Q4 issue of Altera's Embedded e-Newsletter brings you the latest news, software tools, seminars and technical articles on Altera embedded processing products.

Quarterly Spotlight

[Design Example: C2H Compiler Accelerates FIR Filter](#)

Find out how the Nios II C2H Compiler can be used to create a system that computes a symmetrical FIR filter algorithm 52 times faster than a software only-implementation. [Download Now.](#)

Embedded Software & Tools

[Looking for Increased SDRAM Memory Performance?](#)

Boost your memory performance more than 6 times with Microtronix's new SOPC Builder-ready core. Optimized for Stratix® and Cyclone® PLDs, this high-performance multi-port memory-controller IP core provides a complete, easy-to-use solution that interfaces with SDRAM, DDR, and DDR2 memory devices.

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Literature, Tutorials & Technical Resources

[Design Example: High-Performance Multiprocessor Nios II Design](#)

With SOPC Builder, creating multiprocessor systems is easy! This high-performance multiprocessor design example has three Nios® II CPUs and a simple software application that shows how to use the mutex component and shared on-chip memories for interprocessor communication. [Download Now.](#)

[Design Example: Test Nios II System Connection to RAM & Flash](#)

In addition to demonstrating how to use the Nios processor to test the operation of external RAM and flash, this design example demonstrates the use of the direct-memory access-controller peripheral and the Nios II flash-programming application program interface. [Download Now.](#)

[Design Example: Read-Only Zip File System](#)

Did you know Altera offers a simple, read-only file system with the Nios II processor? This design example demonstrates Altera's read-only zip filing system and GNU debugger host filing system. [Download Now.](#)

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Your 2 Cents

Tell us what you think!

Question:

Have you adopted Electronic System Level (ESL) design?

[Take the poll and view results!](#)



[Design Example: Off-Chip Memory PLL Tuning Example](#)

Clocking memory devices incorrectly can cause major headaches. This design example demonstrates how you can vastly improve the reliability of your memory devices. [Download Now](#).

[Tutorial: Boosting Software Performance with Nios II Tightly Coupled Memory](#)

Make your software code fly! Tightly coupled memories provide fixed, low-latency access to on-chip memory resources that are indispensable for performance-critical applications. Find out how to implement these special memories and use them to accelerate your software.

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Events, Net Seminars & Training

Upcoming Events

[Embedded World 2007 Exhibition & Conference](#)

Nuremberg, Germany, Feb. 13-15 2007

Upcoming Training Courses

[Accelerating Software Using the Nios II C2H Compiler](#)

San Jose, CA, Jan. 31 2007

[Designing with the Nios II Processor and SOPC Builder](#)

San Jose, CA, Feb. 14 2007

[Developing Software for the Nios II Processor](#)

San Jose, CA, Feb. 15 - 16 2007

Online, Anytime

- [Nios II C2H Fundamentals](#)
- [Using SOPC Builder](#)
- [System-on-a-Programmable-Chip Design Using the Nios II Embedded Processor](#)

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From the Nios Community

[Avalon UART with FIFO](#)

Nios Forum user, "longshot," posts an enhanced version of the standard Avalon UART to add FIFO and hardware CTS features. Download the component from the Nios Forum.

[C2H Optimization Example](#)

This example takes you through the process of accelerating C code with the Nios II C2H compiler and optimizing results. It's posted on the new Nios Community Wiki.

[Calling Floating-Point Custom Instructions](#)

Accelerate a floating-point operation with your own custom instruction? Learn how to make GCC call your floating-point instruction instead of the standard math library software function.

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