

Welcome to the October issue of the *Inside Edge*. This monthly e-Newsletter gives you the latest news about Altera's products and solutions.

Monthly Spotlight

[Register Now! SOPC World/PLD World 2004 Technical Seminars](#) **Free**

Experts will conduct detailed technical sessions on embedded processing, DSP, high-speed design, and direct memory access. Key sponsors include Aldec, Mentor Graphics, Infineon, The MathWorks, Micron, Tektronix. Plus: Live demos (Altera and partners) & Altera's technology roadmap

FPGAs, CPLDs & Structured ASICs

[Place Your Orders Today for Stratix II EP2S30 & EP2S130 FPGAs](#)

Contact your local Altera sales representative now to order Stratix® II EP2S30 and EP2S130 devices for shipment in Q4 of 2004. The EP2S30 FPGA has 33,880 equivalent logic elements (LEs), 1.3 Mbits of memory, and 16 DSP blocks. The EP2S130 FPGA has 132,540 equivalent LEs, 6.4 Mbits of memory, and 63 DSP blocks.

[Learn How to Interface Cyclone II FPGAs With DDR & DDR2 SDRAM](#)

Cyclone™ II FPGAs are designed to communicate with the latest SDRAM and SRAM memory devices through a dedicated interface that ensures fast and reliable data transfer up to 333 Mbps for DDR2 and 667 Mbps for QDR II. Learn more about interfacing DDR and DDR2 SDRAM with Cyclone II FPGAs.

[Pirelli Adopts Stratix GX FPGAs for Next-Generation ROF 3G Solution](#)

Pirelli selected Stratix GX FPGAs for their next generation radio-over fiber (ROF) 3G network solution, which enables the transmission of radio signals directly over optical fiber. Pirelli chose Stratix GX devices for their combination of high-speed transceivers and industry-leading performance.

Software, Intellectual Property & Development Kits

[Buy the Full-Featured MAX II Development Kit Online for Only \\$150](#)

Evaluate the new MAX® II features and begin prototyping your design now with the low-cost MAX II Development Kit. The board features the EPM1270 device and comes with Quartus® II Web Edition software, a ByteBlaster™ II programming cable, and several reference designs.

[Download SerialLite MegaCore IP for Stratix GX FPGAs](#) **Free Trial**

Significantly reduce time and risk for your serial transceiver design by using the SerialLite MegaCore® function. Supporting up to 16 lanes and data rates up to 3.125 Gbps performance, SerialLite is the lightest, most configurable serial I/O protocol available today.

[DDR2 & QDR II Controllers Now Available in IP Base Suite](#)

Altera's DDR2 and QDR II Controllers are now available at no charge to active IP Base Suite customers. Supporting rates up to 533 Mbps, Altera's memory controller MegaCore functions automatically perform timing analysis to simplify your design.

[Download Constraint File Update for PCI Compiler 3.2.0](#)

PCI Compiler 3.2.0 users should download and use the revision 3.2.1 constraint file update. A readme file included with the update details all changes and improvements. No other

In This Issue:

[FPGAs, CPLDs & Structured ASICs](#)

[Software, Intellectual Property & Development Kits](#)

[Events, Training & Net Seminars](#)

[Recent Articles about Altera](#)

[Subscribe to Inside Edge](#)



components of the PCI Compiler 3.2.0 package need to be updated.

Events, Training & Net Seminars

[Register Now: Three-Part Code:DSP Net Seminar Series](#) **Free**

Beginning on October 6, Altera will host a three-part DSP net seminar series on video and image processing that features leading-edge product demonstrations and experts from Barco Silex, The MathWorks, and Altera. Enter to win a \$500 Amazon.com gift certificate and other great prizes.

[View Now: Enhance Your FPGA Design Flow with Scripting](#) **Free**

The "Enhance Your FPGA Design Flow with Command-Line & Tcl Scripting" net seminar highlights how designers can use command line executables, makefiles, and industry-standard tool command language (Tcl) with Altera's Quartus II software.

[See Altera at the Mentor Graphics European Solution Expo Seminars](#)

Altera will be participating in the Mentor Graphics European Solution Expo events in Sweden, Finland, Germany, and the UK during October. The events will highlight the latest innovations in both HDL and PCB design. Visit the Altera booth, where we will be demonstrating our latest technology.

Recent Articles about Altera

[Altera Releases Development Kits for FPGA, CPLD families, CommsDesign](#)

Customers can now get their hands on two of Altera's newest devices with the release of development kits for Stratix II and MAX II devices. CommsDesign gives readers a taste of what's in both kits.

[Low-Cost Programmable Logic Drives Innovation in Consumer Electronics, EE Times](#)

Find out why low-cost FPGAs are going to make life easier for consumer electronic developers.

[Altera's Stratix GX FPGAs Prove Themselves, EE Product Center](#)

Read how the interoperability of Mindspeed's backplane solutions and Altera's FPGAs will provide customers with ease-of-use, lower costs, and design flexibility in a wide variety of networking equipment.

[Back to top ▲](#)



[Subscribe](#) to additional Altera email updates and e-Newsletters, or view/edit all of your Altera email subscriptions.

Copyright© 1995-2004 Altera Corporation, 101 Innovation Drive, San Jose, California 95134, USA