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Altera's Monthly e-Newsletter

Welcome to the June issue of the *Inside Edge*. This monthly e-Newsletter gives you the latest news about Altera's products and solutions.

## Monthly Spotlight

### [Altera Expands E-Store--FPGAs/CPLDs Now Available For Purchase](#)

Altera is expanding the e-store on [www.altera.com](http://www.altera.com) to include FPGAs, CPLDs, and configuration PROMs. Small quantities of Stratix® II--the biggest and fastest FPGAs, Cyclone™ II--the lowest cost FPGAs ever, and MAX® II--the lowest cost CPLD ever, are available. Purchase your devices online today.

## FPGAs, CPLDs & Structured ASICs

### [Get On-Time Delivery of Altera's Highest Density FPGAs](#)

Patented redundancy technology enables Altera to deliver the largest two members of the Stratix II family, the EP2S130 and EP2S180, in volume, in production, in industrial temperature grade, in lead-free packages, and now in higher-performance "-3" speed grade. Start designing today!

### [Reduce Power Consumption by 1/2 Using 90-nm Cyclone II FPGAs](#)

Altera's Cyclone II FPGAs are the lowest power 90-nm devices available today. Cyclone II devices consume 1/2 the dynamic power, 1/2 the static power of competing solutions, and have zero in-rush current. Design for low-power Cyclone II devices today.

## Software, Intellectual Property & Development Kits

### [Download Quartus II Web Edition v5.0](#) **Free**

This release provides programming support for the latest available MAX® II CPLDs and Cyclone II FPGAs. The new Quartus II pin planner feature facilitates the process of planning and creating pin assignments.

### [Download Nios II Embedded Processor v5.0 Evaluation Edition](#) **Free**

Need a royalty-free processor for your FPGA design? Looking for scalable performance, flexible features, and low cost? The Nios® II processors deliver the perfect fit every time. [Download](#) the evaluation tools now.

### [Pre-Order Now! DSP Dev Kit With Industry's Highest Density FPGA](#)

Do you need maximum digital signal processing (DSP) performance? Use the Stratix II Professional Edition DSP Development Kit to design, prototype, and debug DSP computationally intensive applications on the industry's highest density FPGA. The kit will ship in the third quarter of 2005.

June 2005

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## [Learn SOPC Builder Applications--Enter to Win a Development Kit](#)

SOPC Builder can save weeks of development time by freeing you and your team from mundane system integration tasks. Learn about building peripheral expansion systems or DSP co-processors in minutes! Enter to win a development kit with SOPC Builder (US\$995 value).

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## Technology & System Solutions

### [Download High Performance Network Reference Design for Nios II](#) **Free**

Altera, MoreThanIP, and InterNiche have teamed up to provide Nios® II system designers with a high-performance networking solution delivering over 60 Mbits per second via TCP/IP. [Download](#) the white paper and reference design now.

### [FPGA Configuration & Flash Programming is Easy With MAX II CPLDs](#)

Use MAX® II devices to simplify FPGA configuration when storing the programming file in a flash device. Learn how the MAX II parallel flash loader provides an easy way to configure Altera® FPGAs & program flash devices through the JTAG interface. [Download](#) the application note now. **Free**

### [Get Industry-Leading Solutions at the Updated DSP Solutions Center](#)

Visit the recently updated Altera DSP Solutions Center! The new and improved site has comprehensive and up-to-date information for DSP designers. Learn how Altera is delivering premium solutions for video and image processing and high-speed digital communications.

### [Do You Require Both DSP & NPU Capabilities in the Same System?](#)

The Control Plane Bridge Reference Design from Quasar Systems, Inc is a solution to the control plane required when using ADI's TigerSHARC DSP processor and Intel's IXP2350/IXP2325 series of NPU (network processor unit) processors. [Download](#) the reference design now. **Free**

## Events, Training & Net Seminars

### [Last Chance to Register for Altera's Code:DSP Seminar](#) **Free**

#### **Seminars begin June 14 in North America and June 27 in Europe**

Altera's complimentary full-day Code:DSP Video, Image and Signal Processing seminar will show you how to implement the next-generation of FPGA-based system architectures that boost DSP performance and lower overall costs.

### [Register Now: "Easily Implement PCI Express" Net Seminar](#) **Free**

Learn how Altera's programmable, hardware-proven, PCI Express solution can simplify your PCI Express design and minimize design risk. Attend the seminar on Thursday, June 30 for a chance to win a Pinnacle MovieBox Deluxe (US \$200 value).

### [View Now: "Improve Your Productivity in FPGAs" Net Seminar](#) **Free**



Find out how Altera's Quartus II software provides the industry's first incremental compilation feature to dramatically reduce compilation times and improve designer productivity.

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## Support & Literature

### [Read Altera's 2005 News & Views Spring/Summer Issue--Now Online](#)

Read about low-risk HardCopy® II structured ASICs, new features for the Quartus II software version 5.0, building systems with SOPC Builder, contributed articles from Synopsys and Synplicity, and designing smart embedded networking applications for the Nios II processor.

## Altera in the News

### [Selecting the FPGA that Meets Your Signal Integrity Requirements, FPGA Journal](#)

Concerned about signal integrity? Selecting the right FPGA that meets specific signal integrity requirements is critical for individual design success.

### [The DSP Solution Spectrum for Medical Imaging Applications Using FPGAs, DSP-FPGA.com](#)

Learn how medical imaging equipment manufacturers are developing diagnostic instruments based on advanced DSP algorithms and FPGAs.

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