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InsideEdge

Altera's Monthly e-Newsletter

Welcome to the May issue of the *Inside Edge*. This monthly e-Newsletter gives you the latest news about Altera's products and solutions.

May 2005

Monthly Spotlight

[Improve Your Productivity With Quartus II Software v5.0](#)

Quartus® II software version 5.0 introduces the industry's first incremental compilation feature and sets a new standard for high-density FPGA design productivity. Incremental compilation reduces design iteration times by up to 70% and offers unprecedented timing closure productivity gains.

FPGAs, CPLDs & Structured ASICs

[Which Is Truly Bigger-- Stratix II EP2S180 or the Virtex 4VLX200?](#)

Benchmark studies show that Stratix® II devices offer more logic compared to corresponding Virtex-4 devices. The biggest Stratix II device, EP2S180, offers 5% more logic, 50% more memory, 4X more digital signal processing (DSP) resources, and 21% more user I/O pins.

[DSP Benchmark Results: Altera Performs 2X Faster Than Competition](#)

Altera's Stratix II and Cyclone™ II FPGAs are enabling designs that demand premium DSP performance in areas such as video and image processing and high-speed digital communications while delivering the lowest-cost per channel. [Download white paper](#)

Software, Intellectual Property & Development Kits

[Now Shipping: DSP & Nios II Dev Kits, Cyclone II Editions](#)

Shorten your Cyclone II design times with Altera's new development kits for Nios II and DSP designs. The comprehensive platforms allow engineers to design, prototype, and debug a wide range of price-sensitive applications.

[Simplify Your PCI Designs: PCI Compiler Is Now SOPC Builder Ready](#)

With support for Stratix series, Cyclone series, and MAX II devices, PCI Compiler version 4.0.0 provides automatic Avalon™ bridge capability to your favorite Avalon peripherals. [Download evaluation](#) **Free**

[Program Standard Flash Memory Using the Parallel Flash Loader](#)

The Parallel Flash Loader megafunction is now available in the Quartus II software version 5.0. Using the JTAG block (aka JTAG translator) found in every MAX II CPLD, this feature allows you to program and verify non-JTAG compliant flash devices quickly and efficiently.

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Technology & System Solutions

[Request the Video-Over-IP Reference Design Using Cyclone FPGAs](#)

The industry's first FPGA-based video-over internet protocol (IP) reference design enables designers to quickly develop a low-cost system with a Nios II Development Kit, Cyclone Edition. This reference design carries IP traffic at 1 Gbit per second. Request the reference design today!

Events, Training & Net Seminars

[Register for 2005 Code:DSP Video, Image & Signal Processing Seminar](#)

Coming in June to several locations in North America & Europe Free

Altera's complimentary full-day seminar will show you how to implement the next-generation of FPGA-based system architectures that boost DSP performance and lower overall costs.

[Register for "Improve Productivity in FPGA Designs" Net Seminar](#) Free

Find out how Altera's Quartus II software provides the industry's first incremental compilation technology to dramatically reduce compilation times and improve designer productivity. Attend the net seminar for a chance to win a Gateway DVD recorder (US\$250 value).

[Register for "Reduce System Costs With PLDs" Net Seminar](#) Free

Learn how Altera's low-cost programmable logic device (PLD) solutions can reduce system costs and simplify design tasks while speeding time to market and extending product life at a surprisingly competitive price. Attend the net seminar for a chance to win a Gateway DVD recorder (US\$250 value).

[Visit Altera at 2005 Design Automation Conference \(DAC\) June 13 - 18](#)

Altera will showcase its HardCopy® structured ASICs in booth 572 at the 2005 DAC, which takes place in Anaheim, California. DAC is the premier electronic design automation (EDA) and silicon solution event, with over 50 technical sessions on design methodologies and tools.

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Altera in the News

[Choosing the Right Programmable Logic Solution for PCI Express Applications, RTC Magazine](#)

This article discusses the selection criteria that will help designers find the right combination of power, performance, and density to meet multilayer data path challenges.

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