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# ALTERA®

# InsideEdge

Altera's Monthly e-Newsletter

Welcome to the November issue of the *Inside Edge*. This monthly e-Newsletter gives you the latest news about Altera's products and solutions.

## Monthly Spotlight

### [Introducing Stratix II GX-Transceivers With Optimal Signal Integrity](#)

Altera's Stratix® II GX devices combine the performance and density leadership of Stratix II FPGAs with the lowest power, best-in-class embedded transceivers. These devices support such high-speed serial protocols as PCI Express, CEI-6G, Gigabit Ethernet, XAUI, Serial RapidIO™ standards, SONET and more.

## FPGAs, CPLDs & Structured ASICs

### [Experience the Stratix II Performance Advantage With Open Cores](#)

The 25 most popular designs from www.opencores.org demonstrate that Stratix II is, on average, 18% faster than Virtex-4. Run your own benchmark using these publicly available open cores to experience the Stratix II performance advantage.

### [More Tools Now Available for HardCopy II Structured ASICs](#)

With the release of Altera's Quartus® II version 5.1 software you can now design with LogicLock regions and an improved floor plan editor. You can also estimate your design's performance and power requirements before submitting it to Altera for migration to a low-cost HardCopy® II device.

### [Simplify Your Lead-Free Transition With Altera's RoHS Compliant PLDs](#)

Altera maintains one of the most extensive lead-free product offerings in the industry with over 700 devices available today in RoHS compliant packages. Get the complete list of devices including MAX®, MAX II, Stratix, Stratix II, Cyclone™ and Cyclone II.

## Software, Intellectual Property & Development Kits

### [Optimize Power With PowerPlay Enhancements in New Quartus II v5.1](#)

Quartus II software version 5.1 demonstrates leadership in performance and productivity with new automated power optimization features and enhanced incremental compilation technology to support bottom-up team-based design. Learn more about Quartus II version 5.1 today.

### [New Software: DSP Builder v5.1 With New Simulation Capabilities](#)

DSP Builder enables engineers to shorten the DSP design cycle by creating the hardware representation of a DSP design in an algorithm-friendly

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environment. The new version of DSP Builder allows the incorporation of multiple HDL modules or Quartus II software design projects directly into system models.

### [High-Speed Hardware-Tested RLDRAM II Controller Now Available](#)

Supporting up to 300 MHz RLDRAM II memory interfaces in Stratix II FPGAs, this parameterizable, hardware-tested memory controller will shorten your design time. A full license to this core is part of the IP Base Suite, which is included in a Quartus II software subscription.

### [x8 PCI Express MegaCore Now Available](#)

New features of the PCI Express Compiler version 2.0.0 include support for x8 PCI Express links, Stratix II GX FPGAs (x1/x4/x8), and Cyclone II FPGAs (x1/x4) with PIPE compatible transceivers - including a preset configuration for use with the TI XIO1100 x1 PHY.

### [Stratix II GX Optimized SerialLite II MegaCore Improves Performance](#)

SerialLite II is Altera's second-generation lightweight serial protocol for a range of chip-to-chip, board-to-board and backplane interconnect applications. SerialLite II extends the performance range from 622 Mbps to 102 Gbps in Stratix II GX FPGAs and delivers 60% cost savings.

## Technology & End Markets

### [Lower Costs in Broadcasting Applications Using Cyclone II FPGAs](#)

Learn how implementing DSB-ASI and SDI solutions in Cyclone II FPGAs can reduce development costs, production costs, board space, and complexity. Tested solutions for these interfaces are readily available from Altera for demonstration and implementation.

### [Reduce System Costs by Integrating PCI Interface Functions into CPLDs](#)

While many PCI bus interfaces are implemented using ASSPs, the most common functions of PCI target interfaces can be implemented with CPLDs. Examine this new white paper from Altera to find out how to reduce costs, add flexibility and reduce board space.

### [Get High-Speed Design Tools at the New Signal Integrity Center](#)

The Signal Integrity Center offers design resources that are essential for high-speed interface design. Resources include FPGA and board design guidelines, software simulation tools, models, characterization reports and test platforms.

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## Events, Training & Net Seminars

### [Register: Simplify Your High-Speed Serial Design Net Seminar](#) **Free**

November 16, online--Attend this net seminar to find out how FPGAs can simplify your high-speed serial design while maintaining low power and optimal signal integrity. Understand how complete protocol solutions will shorten design cycles and minimize risk.

### [See Altera at SDR'05, Software Defined Radio Technical Conference](#)



November 14-18, Orange County, CA - SDR applications are becoming a reality, fueled by Altera® FPGAs. Come listen to the opening keynote: "FPGA and Structured ASIC Design Methodologies for SDR Applications" by Dr. Misha Burich, Senior VP - Software and System Engineering at Altera.

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## Altera in the News

### [SerDes Sweet Spot, FPGA Journal](#)

Read the FPGA Journal review of Stratix II GX to understand how Altera's new device family operates with the best possible signal integrity and the lowest possible power in the 622Mbps to 6.375Gbps range.

### [Vendors preview FPGA-based WiMax modem, EDN](#)

Learn how FPGAs allow developers to deliver programmable, low-cost, WiMax-compliant products that can be upgraded in the field to meet changing customer requirements and market conditions.

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