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InsideEdge

Altera's Monthly e-Newsletter

Welcome to the May 2006 issue of the *Inside Edge*, bringing you the latest news about Altera's products and solutions.

Monthly Spotlight

[Improve Productivity with New Quartus II v6.0 Design Software](#)

New Quartus® II software version 6.0 is #1 in performance and productivity for CPLD, FPGA and structured ASIC designs. New features in version 6.0 include TimeQuest, an ASIC-strength timing analysis tool with native Synopsys design constraints (SDC) support.

Software, Intellectual Property & Development Kits

[Announcing New Nios II Design Tool For Accelerating C Into Hardware](#)

Now Nios® II users have a new design tool to substantially increase the performance of their embedded software. This tool automates the conversion of performance-critical ANSI C subroutines into fast hardware accelerators in the FPGA, thereby reducing a manual task from weeks to minutes.

[Download the Nios II Embedded Design Suite v6.0 Today](#)

Download the new Nios II EDS version 6.0 release, featuring a complimentary evaluation of the Nios II C-to-Hardware Acceleration Compiler. Also new in version 6.0: a library of floating point custom instructions and a Nios II plug-in for the Quartus II SignalTap® II. [Learn more about the Nios II processor](#)

[Improve Cost & Productivity with New Video & Imaging Solutions](#)

Improve cost and productivity with Altera's modular, programmable video and image processing solutions. The solutions include a video and image processing intellectual property (IP) suite, development kits, a complete reference design, and a new training class. [Download Now](#)

[Now Shipping--Cyclone II PCI Express x1 Development Kit--US\\$1500](#)

Develop and prototype your PCI Express design today using the Cyclone™ II PCI Express x1 Development Kit available through Knott Systems (www.knottsystems.com). This kit contains all the hardware, software and documentation you need to rapidly develop your PCI Express-based system.

May 2006

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Technology & End Markets

[Blaupunkt Uses Altera Solution to Deliver Advanced Auto Navigation](#)

Find out how Blaupunkt, using a Cyclone II-based programmable logic platform with a Nios II embedded processor, cut six months off its development time and minimized component count for its latest auto navigation product.

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Events, Training & Net Seminars

[Net Seminar: Accelerating FPGA Timing Analysis Net Seminar](#) **Free**

Find out how TimeQuest, the new ASIC-strength timing analyzer included in the Quartus software, can help you create, manage, and analyze complex timing constraints, and to quickly perform advanced timing verification with native SDC support. [Register Now](#)

[Net Seminar: ASIC Prototyping Using FPGAs](#) **Free**

Discover how Altera® FPGAs can be used with Mentor Graphics® synthesis tools to partition and synthesize ASIC prototypes. This net seminar shows you how to minimize verification time and accelerate your time-to-market.

[Register Now](#)

[Seminar: High Performance Backplane Interconnect Solutions](#) **Free**

May 25, Bedford, Massachusetts - Learn how to use FPGA-based transceivers to dynamically tune signal integrity. See demonstrations of TX and RX equalization techniques that aid developers in achieving a low bit-error rate (BER), high-performance interconnect, and shortened development cycles.

[Register Now](#)

[Visit Altera at the Largest EDA Industry Event – EDA Tech Forum](#)

Come and see Altera's latest technology at any one of 18 worldwide locations. These one-day forums provide the opportunity to hear industry expert keynotes and then customize your forum schedule by taking part in the technology sessions that are of most interest to you.

[Discover Altera's Automotive Solutions at the D & E Forum](#)

May 16, Ludwigsburg, Germany - Visit Altera at the Design & Elektronik Forum to learn how multi-processor systems based on FPGAs and structured ASICs are offering a scalable and flexible alternative to automotive microcontrollers.

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Support & Literature

[White Paper: MAX II CPLD Hot-Socketing \(PDF\)](#)

Are you using MAX[®] II CPLDs on a board which contains several voltage levels or complex power up sequences? This white paper describes the I/O characteristics of MAX II when various internal and I/O voltage power-up sequences are used.

[Application Note: MAX II ISP Update with I/O Pin Data Retention \(PDF\)](#)

This application note provides design examples of how you can use the MAX II CPLD in-system programming feature to perform field system updates while retaining I/O register data. This feature ensures glitch-free SRAM download in your system.

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Altera in the News

[Altera tool accelerates C into hardware in Nios II-based systems, EE Times](#)

Learn how the new Nios II C-to-Hardware Acceleration Compiler automatically converts C language subroutines into hardware accelerators and integrates them into FPGA-based Nios II subsystems.

[Design Idea: CPLD automatically powers itself off, EDN](#)

Find out how you can conserve battery power by adding a few discrete components to a CPLD to implement a battery-powered system's power-down circuit.

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