

August 2007 *Inside Edge*

Bringing you the latest Altera® product and solution news.

## Monthly Spotlight

### [New Arria GX FPGAs Now Available in the eStore](#)

Arria™ GX FPGAs are now available to buy online. These low-cost, transceiver-based FPGAs are optimized to support the PCI Express, Gigabit Ethernet, and Serial RapidIO™ standards. You can create Arria GX designs using the free Quartus® II Web Edition software.

## FPGAs, CPLDs & Structured ASICs

### [Arria GX FPGAs pass PCI Express PCI-SIG compliance](#)

Arria GX FPGAs successfully passed PCI Express certification at the 55<sup>th</sup> PCI-SIG Compliance Workshop. Arria GX devices are just one part of Altera's complete PCI Express solution, which also includes development kits, MegaCore® IP functions, reference designs, and online training.

[Back to Top](#)

## Software, Intellectual Property & Development Kits

### [New Synplify ValuePack for Cyclone FPGA series](#)

The Synplify® ValuePack synthesis and debug tool can help you get your Cyclone® series design to fit into the smallest device and to get it out the door, saving you time and money. Starting at just \$995, Synplify ValuePack software could pay for itself in only one production design.

### [New complete USB 2.0 solution from SLS](#)

The new SLS USB 2.0 device controller solution is made up of a configurable, SOPC Builder-Ready IP core, extensive software and documentation, and PHY daughtercards. It's available for immediate download, evaluation, and purchase for quick and easy implementation.

[Back to Top](#)

## Technology & End Markets



**Guidelines for Designing Gigabit Channels**

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## Did You Know...

Which book is the all-time best seller? It's not Harry Potter!  
[Find out.](#)



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## [SI Prescription with Dr. Bogatin: Don't breathe too hard](#)

If you think you have enough to worry about in designing high-speed serial links, here comes a new one: humidity. Read more about this new study by Intel and Tyco, entitled "Humidity-Dependent Loss in PCB Substrates".

[Back to Top](#)

## Events, Training & Net Seminars

### [Online PCI Express training now available](#) **Free**

Quickly get up to speed on Altera's PCI Express solutions by taking this new online training. You'll learn how to implement a PCI Express endpoint solution using Stratix® II GX or Arria GX FPGAs, IP cores and a PCI Express development kit, and see available design resources.

### [Net seminar: Accelerate HPC applications with AMD & Altera](#) **Free**

Are you ready to speed up your high-performance applications without drastic increases in your power budget? Join AMD and Altera in this net seminar to learn how to gain maximum performance and lower power consumption at a better price/performance ratio than processors alone.

### [Updated Quartus II software basic training class \(\\$495\)](#)

Held in locations around the US, this instructor-led class teaches how to use Quartus II software v7.1 to develop a design on an FPGA or CPLD. You'll create a new project, enter design files, compile to your target device, and configure it to see the design working in-system.

### [Discover Altera's HD Quality Solutions at IBC 2007](#)

September 7-11, Amsterdam, Holland: Visit Altera at the RAI Congress Centre, Hall 10, Booth 100, to see how to deliver the highest video quality. Altera and its partners can help you create IP-based equipment for tomorrow's HD applications. Visit our booth to learn more.

[Back to Top](#)

## Support & Literature

### [From the Forum: Satisfying hard routing constraints in FPGA design](#)

Altera Forum user **Tristan** made some changes to his Cyclone II design, and now he's looking for help on getting it to fit. Read the comments and solutions that other Forum users suggested, then post your own questions, tips, and tricks today!

### [New error correction code megafunction user guide \(PDF\)](#)

Released with Quartus II software v7.1, the error correction code (ECC) megafunction enables error detection at the receiver side and correction of corrupt data in a digital data transmission system. The user guide gets you started quickly with design examples, including simulation.

### [New ROM megafunction user guide \(PDF\)](#)

Learn to quickly configure a read-only memory (ROM) with asynchronous clears, different modes, enables such as read, clock, and address clock, and other features. This user guide provides design examples such as implementing and instantiating a single-port ROM.

### [Have questions about embedded design?](#)

Whether you are considering adding a processor to your system or have designed with the Nios<sup>®</sup> II processor for years, visit the Embedded User Community to interact with thousands of designers. Once there, you can post questions, read others' comments, and find new ideas.

### [Check out the new Altera Knowledge Database](#)

Altera's new Knowledge Database can be your first stop for technical support. It includes a library of support solutions, known issues, troubleshooters, and other self-help tools to help you find answers more quickly. Try it out today!

[Back to Top](#)

## Altera in the News

### [Running an FPGA at ASIC speed, EDN.com](#)

Texas Instruments' hardware-emulation team needed to prototype a next-generation wireless handset processor, and needed to do it fast. Multi-FPGA design was clearly the way to go. Could they partition, debug, and run as fast as the ASIC without changing the RTL? See how they did it.

[Back to Top](#)

## Most Popular News from Last Issue

### [Inspiration for embedded designs: Award-winning white papers](#)

Check out the top 18 white papers of the 2006 Nios II Embedded Processor Design Contest, with finalists selected from over 500 entries. See how you can use Nios II processors in applications such as: encryption, image and audio processing, networking, security, and signal processing.

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