

ALTERA**InsideEdge**

Altera's Monthly e-Newsletter

February 2007 **Inside Edge**

Bringing you the latest Altera® product and solution news.

Monthly Spotlight**[Design with Stratix III FPGAs—30-day software trial!](#) **Free****

Ready to try out Altera's lowest power high-performance Stratix® III FPGAs? Download the Subscription Edition of Quartus® II software at no cost for 30 days. You'll get all of its productivity tools, like timing and power analysis, incremental compilation, SOPC Builder, and more!

FPGAs, CPLDs & Structured ASICs**[New: Industry's first and only ITAR-compliant structured ASICs](#)**

Does your military or aerospace application require ITAR-compliant ASICs but need lower risks with faster time-to-market? HardCopy® II devices are the only high-performance structured ASICs with an ITAR-compliant design and manufacturing flow, approved by the Department of State.

[Reduce board size with new MAX II packages](#)

With their new small form-factor packages, new power-down capability, and the industry's lowest cost, MAX® II CPLDs offer 50% lower power, 2x I/O pins, and 3x the logic in the same board space vs. competing CPLDs. Design for these tiny packages free with Quartus II Web Edition software.

[Tired of guessing at SI settings for your FPGA's transceiver?](#)

Altera's pre-emphasis and equalization link estimator (PELE) SI technology saves you weeks--it determines optimal SI settings to simulate and predict link performance, and even sets up SPICE for you. Get it now as part of a Mentor Graphics Stratix II GX design kit.

[Stratix II FPGAs now support military temperature range operation](#)

Military systems operate in rougher conditions than most electronics and still require the flexibility and performance offered by high-end FPGAs. Of all 90-nm high-end FPGAs, only Altera's Stratix series supports military temperature range operation (-55°C to +125°C).

[All Stratix II GX family members are now in production](#)

Stratix II GX FPGAs, the only production FPGAs to support 6-Gbps data rates, are part of a complete solution that includes boards, tools, IP, characterization, and collateral. Use Stratix II GX FPGAs to simplify your next board layout and protocol implementation.

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**On the Edge**

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See the first-ever comic devoted to the programmable logic industry.

Inside Edge Poll

Which HDTV technology do you own or...

[Take the poll. See the results.](#)

Did You Know...

...why only women give presents on Valentine's Day in Japan?

[Find out.](#)

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Software, Intellectual Property & Development Kits

[Free evaluation: Nios II C-to-hardware acceleration compiler](#) **Free**

Download the latest version of the Nios® II Embedded Design Suite to evaluate the Nios II C2H Compiler. This productivity tool boosts the performance of your time-critical ANSI C functions by converting them into hardware accelerators in the FPGA. [Download now.](#)

[What should you consider when planning your design? \(PDF\)](#)

The new Design Planning chapter in the Quartus II Handbook provides tips on planning your design to take advantage of Quartus II features that help improve your productivity. Download it today!

[Perform board-level SI simulations for high-speed designs \(PDF\)](#)

For accurate board-level signal integrity simulations, you need accurate I/O models. Learn how easy it is to create I/O models with the IBIS and HSPICE Writers in the Quartus II software.

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Technology & End Markets

[SI prescription with Dr. Bogatin: Approaching transparent connectors](#)

The higher the bit rate, the more problems connectors introduce. Dr. Bogatin discusses two technology options that could be building blocks in the next generation of connectors. Learn about signal integrity (SI) from Dr. Bogatin, and submit your nagging SI questions to the SI doctor.

[FPGAs bring flexibility to the industrial market](#)

If your challenges involve dealing with obsolescence, cost reduction, and rapidly changing industrial Ethernet technologies, Altera's industrial-grade FPGAs can help. Visit the Altera web site's section on the industrial market to learn more.

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Events, Training & Net Seminars

[Three new instructor-led customer training classes now available](#)

Enhance your design skills with our new Quartus II training classes:

- [Foundation](#): Get started with the basics of Quartus II design
- [Verification](#): Learn advanced verification and debugging techniques
- [Optimization](#): Improve design performance and utilization

[Visit Altera at the Software Radio Summit & Software Radio University](#)

February 20-23, 2007, Tyson's Corner, Vienna, VA — Attend the Software Radio Summit and Software Radio University events to learn about Altera's solutions for military software-defined radio (SDR) solutions. The events will have technical tracks and updates on the JTRS program.

[Net seminar: Reducing FPGA design compile times](#)

Learn how your software can increase your productivity. With Quartus II v6.1 software, you can recompile specific design areas while preserving performance in the areas that haven't changed. Using incremental compilation, you'll reduce your compile times for faster timing closure.

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Support & Literature

[Design example: Test system connection to RAM & flash](#)

Accelerate board bring-up with the Memory Test design example, which tests the operation of your board's external RAM and flash. This design example also demonstrates the direct memory access (DMA) controller peripheral and Nios II flash application program interface (API).

[Design example: High-performance multiprocessor Nios II design](#)

With SOPC Builder, creating multiprocessor systems is easy! This high-performance multiprocessor design example has three Nios II CPUs and a simple software application that shows how to use the mutex component and shared on-chip memories for interprocessor communication. Download now.

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Altera in the News

[How to achieve faster compile times in high-density FPGAs, Programmable Logic DesignLine](#)

This article describes three steps you can take to reduce compile times on your next high-density design. For example, using the latest place-and-route algorithms can cut your compile times by up to 47%!

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Most Popular News from Last Issue

[Using MAX II CPLDs as Analog Keyboard Encoders \(PDF\)](#)

Download this application note to find out how MAX II CPLDs can be used to decode a large number of switches in a keypad or keyboard with only two I/O pins and a GND pin.

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